A LOW VOLTAGE LOW POWER CMOS BASED 4GHz VCO FOR RF APPLICATIONS

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Abstract: - This paper presents a novel circuit design of a CMOS LC voltage controlled oscillators. Being a crucial part in RF front-ends, the voltage-controlled oscillator (VCO) is considered as one of the most power-consuming components. The proposed VCO is suitable for low voltage and low power application. By replacing the tail current source by an inductor, VCO operates at reduced supply voltage. Adding one more pair of switching transistor, achieves low power dissipation and maintains the circuit performance in terms of voltage swing and tuning range. The simulation results of the proposed topology are compared with the reference circuit, to establish the usefulness of the circuit. Both proposed and references VCOs are simulated and realized in a 0.18 µm CMOS process technology. The proposed VCO is consuming a dc power of 7.02 mW at 0.5V supply voltage and 12.1 mW at 0.6V supply voltage. VCO exhibits a frequency tuning range of 2.8%. The dc power consumption for reference VCO is 12.3 mW at 0.5V supply voltage and 35.37mW at a 0.6V supply voltage.

Key-Words: - Low-voltage, low-power, capacitive feedback, voltage controlled oscillators (VCOs) and RF applications

1 Introduction

The beginning of the twenty-first century will be remembered for the tremendous growth in mobile and wireless communications. Driven by economical and technological forces, small and low-cost handheld devices have invaded the market. Technology improvements and market growth have been pushing for higher quality of service in transmission and reception of information at faster data rates. Third generation (3G) communication systems enable high-speed data communication, mobile Internet, E-mail, video on demand, and E-commerce as from [1], [2], [3]. Short-range wireless local area networks (WLAN) have also emerged, leading to standards such as the IEEE802.11a and its European counterpart HIPERLAN, that target for 54Mbps at 4 GHz and 5GHz, while the IEE802.11b and the recent IEEE802.11g enable data rates of 11Mbps and 22-50Mbps, respectively, at 2.4GHz [4]. With this the emerging applications such as wireless personal area networks (WPANs), wireless sensor networks, RFICs and RF identification (RFIDs) for short-range communication also attracted researchers toward them.

Because of the required threshold voltage and the inherently low trans-conductance of the MOSFETs, it is extremely difficult to operate RF front-end circuits with reduced supply voltage and power dissipation, especially for multi-gigahertz applications [5]. The voltage-controlled oscillator (VCO) is considered as one of the crucial part in the RF front-ends. It is also a main power-consuming component. Oscillators with low supply voltages and low power are reported in [6]–[11]. However, because of low voltage and low power most of the circuits suffer from reduced output swing and degraded phase. Works on phase noise are reported in [12]-[22]. In this paper, a VCO topology suitable for low-voltage and low-power operations for RF applications is presented. Using a 0.18-µm CMOS technology, a 4-GHz VCO is realized.

The remainder of this paper is organized as follows. Section 2 describes the proposed circuit topology and analysis. The circuit design with proposed methodology and the simulation results of the proposed CMOS VCO are presented in Sections 3 and 4, respectively. Finally, conclusion and future work are given in Section 5.

2 Proposed VCO Topology

The schematic of the proposed VCO is shown in Fig. 1.
In order to reduce the power consumption the differential topology is used, to reduce the required supply voltage and to eliminate additional noise contribution, the tail current transistor in the differential Colpitts VCO no. 2 of [11] is replaced by an on-chip inductor. For an enhanced voltage swing under low supply voltage, the capacitive-feedback technique is employed for M1 and M2. Due to the use of the on-chip inductor and the feedback loop established by \( C_1 \) and \( C_2 \), the drain and source voltages can swing above the supply voltage and below the ground potential as shown in Fig. 2. Consequently the output swing of the VCO is enhanced, leading to superior phase noise.

2.1 Design Procedure

The main design issues for a VCO are central frequency of oscillation, tuning range, DC power dissipation, voltage swing and phase noise. In this design first we calculate the relation for the central frequency. Then we calculate the relation for small signal gain, as small signal gain decides the DC power dissipation. And finally we calculate the expression for voltage swing.

\[
R_1 \approx \omega^2 L_1^2 / R_{s_1}
\]  
(1)

\[
R_2 \approx \omega^2 L_2^2 / R_{s_2}
\]  
(2)

where \( R_{s_1} \) and \( R_{s_2} \) are the equivalent series resistances of L1 and L2 respectively. Besides, the transistor parasitic capacitances, which are much smaller than the values of \( C_1 \) and \( C_2 \), are neglected. The transfer function between \( V_0 \) and \( V_i \) is given by

\[
\frac{V_0}{V_i} = -\frac{g_m(b_2 s^2 + b_1 s + b_0)s}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}
\]  
(3)

where for simplification, assuming \( R_1 = R_2 = R \) and \( L_1 = L_2 = L \). The constants in (3) are as follows:

\[
b_0 = g_m R^2 L
\]

\[
b_1 = R^2 L C_2 + 2g_m R L^2
\]

\[
\approx R^2 L C_1, \ldots\ldots(\text{RC} \gg g_m L)
\]

\[
b_2 = 2g_m R^2 L^2 C_2 + 2g_m R L^2 C_2 + 2RC_1 L^2
\]

\[
\approx 2g_m R^2 L^2 C_2 + 2RC_1 L^2 \ldots \ldots g_m C_2 << C_1
\]

\[
a_0 = g_m R^2,
\]

\[
a_1 = 2g_m R L + 2g_m R^2 L + R^3 (C_1 + C_2)
\]

\[
a_2 = \left( 2g_m R^2 L + 2g_m R L^2 + 2g_m R^2 L (C_1 + C_2) \right)
\]

\[
\approx \left( 2g_m R^2 L (C_1 + C_2) + 2RL(C_1 + C_2) \right)
\]

\[
\ldots \ldots (g_m R \equiv 1, g_m L \ll R(C_1 + C_2))
\]

\[
a_3 = \left( R^2 C_1 C_2 L + 2g_m R^2 L R(C_1 + C_2) + 2L^2 (C_1 + C_2) \right)
\]

\[
a_4 = 2g_m R^2 L^2 C_1 C_2 + 2RL^2 C_1 C_2
\]

From (3) it is clear that this topology provides the negative resistance to the LC tank circuit, so the circuit oscillates if the negative resistance overcomes the loss in the tank circuit.
The condition for circuit to oscillate is the loop gain should be unity or more, which corresponds to a voltage gain \( V_0/V_i = -1 \) at the oscillation frequency \( \omega_0 \). Therefore, by putting the value of \( V_0/V_i = -1 \) in (3) we get,

\[
-1 = -\frac{g_m(-b_2\omega_0^2 + b_1j\omega_0 + b_0)j\omega_0}{a_4\omega_0 + a_3j\omega_0^2 + a_2\omega_0 + a_1j\omega_0 + a_0}
\]

(4)

With proper arrangement, (4) yields the oscillation frequency as well as the small signal gain. The oscillation frequency is calculated by comparing the even powers of \( \omega_0 \) and small signal gain is calculated by comparing the odd powers of \( \omega_0 \). The oscillating frequency for this new VCO is given as follows

\[
\omega_0 \approx \sqrt{(C_1 + C_2)/LC_1C_2}
\]

(5)

The small signal gain is given by

\[
g_mR \approx 1
\]

(6)

From (5) it is clear that the variation in \( C_1/C_2 \) has the influence on the VCO frequency. As a result the capacitor \( C_1 \) is kept constant and \( C_2 \) is realized by varactor in this design to vary the \( C_1/C_2 \) ratio. It is easy to implement \( C_2 \) using varactor as compare to \( C_1 \). Once the capacitor ratio is determined, the required trans-conductance of the cross-coupled transistors can be estimated by (6). Here we have assumed an inductor value of 2 nH, an oscillator frequency of 5 GHz and Q=12.

Output Voltage Swing: Due to the in-phase relationship provided by the capacitive feedback and the use of on-chip inductor, the drain and source voltage can swing above the supply voltage and below the ground potential, as illustrated in Fig. 2. The output voltage swing of the VCO is derived from the time-domain waveform of the drain current \( I(t) \) of M1, as shown in Fig. 4. For simplicity, the periodic drain current is modeled by a square wave with a period of \( T = 2\pi/\omega_0 \) and amplitude \( I_0 \).

\[
I(t) = \begin{cases} 0 & -T < t < 0 \\ I_0 & 0 < t < T \end{cases}
\]

Fig. 4. Modeled drain current waveform of the transistor M1.

The maximum drain current occurs when the gate voltage of M1 or M3 reaches its peak value. Assuming that the amplitude of output oscillating signal is \( P \), the gate voltages \( V_{G1} \) and \( V_{G2} \) are \( V_{DD}-P \) and \( V_{DD}+P \), respectively, while the source voltages of M1 and M2 are \( V_{SS1} \) and \( V_{SS2} \), can be obtained by the voltage divider of \( C_1 \) and \( C_2 \). Thus, \( I_0 \) is approximated by the maximum drain current with the transistor M1 operating in the non-saturated region

\[
I_0 = \mu_mC_{ox}\frac{W}{L}\left[\left(V_{DD}+P+nP-V_i\right)\left(V_{DD}-P+nP\right)\right]
\]

(7)

where \( n=C_1/ (C_1+C_2) \). From the Fourier series of \( I(t) \), the fundamental current component is given by

\[
[I(t)]_{fundamental} = \frac{2}{\pi}I_0\sin\omega_0
\]

(8)

and the fundamental voltage amplitude is

\[
P = \frac{2}{\pi}I_0R
\]

(9)

where \( R \) is the load resistance. From (7) and (9), a simplified expression of the VCO output swing is given by

\[
P \approx \left(1 + C_1/C_2\right)V_{DD}
\]

(10)

According to (10), the simulated VCO output voltage is a function of \( C_1/C_2 \) ratio and supply voltage as depicted in Fig. 5. It is obvious that an output voltage swing significantly larger than the supply voltage can be achieved by the proposed capacitive feedback. But in proposed VCO, peak-to-
peak amplitude follows equation (10) only up to the capacitor ratio of 0.3.

Fig. 5. Simulated peak-to-peak amplitude at the VCO output.

### 3 Methodology and Circuit Design

The design procedure of the proposed VCO is already discussed in section II. So according to the steps followed, the proposed methodology is shown in Fig. 6. The circuit design starts with the inductors L1 and L2. For simplification, both inductors are chosen to be identical as L, which are optimized for a high-Q factor at the frequencies of interest. Here the inductors are assumed to be equal to 1.5 nH with the oscillation frequency of 4 GHz and the loss resistance R=633 ohm as from the data of [6]. Once the inductance is determined, the required value of C1 and C2 can be obtained from the designed oscillation frequency by (5) assuming C1/C2=0.25 as discussed in [24] as the initial value. The required trans-conductance of the cross-coupled transistors can be calculated from (6) and finally the sizing of transistors can be calculated. Considering the design specifications such as the, output swing, tuning range, and power consumption, the optimum is thus determined and the circuit parameters including the capacitance values and the transistor aspect ratio can be calculated accordingly. Finally, optimization is performed and design iterations may be needed to satisfy the required circuit performance.

In this section, circuit analysis of the proposed VCO has been done. By the circuit analysis it can be concluded that this topology can be used for lower supply voltages as well as the power dissipation is reduced in this design. Finally the design methodology is presented in this section and by using this methodology circuit design parameters are calculated and tabulated in Table 1.

#### Table 1: Circuit Parameters of the VCO

<table>
<thead>
<tr>
<th>Devices</th>
<th>Design Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>40µm/0.18µm</td>
</tr>
<tr>
<td>L1, L2</td>
<td>L 1.5nH</td>
</tr>
<tr>
<td>C1</td>
<td>0.625pF</td>
</tr>
<tr>
<td>C2</td>
<td>2 pF-3pF</td>
</tr>
<tr>
<td>C1/C2</td>
<td>0.2-0.3</td>
</tr>
<tr>
<td>g_m</td>
<td>1.5mA/V</td>
</tr>
</tbody>
</table>

Fig. 6. Methodology for the design of the low-voltage VCO.

#### 4 Simulation Results

The differential simulated output voltage is shown in Fig. 7. The simulated results for output Voltage swing is shown in Table 2. This Table shows that the output voltage swing follows (10) for the capacitor ratios from 0.1 to 0.3. But for C1/C2 = 0.4 voltage swing decreases. So from here C1/C2 ratio is optimized and selected from 0.2 to 0.3. As
for the lower value of capacitor ratio the value of $C_2$ is more and it is difficult to realize larger varactor.

Simulation result for the Current consumption from the supply voltage and power dissipation is shown in Table-3, we have seen that as the supply voltage increases the current consumption will be more. The results are very obvious as the voltage increases the current will also increases so the power. Note that the current consumption and power dissipation is independent of capacitor ratio.

<table>
<thead>
<tr>
<th>C1/C2</th>
<th>VDD= 0.4V</th>
<th>VDD= 0.5V</th>
<th>VDD= 0.6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>1.13319</td>
<td>1.4654</td>
<td>1.80939</td>
</tr>
<tr>
<td>0.2</td>
<td>1.31561</td>
<td>1.69506</td>
<td>2.10609</td>
</tr>
<tr>
<td>0.25</td>
<td>1.36245</td>
<td>1.7746</td>
<td>2.17561</td>
</tr>
<tr>
<td>0.3</td>
<td>1.55625</td>
<td>1.90339</td>
<td>2.26343</td>
</tr>
<tr>
<td>0.4</td>
<td>1.30623</td>
<td>1.60936</td>
<td>1.94363</td>
</tr>
</tbody>
</table>

Table 2: Output Voltage Swing (V) variation with capacitor ratio and supply voltage

Table 3: Current consumption and Power dissipation with supply voltage

<table>
<thead>
<tr>
<th>VDD</th>
<th>Supply Voltage Current (mA)</th>
<th>Total Power Dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>8.984</td>
<td>3.59</td>
</tr>
<tr>
<td>0.5</td>
<td>14.04</td>
<td>7.02</td>
</tr>
<tr>
<td>0.6</td>
<td>20.2</td>
<td>12.1</td>
</tr>
<tr>
<td>0.7</td>
<td>27.51</td>
<td>19.3</td>
</tr>
<tr>
<td>0.8</td>
<td>35.93</td>
<td>28.7</td>
</tr>
<tr>
<td>0.9</td>
<td>45.48</td>
<td>40.92</td>
</tr>
</tbody>
</table>

Frequency is an important issue for a VCO. The expression for the frequency is given by equation 5. The simulated result for the frequency versus $C_1/C_2$ ratio is plotted in figure 8. The variation of frequency with supply voltage is also important and is observed in Fig. 8. It is verified that, as $C_1/C_2$ ratio increases, the frequency of operation also increases. The simulation result for the frequency versus supply voltage is plotted in Figure 9.

To facilitate the evaluation of power dissipation improvement of the proposed VCO, a reference VCO i.e. Hung’s circuit using the same model parameters are simulated in P-SPICE. The current consumption versus supply voltage and power dissipation results for the Hung’s are shown in Table 4. By comparing Table 4 with Table 3, we conclude that, there is a reduction in the current consumption and power dissipation for the Proposed VCO.

<table>
<thead>
<tr>
<th>VDD</th>
<th>Supply Voltage Current (mA)</th>
<th>Total Power Dissipation (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>24.56</td>
<td>12.3</td>
</tr>
<tr>
<td>0.6</td>
<td>35.37</td>
<td>21.2</td>
</tr>
<tr>
<td>0.7</td>
<td>48.1</td>
<td>33.7</td>
</tr>
<tr>
<td>0.8</td>
<td>62.89</td>
<td>50.3</td>
</tr>
<tr>
<td>0.9</td>
<td>79.59</td>
<td>71.6</td>
</tr>
</tbody>
</table>

Table 4: Current consumption and Power dissipation with supply voltage for Hung’s Circuit

Fig. 8 Frequency verses $C_1/C_2$ ratio (VDD=0.5V)
On the basis of last section, we can conclude that the proposed VCO has reduced current consumption and power dissipation as compared to the Hung’s topology. The proposed VCO when operating at a supply voltage of 0.5V, the VCO consumes a DC power of 7.02 mW and the current consumption is 14.07 mA. From Figure 8, tuning characteristics is measured. As C1/C2 ratio changes from 0.2 to 0.3, the 4 GHz VCO exhibits a frequency tuning range of 2.8 %. Tuning range can be increased to 6.8 % with C1/C2= 0.1. For low voltage operation, the sensitivity to the supply voltage is also investigated. The performance of the VCO is summarized in Table 5 along with reference circuit (Hung’s circuit).

5 CONCLUSIONS AND FUTURE WORK

Using a 0.18-µm CMOS technology, a VCO operating at a reduced power dissipation and supply voltage is presented. The performance of the circuit is characterized with a supply voltage of 0.5 V. Due to the use of the capacitive feedback, significant performance improvement in terms of output swing, power dissipation, is demonstrated, making it extremely attractive for low-power and low-voltage RF applications. A reference VCO, i.e. Hung’s circuit, is also realized and simulated for performance comparison with the proposed VCO to establish the usefulness of the proposed topology. In the reference VCO, power dissipation is measured to be about 12.3 mW at 0.5V and 35.37mW at 0.6V. The proposed VCO’s power dissipation is found to be 7.02mW at 0.5V and 12.1mW at 0.6V. Therefore, the power dissipation has been reduced in proposed VCO. Also the proposed VCO can work under supply voltage less then 1V. The number of inductors in proposed VCO topology has been reduced to 3 as compared to the reference circuit. Further, the phase noise in comparison to the conventional VCOs is less. As no tail current source is there and the tail current source is considered as the main contributor to the phase noise, but as compared to the reference circuit it will be more because of added switching transistors.

Phase noise is an important design factor for the designing of a VCO in deep submicron technology. The optimization can be performed by considering the phase noise. Further, better performance can also be achieved by using some more accurate inductor and capacitor models.

References:


