A Saw-tooth Wave Based Design of Time to Digital Converter

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Abstract: - We propose an alternative approach for time interpolation of TDC in which a saw-tooth wave is generated instead of using sinusoidal wave in [10]. The proposed approach avoids floating number operation as well as lowers the dependency on analog passive components. Since the differential portion of two projected signals is amplified in the interpolation circuit, the wider range of time interval can be measured while preserving a few picoseconds resolution. It is also expected that the computational burden of DSP is decreased as well as its repeatability is enhanced.
Compared with the conventional analog interpolation approach, the proposed saw-tooth based interpolation TDC overcomes the drawbacks of conventional analog interpolation TDC by reducing the dependency on passive components which are sensitive to environment and operational conditions. It provides high repeatability and linearity property within a wide range of operation with high resolution of measurement. With the aid of proposed interpolation circuit, a practical TDC and its embedded measurement system are expected to be implemented. The experiment results demonstrate its feasibility and effectiveness for practical usage with a simple and low cost implementation.

Key-Words: - Saw-tooth wave, Time to Digital Converter(TDC), Laser, Measurement, robust

1 Introduction

Time to digital converter(TDC) is a measurement circuit for infinitesimal time difference between rapid transit signals. Since the time of flight(TOF) of traveling light pulse is in proportion to distance to an object, TDC is required to be sensitive enough to measure picoseconds unit for target object in minimum distance.

Considering its cost and accessibility to passive components, the majority of TDC researches focus on analog interpolation rather than digital interpolation method. Analogue interpolation measures time by using low clock frequency after linearly expanding the minute time interval [2][4][5][6][11][12][13]. On the other hand, digital interpolation method uses gate delay to estimate TOF for traveling light pulse [1][2][7][8][9][14][15][16]. While the measurement system using digital interpolation TDC ensures its precision and repeatability, its cost is mostly higher than the analog interpolation TDC equipment. That is, compared with digital interpolation, analog interpolation TDC is cost effective due to usage of cheap passive components. Despite of its cost effectiveness, however, the passive components used in analog interpolation TDC are sensitive to temperature variation causing measurement error. Moreover, the non-uniform parts of passive components induce additional error and difficulty in maintaining the expected repeatability of measurement. Instead of using passive components for analog interpolation, an oscillator can be used to generate sinusoidal waves for time interpolation, which avoids the above mentioned difficulties [10]. This method samples and holds sinusoidal waves at the time events of triggering pulses. A drawback is that the sinusoidal wave is hard to catch its distortion and necessitates floating number operation.

We propose an alternative approach for time interpolation of TDC in which a saw-tooth wave is generated instead of sinusoidal wave. The proposed approach avoids floating number operation as well as lowers the dependency on analog passive components. As shown in Fig. 1 and Fig.2, since the differential portion of two projected signals is amplified, the wider range of time interval can be measured while preserving a few picoseconds resolution. It is also expected that the computational burden of DSP is decreased as well as its repeatability is enhanced.

2 Design Concept Description

Fig.1 shows a block diagram of proposed TDC which measures TOF of traveling pulse using a saw-tooth wave.

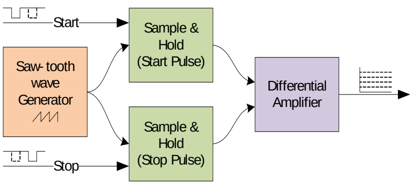

Fig 1. Block Diagram of Saw-tooth Wave Based TDC

In Fig.1, the start signal triggers saw-tooth generator and sample/hold to input its sampled output to the negative input port of differential amplifier. Similarly, the stop pulse activates the operation of saw-tooth generator and sample/hold so that the projected saw-tooth voltage can be submitted to the positive input port of differential amplifier. The amplifier magnifies the small differential voltage signal of two inputs to the extent that the subsequent digital logic circuit measures the corresponding picoseconds time interval. Assuming the saw-tooth wave with positive slope, the output of differential amplifier has positive value and it becomes larger as the time difference of traveling pulse increases. Fig.2 shows the design concept of saw-tooth based TDC where the linear relation of input and output signals is identified before and after amplification.

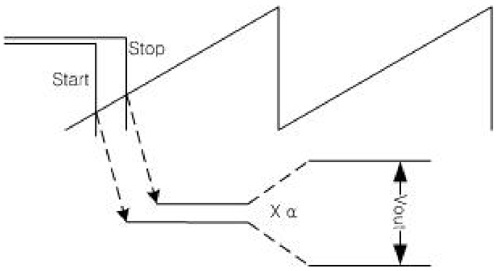

Fig 2. Design Concept of Proposed TDC

3 Implementation

Fig.3 shows an implementation of circuits which realizes the block diagram of TDC in Fig.1.

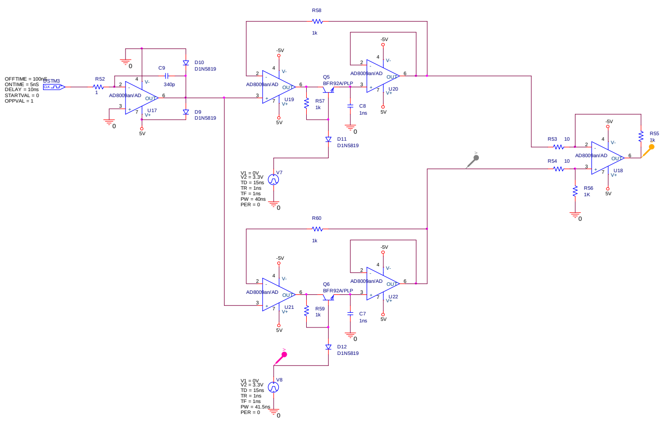

Fig 3. An Implementation of TDC Blocks in Fig. 1

In the figure designed are a saw-tooth generator, two sample and hold circuits, and a differential amplifier. The input signals to these circuits include a synchronizing clock for periodic generation of saw-tooth wave, start and stop pulses, and a reset input for initialization. The saw-tooth wave is sampled at the falling edges of start and stop pulses which necessitates an input synchronizing circuit. For the synchronizing circuit, flip-flops of FPGA are used as in Fig.4. In Fig.5, simulated synchronizing signals are shown for the flip-flop circuit.

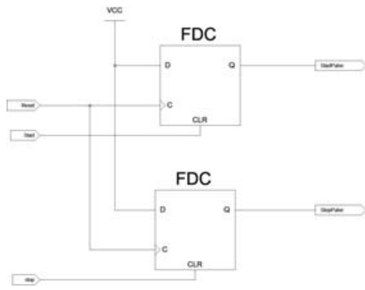

Fig 4. Flip-flop Circuit for Synchronizing Signals

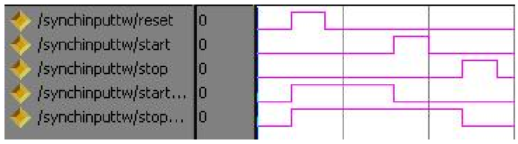

Fig 5. Simulated Synchronizing Pulses

Applying the synchronizing pulses to TDC circuit in Fig.3, the operation of measurement process was tested. After an input of start signal, three stop pulses with 500ps interval are applied to the circuit. In Fig.6, the linear relation of sampled saw-tooth signals is verified and their difference is amplified passing through the differential amplifier.

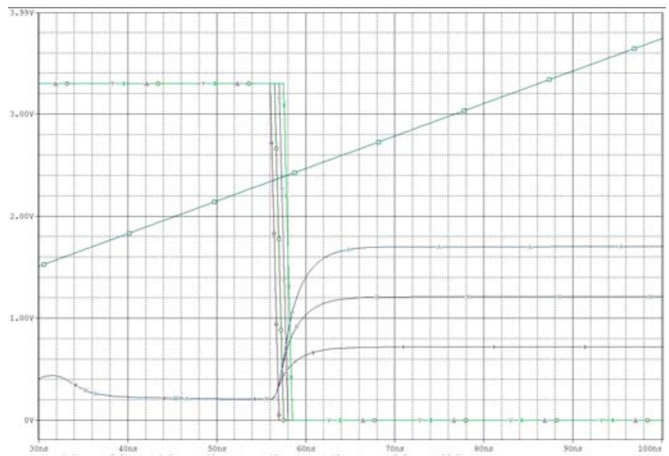

Fig 6. Simulated Measurement Process

The differential voltage of sampled saw-tooth wave is 6mV for the time difference of 500ps between synchronizing start and stop signals. Similarly, the differential voltages of 10mV and 15mV correspond to 1ns and 1.5ns time differences, respectively. The outputs of differential amplifier for the three sampled signals are 716.86mV, 1.21V, and 1.7V, respectively, showing a constant increasing rate of about 500mV. Assuming the maximum voltage output of 5V, a 10bit ADC provides 4.88mV resolution per step corresponding to 4.88ps. When 12bit or 16bit ADC used, the resolution increases to 1.22ps or 0.076ps, respectively. Considering 1/2 LSB error of ADC, these resolutions amount to 9.76ps, 2.44ps, and 0.152ps, respectively, implying the measurement of distance less than mm unit is possible. The resolution of measurement can be also controlled by changing the amplification rate of differential amplifier. This method provides an alternative solution to high resolution measurement otherwise impossible with only a finite slope saw-tooth wave. In summary, our preliminary experiment verifies the effectiveness of using saw-tooth wave in fast and precision measurement of time interval for a wide range of traveling distance while maintaining fine resolution of measurement.

4 Conclusion and Further Works

This paper presents a saw-tooth based interpolation circuit for TDC which overcomes the drawbacks of conventional analog interpolation method using passive components. The proposed TDC circuit reduces the dependency on passive components prone to be sensitive to environment and operational conditions. It provides high repeatability and linearity property within a wide range of operation and also supports high resolution of measurement. The experiment results demonstrate its feasibility and effectiveness for practical usage with a simple and low cost implementation.

Our further work is to design and implement a complete TDC and TDC embedded measurement system including ADC and digital logic circuits using FPGA and DSP.

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