Augmented Digital Zero Crossing Timing Error Detector

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Abstract: - Improvements of data timing synchronization algorithms applying an augmentation of zero cross error detector are presented in this paper. Describing methods are destined for high speed PSK coherent demodulator. Timing error synchronizers are usually the most complicated subsystems in the demodulator, and they can be often limitary for their implementation in the DSP hardware above all for high-rate data transmission. This contribution is focused on feedback timing estimators based on ML-criterion. There are analyzed a modification of zero crossing detection and shown an easy implementation into DSP system.

Key-Words: - Timing error detector, Data decision, Coherent detector, Maximum likelihood, Synchronization

1 Introduction
Synchronization is a pivotal operation in coherent digital receivers, and minimization of error of estimated current carrier frequency, respectively phase, and symbol timing plays the key role for an obtaining of faultless message after demodulation. Symbol timing estimator is more complicated than carrier phase synchronizer and its implementation in DSP systems limits achievable baud-rate of digital receiver. Structures of all feedback timing synchronizers result from a general closed loop, where the tracked parameter is the delay between optimum and actual symbol timings. The analytical description of such a closed loop corresponds to a phase lock loop (PLL) analysis, where the phase error is replaced by the time error or the delay. Consequently, the feedback timing synchronizer presents a delay lock loop (DLL) (Fig. 1).

2 Symbol Timing Synchronization
Considering a general I-Q demodulator, the phase error determination is a simple procedure executed by the Phase Error Detector (PED). The phase can be easily extracted from the signal components (I and Q) for any sample:

$$\phi = \arctan\left(\frac{y_Q}{y_I}\right)$$

(1)

An extraction of optimal sampling time for particular symbol is not so primitive. The system, which generates the symbol timing error, is called as Timing Error Detector (TED). Choice of a proper TED algorithm is a crucial point of timing synchronizer design. Above all, it depends on the modulation constellation, pulse shaping and the expected signal-to-noise ratio. The best results are reached by the application of maximum-likelihood (ML) criterion. However, the delay (or symbol timing error) determination optimally (using ML) requires knowledge of all incoming signal (past and future). The suboptimal solution is computed from basic ML-structure and usually needs two last consecutive samples.

![Fig. 1. Flow diagram of the feedback timing synchronizer.](image)

Mathematical operations for obtaining ML-based equations for TED have been derived completely in the source [1]. There is shown a derivation of general ML formula for timing error estimation using log-likelihood function. The timing error signal for n-th term is given by equation:

$$e_n = \hat{e}_n - \hat{e}_n' + \sum_{m=-\infty}^{\infty} \hat{c}_m h(n-m)T_s$$

(2)

where $\hat{c}_m$ determines the sequence of estimated data, $y'_n$ is receiving signal filtered by matched filter, $T_s$ is symbol period, $\hat{e}_n$ is estimation of symbol timing shift, and $h(\bullet)$ is impulse characteristics of symbol, respectively.
total shaping of every symbols over transmission path. 

This formula for derivation of symbol timing error has two drawbacks. The first is a requirement of infinite sum, which is impossible to realize. The second problem is that, timing error involves data decisions which extend into the future. In practice, the marked simplification of this formula is usually applied and then such TEDs represent suboptimal solutions known as ad-hoc error detectors. Representative suboptimal TEDs are Zero-Crossing Detector (ZCD), whereas the error signal is defined by the following equation:

\[ e_1(n) = (\hat{c}_{n+1} - \hat{c}_n) y_s \left( nT_s - \frac{T_c}{2} + \hat{r}_{n+1} \right) \],

(3)

and well-known Early-Late Detector (ELD):

\[ e_2(n) = \hat{c}_n \left( y_s \left( nT_s + \frac{T_c}{2} + \hat{r}_n \right) - y_s \left( nT_s - \frac{T_c}{2} + \hat{r}_{n+1} \right) \right) \].

(4)

These algorithms can be successfully applied for linear modulations and implemented in the DSP system immediately. In [1] are shown characteristics of these two algorithms determined by the variance of timing error for specific initial conditions - the objective evaluation of the detection capability requires precise definition of input signal parameters include modulation scheme, characteristics of transmission channel, parameters of the shaping filter, range of normalized signal-to-noise ratio in the detector input etc. The variance of error quantity is the best quality index to achieving the minimal bit error ratio (BER) of the detector under test [1]. Numerous tests of ZCD and ELD for PSK modulations shown that the ZDC return less variance than ELD.

In the figure 2, the variances of timing error are presented for BPSK signals with the general raised-cosine pulse shaping and additive white Gaussian noise AWGN. This configuration is the most widespread in practice. All simulations have assumed an application of the first order digital delay loop with the normalized noise bandwidth \( B_{LN}=0.01 \). The input signal is generated by the maximum length sequence MLS, which warrants equal data probability, which is often solved by an appropriate source encoding. Simulations are performed for the chosen values of roll-off factor \( \alpha \) and for the normalized signal-to-noise ratio in the range \( \gamma \in <0; 30> \text{ dB} \). The absolute timing error is converted into normalized delay expressed by:

\[ \delta_n = \hat{r}_n / T_s \].

(5)

The influence of the roll-off-factor on the variance of normalized delay is considerable and depends on the applied type of error detector. The variance of delay is growing for the small roll-off-factor values in ZCD application. This effect is obvious for high values of the normalized signal-to-noise ratio. The same effect gives ELD. Cause of this phenomenon is the soft falling of shaping impulse for low values of roll-off-factor.

3 Augmentation of Zero Cross Detector

In general communication systems, the roll-off-factor is set in range 0.3 – 0.5, and ZCD mentioned above has not good characteristics for these values. An added error in timing error computation by ZCD is caused by leaving out the infinite sum in exact ML derivation (2) from the equation (3) for ad hoc ZCD. This component is more significant for small roll-of-factors and source of this phenomenon is explained in the figure 3.

Every symbol in transmitted message is formed by shaping filters (matching filtering) generally with infinite impulse response and affect signal in other symbol time intervals (figures 3 a to d). The basic feature of general shaping filters is an elimination of this influence at the optimal sampling time for data decision from receiving symbol. These filters fulfill a condition of zero inter-symbol interference ISI. But outside of optimal decision time the symbols interact and implicate an operation of timing synchronizer. Procedure of ZCD is based on evaluation of signal error in time by its theoretical passing through zero level between two different symbols (before and after zero level passing) as figure 3e shows (perfect zero crossing). Other symbols bring into computation an additional error (figure 3f).

Limitation of this effect can be achieved by subtraction a theoretical level of other symbols in optimum passing time, as it is evident in equation (2).
Fig. 3. Shapes of raised-cosine pulses ($\alpha=0.01$): a)-d) separate pulses for symbol sequence -1, +1, +1, -1; e) component sum for neighbouring symbols between timing error decision (c+d); f) component sum for all symbols of sequence (a+b+c+d) and resulting zero crossing error.

However in practical DSP system, the set of this subtraction have to be restricted to number of the nearest symbols and then equation (2) can be rearranged to form:

$$e_T(n) = \hat{c}_n \left[ y_n(nT_s + \hat{t}_n) - \sum_{m=n-d}^{n+d} \hat{c}_m h^{(n-m)}(T_s) \right]. \tag{6}$$

Parameter $d$ can be specified as processing depth reflecting number of shaped symbols which are taken into symbol timing error computation from left (before current symbol) and right (after current symbol) side. It is possible to describe augmented ZCD (AZCD) structure, which is derived from definition (6), by following formula:

$$e_T(n) = (\hat{c}_{n+1} - \hat{c}_{n+1}) \left[ y_n(nT_s + \hat{t}_n) - \sum_{m=n-d}^{n+d} \hat{c}_m h^{(n-m)}(T_s) - \sum_{m=n+1}^{n+d} \hat{c}_m h^{(n-m)}(T_s) \right], \tag{7}$$

where depth parameter is 2, 3, 4 or more. The most frequently applied raised-cosine pulse shaping is defined by response:

$$h(t) = \frac{\sin \left( \frac{t}{T_s} \right)}{T_s} \cos \left( \alpha \cdot \pi \cdot \frac{t}{T_s} \right) \left( 1 - \frac{2\alpha \cdot \pi \cdot t}{T_s} \right)^2, \tag{8}$$

where $\alpha$ is represent roll-off-factor as communication system parameter.
AZCD defined by equation (7) was tested for BPSK signal shaped by raised-cosine pulse with various roll-off-factor and a few processing depths. Resulting characteristics of variances of timing error are presented in the figure 4 as function of and additive white Gaussian noise AWGN. All simulations have assumed the same conditions as example in figure 2, it means, that the first order digital delay loop with the normalized noise bandwidth $B_{LN}=0.01$ and the same MLS sequence was applied. A positive impact of augmentation of ZCD algorithm to reducing the added error for estimation of timing error due to pulse shaping is confirmed by comparing of simulation results. An application of AZCD with processing depth $d=2$ brings significant limitation of added error for roll-off-factor $\alpha>0.4$. AZCD with processing depth $d=3$ is suitable for systems with roll-off-factor about 0.3. The communication system with lower roll-off-factors needs processing depth more than 3, it is fortunately that such systems are not too used in practice.

### 3 AZCD Algorithm Implementation

In this chapter is shown a very simple implementation of AZCD algorithm in the digital radio resulting from formula (7). The terms in sums of impulse responses in equation (7) are determined for sample time (half time) between two neighboring optimal sampling points for symbol. It means that these sums depend only on decision data sequence and impulse response (for RC filtering it depends on roll-off-factor). Values of RC impulse response for required sampling times and selected roll-off-factors obtaining from equation (8) are presented in the table 1. Because the impulse responses of shaping filters are symmetrical, the same values are defined for negative time. Sums of these components for all variations of data sequences imagine the wanted sums in formula (7) and they can be saved in simple look-up table. Then the current data sequence generates an address for this look-up table and output specified resulting sum of added error due to pulse shaping. This value is after used to elimination of added error in subtraction operator. Resulting structure for AZCD timing error generator is shown in the figure 4.

<table>
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<tr>
<th>$\alpha$</th>
<th>Sampling time</th>
<th>1.5-$T_s$</th>
<th>2.5-$T_s$</th>
<th>3.5-$T_s$</th>
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<td>-0.080977</td>
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<td>-0.015316</td>
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</table>

Fig. 4. Flow diagram of augmented ZCD with processing depth $d=4$.

### 4 Conclusion

An impact of pulse shaping of symbol on zero crossing timing error detector is shown in this paper. Result of this is the undesirable added error and degradation of timing error characteristics. This problem can be successfully eliminated by an application of augmented ZCD, which is presented in results of simulations. There is performed a solution for BPSK signal filtered by RC shaping filter in AWGN channel. It is possible to state, that this method can bring a good effect for other types of signals. In the last chapter is shown that an implementation of AZCD in DSP system can be quite simple.

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**References:**


