A 0.18\(\mu \)m 3GHz True Single Phase Clocking Divider-by-3 Circuit

MASAYUKI IKEBE, JUNICHI MOTOHISA, and EIICHI SANO
Hokkaido University, Graduate School of Information Science and Technology
Kita-ku, Kita 14, Nishi 9, Sapporo JAPAN
and
Hokkaido University, Research Center For Integrated Quantum Electronics
Kita-ku, Kita 13, Nishi 8, Sapporo JAPAN

Abstract: We evaluated the use of a true single phase clocking (TSPC) circuit as a high-frequency divider-by-3 circuit. This divider consists of two TSPC D-flip-flops (D-FFs) with NOR gate logic circuitry. To achieve high-speed operations as well as downsizing the circuit, the NOR functions are implemented into the TSPC D-FF. We designed the divider using a 0.18-\(\mu \)m RF CMOS process; the circuit is 100 \(\times\) 200 \(\mu \)m\(^2\). In the measurements, we confirmed the frequency divided by 3 at less than 3.14 GHz clock with 2.34 W.

Key–Words: SCL, TSPC, High frequency divider, Divider-by-3 circuit, High speed operation.

1 Introduction

The field of broadband communications has been rapidly expanding as the information society continues to grow. Relatively large amounts of data can now be handled with ease, and the exchange of image and music data is commonplace. In both wired and wireless communications, synchronous technology is indispensable, and this technology is used on various levels, such as the protocol and circuit levels. A divider generates a fraction of the reference frequency, and is used for a clock generator, a frequency synthesizer, and other operations.

An ordinary high frequency divider in a CMOS process consists of source coupled logic- (SCL-)[1] D-flip-flops (D-FFs). Since the SCL uses a differential operation, this circuit can perform high-speed operations at low amplitudes (Fig. 1). However, for a divider-by-2 circuit, a D-FF with two SCL circuits is required[2]. Moreover, the circuit configuration of the divider-by-3 circuit needs two D-FFs and additional logic circuits. Therefore, it has been difficult to produce a high frequency divider with a small circuit composition.

To overcome this problem, we propose new circuitry for high frequency division by 3 that has a TSPC architecture that can be used for various applications.

2 True Single Phase Clocking divider

2.1 Operation of TSPC logic circuit

A TSPC logic circuit alternately generates \( Data \)-through state [\( L \)and\( H \)] Hold state \( Data \) operations by switching between CMOS devices. Like a dynamic logic circuit that alternately performs \( \phi \) Pre-charge \( \phi \) Evaluate \( \phi \) operations in parasitic capacitance, the TSPC circuit operates a data fetch by using the pre-charge and data hold performed by the high impedance switching at the clock-signal timing[3, 4].

Figure 2 shows the D-FF operation of a TSPC circuit. When \( \phi = L \), the parasitic capacitance of the input part is pre-charged along with the \( Data[t+1] \).
2.2 TSPC divider-by-3 circuit

The proposed divider-by-3 circuit consists of sequential circuits based on the TSPC D-FFs and 2-AND gate logic. Figure 3 shows the proposed circuit and its truth table.

This circuit achieves frequency division by using logic operations. By AND logic, when only \( Q1[t] = 1 \) and \( Q2[t] = 0 \), \( Q2[t + 1] \) becomes “1”. In other condition, \( Q2[t + 1] \) becomes “0”. Therefore the circuit as shown in Fig. 3 performs frequency dividing by 3.

In the circuit configuration, the cascade connection between the D-FF and the AND gate degrades the frequency characteristic by adding additional delay to the circuitry. Therefore, the NOR function was implemented into the TSPC D-FF without using the optional AND gate circuit. A differential output is achieved by using an additional inverter.

3 Circuit Design and its Simulation

We designed the divider by using a 0.18-\( \mu \)m mixed signal/RF CMOS process with one poly and six metal layers. In this design, the output-impedance matching was not set to 50 \( \Omega \) terminated, because we assume that the next stage circuit is a conventional logic circuit that has a high input impedance. The ratio of the size of the p- and n-MOSFET was set to 3:1 due to the mobility of the MOSFETs, but the actual sizes were determined by the operating frequency. By the MOSFETs size of the additional output inverter, we control the signal duty.

Figure 4 shows the size depending on the operating frequency. The power dissipation for a 3-GHz operation was 2.7 mW under typical conditions. We confirmed that we could convert the frequency from 3 GHz into 1 GHz. The result of transition simulation is shown in Fig. 5.

Based on the measurement setup, we also include the result for 50 \( \Omega \) terminated configuration. We were able to confirm division operations up to 3.6 GHz using our design by conducting circuit simulations under typical conditions. Figure 6 shows the layout of the circuit When compared to a standard SCL configuration, we decreased the circuit area by 50% using the SCL D-FF basis. Our circuit was \( 100 \times 120 \mu m^2 \).

4 Measurement result

Figure 7 shows the measurement setup. One of the fabricated chips was placed on a probe station. The transition characteristic was measured with an oscilloscope. The signal generator port was connected to the divider input.

In this measurement, an input signal with 7 dBm was applied to the divider through a cable with 50 - \( \Omega \) characteristic-impedance configuration. The measured results are shown in Fig. 8 and 9. We confirmed the operation of dividing by 3 at less than 3.14 GHz with 2.34-mW. Moreover, when supply voltage VDD
Figure 3: TSPC-divider-by-3 circuit.

5 Conclusion

We designed a high-frequency-TSPC divider-by-3 circuit. This divider, which has two TSPC D-FFs, converted a 3-GHz reference signal into a 1 GHz one with only a 2.7 mW. The circuit was 100 $\times$ 120 $\mu$m$^2$ and was constructed using a 0.18-$\mu$m mixed signal/RF CMOS process. We fabricated and measured the designed divider. A 3-GHz operation of dividing by 3 with 2.34 mW was confirmed by measurement.

Acknowledgements: This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc. and Agilent Technologies Japan, Ltd.

References:


Figure 5: Transition simulation results.

(a) Open

(b) 50 Ω terminated.

Figure 6: Layout of proposed divider.

Figure 7: Measurement setup.

Figure 8: Measurement results of proposed circuit.

Figure 9: Maximum Operating frequency vs. supply voltage for current dissipation.