A high-speed voltage-follower based on a global feedback technique

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Abstract: This paper presents a novel voltage-follower, implemented in bipolar technology, based on a global feedback technique. The evaluation of the circuit has been carried out using extra fast complimentary transistors and the biasing circuitry followed the same design philosophy. The proposed design exhibits very high input and very low output impedance, due to the feedback technique, for operating frequencies beyond 1GHz. The small-signal bandwidth achieved is higher than 3GHz, the output voltage swing is some ±3.2V, the offset voltage is around 200uV while the input offset current is just above 130nA. The new circuit achieved gain flatness to within 0.1dB up to 170MHz, featuring total harmonic distortion better than -65dB and intermodulation distortion of around -70dB, for capacitive loads up to 10pF. The operation of the novel design is specified from -20°C to +100°C and the power dissipation is some 52mW on a ±5V power supply.

Key-Words: Voltage-follower, buffer, low-distortion, global feedback

1 Introduction

The exponential growth of high frequency applications increased the need for more sophisticated circuit design. In order to achieve a satisfactory overall circuit performance high frequency front-end stages have to be used, to avoid limitations of the system. In addition, the interconnection of several high voltage gain stages with high dynamic output impedance introduces low frequency poles in the system, especially on capacitive loads. Besides, several typical applications such as high-speed analog signal multiplexers, RGB driving stages and LCD displays require special circuitry for isolation and bandwidth [1].

The ideal voltage follower presents an infinite input and zero output impedance and re-produces the input signal in the output irrespective of loading and operating conditions [2]. In practice, the increased output impedance, the instability and distortion as well as the gain variation limit the performance of such configurations. The circuit proposed in this paper, and thought to be novel, combines low distortion and good isolation with relatively simple architecture.

2 Circuit Description

The starting point of the proposed voltage-follower is shown in Fig.1. A single stage, long-tailed pair amplifier is followed by an emitter-follower which provides the required feedback [3-4].

Fig.1 Core circuit of the proposed follower, labeled for a DC analysis
Straightforward circuit analysis according to the relevant voltage and currents shown above for the DC analysis, gives

\[ I_{B3} < \frac{2I_O}{(1+\beta)} + \frac{I_O}{(1+\beta)} + \frac{V_O}{(1+\beta)R_L} \approx \frac{I_O}{(1+\beta)} \]  \hspace{1cm} (1)

\[ I_{C2} = I_O - \frac{I_O}{(1+\beta)} = \alpha I_O \]  \hspace{1cm} (2)

and

\[ I_{E2} = \frac{1}{\alpha} (\alpha I_O) = I_O \]  \hspace{1cm} (3)

Since, \( I_{E1} = I_O \) and \( I_{C1} = \alpha I_O \)

\[ I_{C1} = I_{C2} \]

However

\[ V_{OS} = V_{BE1} - V_{BE2} = V_T \log_e \frac{I_{C1}}{I_{C2}} \]  \hspace{1cm} (4)

Hence

\[ V_{OS} = 0 \]

From standard feedback theory [5] the low frequency gain \( G(0) \) of the feedback amplifier is given by

\[ G(0) = \frac{A(0)}{[1 + A(0)]} \approx 1 \]  \hspace{1cm} (5)

The input \( R_{if} \) and output \( R_{of} \) resistances with feedback, in terms of the input and output resistances without feedback, are given as

\[ R_{if} = R_i [1 + A(0)] >> R_i \]  \hspace{1cm} (6)

\[ R_{of} = R_o \sqrt{[1 + A(0)]} << R_o \]  \hspace{1cm} (7)

The circuit of Fig.1 is not, as it stands, suitable for handling fast negative-going pulse edges, similarly to a simple emitter-follower. This limitation is overcome in the proposed circuit.

3 The proposed configuration

The complete circuit of the proposed design is shown in Fig.2. The biasing scheme for both source and sink is the “6-pack”, used in several recent designs [6-8]. Comparing Fig.1 with Fig.2, Q6 and Q9 are added to provide suitable biasing for the complementary output stage. With \( V_S = 0 \) negative feedback ensures that \( V_O \approx 0 \), provided the transistors operate in the forward-active mode, with the DC current distribution shown. Now if \( V_O = 0 \), then the base of Q5 is 2\( V_{BE} \) above earth potential. The inclusion of the diode-strapped transistor Q3 and Q4 ensures that the collector voltage of Q2 is zero. Connecting the collector of Q1 to the output terminal makes the collector voltage of Q1 zero, too. Q7 and Q8 are connected in parallel so that their base-emitter voltage is the same as the other transistors and each has a collector current of 1mA. The connections, indicated, provide bootstrapping for the collector of both Q1 and Q2, with the intention of providing increased input impedance.
The proposed circuit was simulated with $V_S = 0$ to check the DC conditions. However the output revealed the presence of sustained sinusoidal oscillations occurring at a frequency of approximately 4.2GHz. Thus, the loop-gain magnitude and the loop-gain phase investigated. The result is shown in Fig.3. It is clear that $|L_G| = 2.77$dB (i.e., $> 0$dB) when $\angle L_G = 0^\circ$, at $f = 4.46$GHz.

To achieve stability the ‘dominant-pole’ approach was adopted [9]. A small capacitor $C_1$ was connected to the collector of Q25 as shown in Fig.2 since this point has a comparatively high incremental resistance associated with it. $C_1$ has the effect of reducing the bandwidth with the result that $|L_G| < 0$dB when $\angle L_G = 0^\circ$. Trial and error revealed that $C_1 = 0.2\mu F$ was just enough to achieve a gain and phase margin that would not only take account of circuit tolerances but also to provide acceptable peaking in the frequency response of the closed-loop gain, a value of $0.35\mu F$ was decided on. This provides a gain margin of $2.26$dB.

A higher gain margin could be achieved with a larger value of $C_1$ but that would be at the expense of closed-loop bandwidth and chip area.

3.1 DC conditions of the proposed design

The simulated transfer characteristic of the new circuit, shown in Fig.4, has good linearity and unity slope, a consequence of the overall feedback [10]. The enlarged plot of Fig.4 in the vicinity of the origin, shown in Fig.5, confirms the existence of a very small offset voltage, for reasons described in the initial schematic.

![Fig.4 Simulated transfer characteristic of the VF](image)

![Fig.5 Expanded view of the transfer characteristic in the vicinity of the origin](image)
The quiescent power dissipation produced from the simulation of the circuit was 51.6mW at room temperature, in good agreement with the theory.

3.2 Small-signal voltage-gain
Fig.6 shows the frequency response of the proposed circuit. Compared to conventional followers it presents considerably reduced peaking, due to the feedback loop and the stability that the negative feedback offers.

![Frequency response for the small-signal gain](image)

Fig.6 Frequency response for the small-signal gain $|\xi|$ of the proposed circuit with different loads

3.3 Incremental input impedance
The incremental input impedance as a function of frequency is shown in Fig.7. Spot values are shown in Table 1. The high input impedance results from the bootstrapping of the collector of $Q_1$.

![Bode plots for $|Z_{in}|$](image)

Fig.7 Bode plots for $|Z_{in}|$ for several loads and input phase

| Conditions | $|Z_{in}|$ (Ω) |
|------------|--------------|
| Operating temp. (°C) | -20 | 27 | 100 | -20 | 27 | 100 |
| Freq. 312.5KHz | 10.2M | 15.5M | 25.9M | 9.8M | 15.1M | 25.3M |
| Freq. 31.25MHz | 309K | 401K | 552K | 307K | 398K | 549K |
| Freq. 250MHz | 38.6K | 49.3K | 66.5K | 38.4K | 49.2K | 66.4K |
| Output load | $R_L = \infty$ | $R_L = 5\Omega$ |

Table 1 $|Z_{in}|$ of the VF with $R_L = \infty$ and $R_L = 5\Omega$, as a function of $f$ and $T$

3.4 Incremental output impedance
The approach presented here, to calculate the incremental output impedance of the circuit, is based on a general property of linear voltage amplifier circuits. If the output is incrementally short-circuited, $V_O = 0$ and $i_O = i_{SC}$.

Hence

$$ GV_S = i_{SC}r_O$$

By inspection in Fig.2, looking into the base of $Q_5$, the incremental resistance is

$$ R_{BS} = r_{X5} + r_{XS} + \left[ (\beta_5 + 1) \left( \frac{r_{XX} + r_{XX}}{2} \right) / r_{O5} \right] $$

where $r_X$, with appropriate second subscript, represents the transistor base bulk resistance.

Straightforward calculations according to the operating conditions, gives

$$ r_O = \frac{V_S}{i_{SC}} - \frac{V_S}{i_{BS}(\beta_5 + 1)\beta_7 + 1} = 31.3m\Omega $$

Fig.8 shows $|Z_o|$ and $\angle Z_o$ as a function of frequency for three different operating temperatures. Spot values for $|Z_o|$ as a function of $f$ and $T$ are shown in Table 2. The difference between theoretical and simulated value is accounted for the extra components of $i_{SC}$ that have been ignored. These are the current flowing to the collector of $Q1$ and the current reaching the output via the base of $Q1$ and $Q2$. In connection with the emitter-follower outputs, $Z_o$ is inductive at high frequencies.
3.5 Total harmonic and intermodulation distortion

Tables 3 and 4 show, respectively, THD under specified conditions at 31.25MHz and 250MHz. The performance of the circuit at higher frequencies deteriorates mainly due to the compensation capacitor and the collector current of the output transistor. Table 5 shows the IMD performance results for the proposed circuit, as a function of operating frequency and temperature.

### Table 3 THD of the new circuit at 31.25MHz

<table>
<thead>
<tr>
<th>Conditions</th>
<th>THD (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temp. (°C)</td>
<td>-20° 27 100</td>
</tr>
<tr>
<td>Freq. 31.25MHz</td>
<td>49m 36m 29m</td>
</tr>
<tr>
<td>Freq. 31.25MHz</td>
<td>130m 131m 133m</td>
</tr>
<tr>
<td>Freq. 250MHz</td>
<td>923m 990m 1130m</td>
</tr>
</tbody>
</table>

### Table 4 THD of the new circuit at 250MHz

<table>
<thead>
<tr>
<th>Conditions</th>
<th>THD (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temp. (°C)</td>
<td>-20° 27 100</td>
</tr>
<tr>
<td>Freq. 31.25MHz</td>
<td>-87.1 -87.5 -88.9</td>
</tr>
<tr>
<td>Freq. 250MHz</td>
<td>-57.7 -58.3 -61.2</td>
</tr>
</tbody>
</table>

### Table 5 IMD of the new circuit as a function of f and T

#### 3.6 Pulse response

An approximate analysis of the transient response of the voltage follower has been carried out using the charge-control approach pioneered by Beaufoy and Sparks [11]. According to that the Slew Rate, which determines the maximum sinusoidal output voltage at a given frequency, is limited by the product $C_k r_e$ or the ratio $I_o / C_L$, where

$$\left(\frac{C_L}{\beta+\mu} \right) = C_k,$$

whichever give the greater value for rise and fall times for $u_o$.

To proceed further it is necessary to decide on the nature of input signal, $u_i$. In case it has the form of a truncated ramp voltage, as shown in Fig.9, the component parts of the leading edge will the similar to that shown in Fig.10.

Accurate prediction of rise and fall times and current maximum amplitudes is not simple. In practice, it is necessary to ensure from the
simulation plots that the transistor does not exceed its $i_{C_{\text{max}}}$ and $P_{C_{\text{max}}}$ in the event of small values of $t_r, t_f$ and large values of $C_L$.

Fig.9 Assumed input voltage signal

$$u_b = \frac{V_B}{t_r} t$$

$$u_b = U(t-t_r) \frac{V_B}{t_r} (t-t_r)$$

Fig.10 Components of the leading edge

Fig.11 shows the waveforms when a positive going input pulse of amplitude 1V and rise and fall times of 1nS is applied.

Fig.11 Pulse response for an input signal with 1nS rise and fall times

4 Conclusion

A voltage-follower for high frequency applications has been presented. The circuit was simulated using Analog Devices’ extra fast complementary transistors, with 1mA operating current and ±5V power supply. The new voltage-follower is using overall feedback in addition to local feedback which is lay to a number of improvements in the VF performance, notably with respect to input and output impedance, offset voltage and pulse response. In addition it combines good distortion levels with wide linear operating range. The price to be paid for this is a relatively restricted operating bandwidth due to the added capacitor which ensures Nyquist stability. This research work is still ongoing and the circuit performance is being evaluated for operation at reduced power supply values. Initial results suggest that the performance is not significantly degraded when used with ±3.3V power supplies.

References: