Abstract — in the brief, a programmable phase-locked loop (PLL) based ISM band fractional-N frequency synthesizer commonly used in wireless communication system is presented. The third order error-feedback Sigma-Delta modulator and high linearity PFD / Charge Pump are adopted to reduce close-in phase noise due to $\Sigma\Delta$ quantization noise folding. Automatic calibration technique is also introduced to adjust the nominal frequency of voltage controlled oscillator (VCO) through PVT variation. The Synthesizer is designed in UMC .18um RF process and has a die size of 1.5mm*2.3mm. The measured phase noise is -112 dBc/Hz at 1 MHz offset.

Keywords— Fractional –N Frequency Synthesizer, Delta-Sigma Modulation, Quantization noise folding, automatic calibration technique

INTRODUCTION

The recent boom in the wireless telecommunication systems has resulted in great demand in high performance, low cost RF front end [1]-[3]. Frequency synthesizer is a phase-locked loop (PLL) circuit that locks the clock from the feedback divider with the reference clock [4]. In the wireless RF transceiver, frequency synthesizer affords a stable RF frequency to up/down convert the modulated signals in the transmit/received path by Mixer [5] [6]. The frequency synthesizer can be either an integer-N or fractional-N PLL [7]. The Integer-N frequency synthesizer suffers from trade off between fast dynamics and high frequency resolution. In a fractional-N frequency synthesizer, the frequency divider averages many integer divider cycles over time to get an effective fractional divider ratio. A simple accumulator with an overflow can be used as a fractional modulator, but this method generates periodic fixed tone. $\Sigma\Delta$ modulation is adopted to get the fractional number while shaping the quantization noise to high frequency band. Then the quantization noise is filtered by the low-pass response of frequency synthesizer [8] [9]. $\Sigma\Delta$ frequency synthesizer can achieve fast loop dynamics and high frequency resolution with high reference frequency.

A high level block diagram of the implement PLL is shown in Fig.1. The details of the PLL are described throughout the remainder of the paper. Section II describes Voltage Controlled Oscillator (VCO), third order error-feedback sigma-delta modulator, and PFD/CP linearization technique and automatic calibration technique respectively. Section III presents the measured results.

II. SYNTHESIZER ARCHITECTURE AND CIRCUIT DESIGN

A. VCO

Fig.1 shows a schematic of the LC VCO, which is based on pMOS and nMOS cross-coupled pairs with an LC resonant tank
[1][10]. Combination of cross-coupled NMOS and PMOS transistors is utilized to cancel out the loss of the LC tank.

The LC tank consists of an on-chip spiral inductor with patterned ground shield as well as diode varactors implemented with p+ diffusion in N-well. And a 16-bit digitally controlled capacitor array is parallel with the resonant tank to achieve large frequency tuning range and to overcome process variation and temperature changes. The VCO gain is 40MHz/V. The control voltage of fine varactor is tuned from 0.8V to 1.2V, and generation scheme of the controlled bits of switched capacitors is discussed in section III. To decrease phase noise due to switching activities of MIM capacitors, a thermo-decoder is added.

B. Error-feedback ΣΔ modulator

High order single bit ΣΔ modulators effectively push the quantization noise to high frequency offset, but suffer the stability problem. MASH 1-1-1 stables over the whole input range, but the output integer stream vary over a wide range to incur quantization noise folding due to PFD/CP nonlinearity [5][8]. The error feedback sigma delta modulator modifies the Butterworth filter in the feedback path to restrain high frequency noise, and still stables over the whole input range, which is shown in Fig.3.

The feedback filter transfer function is

\[
H(\nu) = \frac{3\nu^{-1}(1-0.5\nu^{-1})(1-\frac{4}{3}\nu^{-1} + \frac{2}{3}\nu^{-2})}{1-\nu^{-1} + 0.5\nu^{-2}}
\] (1)

Compared to MASH modulator, the error-feedback modulator has less high frequency noise, and the simulated quantization noise PSD is shown in Fig.4.
noise to fold back to low frequency offset to increase in band noise floor. In this design, an offset tri-state PFD [11], shown in Fig.5, is used to achieve only the up current branch in charge pump switching on/off when PLL is in lock condition. A source degenerated cascade charge pump is used to improve the output impedance to afford better up/down current matching.

![Fig.5 Offset tri-state PFD](image)

D. Self-Calibration Technique

There are two approaches to calibrate the tuning range of wideband VCO in a PLL loop operation. One approach is to program the control word externally by memory. Another approach is to adaptively change control bits by auto-calibration circuit in the PLL loop [12] [13]. In this paper, the auto-calibration technique is implemented. The auto-calibration process operates in the close-loop, which doesn’t need to open the loop. The PLL loop with auto-calibration circuit is shown in Fig.1.

As in the normal PLL locking process, PFD checks the phase difference of reference clock and clock from Multi-Mode Divider, then Charge Pump charges or discharges the loop filter to tune the control voltage of VCO. The control voltage is also fed into the calibration circuit to set the control bits of switched capacitors.

The calibration circuit consists of two comparators, a clock generation circuit, and a counter, shown in Fig.6.

The comparators determine whether the control voltage is between V_low and V_high. If not, the Up or Down Signal is assigned.

![Fig.6 Auto Calibration Circuit](image)

Fig.6 Auto Calibration Circuit

The counter is to count up or down the control bits of switched capacitors based on the Up or Down Signal. The clock generation circuit is used to generate the clock of the counter. When the loop is locked, the control voltage locates between V_low and V_high, and control bits are locked to a certain number. The locking and auto calibration process is shown in Fig.7.

![Fig.7 auto calibration process](image)

Fig.7 auto calibration process

III measured performance

A 2.4-GHz transceiver RF-end is implemented in UMC 0.18μm process, including LNA, Mixer, PA, Fractional-N frequency synthesizer and VGA. Reference clock is 10 MHz. The loop bandwidth is 250KHz to implement the in-loop GMSK modulation of 1Mbps data rate. The measured phase noise is shown in Fig.8. The prototype achieves -112dBc/Hz at 1MHz offset, -119dBc/Hz at 3MHz offset.
IV. CONCLUSION

A 2.4GHz Fractional-N frequency synthesizer with automatic calibration technique is presented. High order error-feedback sigma-delta modulator and PFD/CP linearity technique are adopted to improve the in-band phase noise performance. The prototype chip is designed in UMC18 RF process, and occupies 1.5*2.3 mm$^2$, the measured phase noise from the closed loop is -112 dBc/Hz at 1 MHz offset.

REFERENCES