The threshold voltage of MOSFET and its influence on digital circuits

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Abstract: The aim of this paper is to research the impact of physical parameters which characterize the MOSFET transistors structure on the threshold voltage value. The MOSFET threshold voltage value will have influence in behaviour of electronic device which contain MOSFET transistors. The results obtained emphasize the impact of each single physical parameter on the total value of the threshold voltage. Moreover, all of these parameters will have significant and small impact on the threshold voltage. Hence, by adjusting the values of MOSFET physical parameters the accepted threshold voltage can be achieved. As the threshold voltage will have influence on critical voltage values which characterise MOSFET digital circuits and delays during transfer logic states, it must be taken into consideration during design phase of logic gates.

Key words: threshold voltage, MOSFET parameters, enhancement-type NMOS, impurities, thickness of oxide layer, doped density, short-channel, narrow-channel, voltage level, propagation delay, output voltage level.

1 Introduction

The important value which characterizes the MOSFET transistors is the value of threshold voltage, which can be positive and negative according to the MOSFET type. This value can be controlled during the fabrication process of MOSFET transistors. The physical structure of n-channel enhancement-type MOSFET (or NMOS) is represented in Fig.1. Because the enhancement-type NMOS have advantage over other type of MOSFET transistors, in the following we will focus on this analysis. Terminals of MOSFET transistors are indicated with S (source), D (drain), G (gate) and B (body).

The value of the gate-to-source voltage V_{GS} needed to create (induced) the conducting channel (to cause surface inversion) is called the threshold voltage (V_{th} or V_t). The value of the threshold voltage is dependent from some physical parameters which characterize the MOSFET structure such as: the gate material, the thickness of oxide layer t_{ox}, substrate doping concentration (density) N_A, oxide–interface fixed charge concentration (density) N_{ox}, channel length L, channel width W and the bias voltage V_{SB} [1, 2, 5].

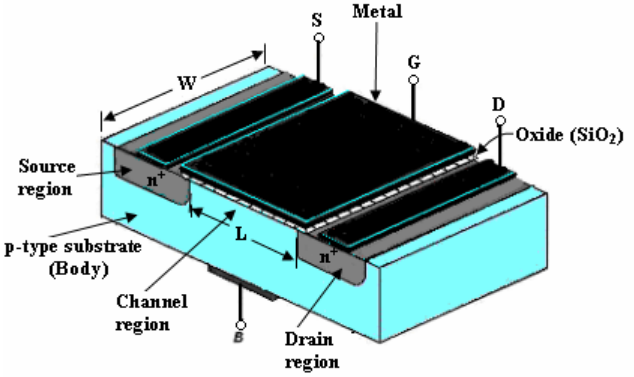


Fig.1 The physical structure of an n-channel enhancement-type MOSFET in perspective view.

2 The threshold voltage on MOSFET-transistors

2.1 The threshold voltage of NMOS-transistors with long-channel

To calculate the threshold voltage we must consider physical parameters of MOSFET structure which have the impact in value of the threshold voltage by considering the various components of V_t (when V_{SB} = 0V, the threshold voltage will indicate V_{t0}) [2]:

$$V_{t0} = \Phi_{GC} - 2\phi - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \qquad (1)$$

For nonzero substrate bias voltage ($V_{SB} > 0$), now the generalized form of threshold voltage will be [2]:

$$V_t = V_{t0} + \gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) \qquad (2)$$

where:
γ - is the body-effect parameter and
ϕ_F - is the substrate Fermi potential.

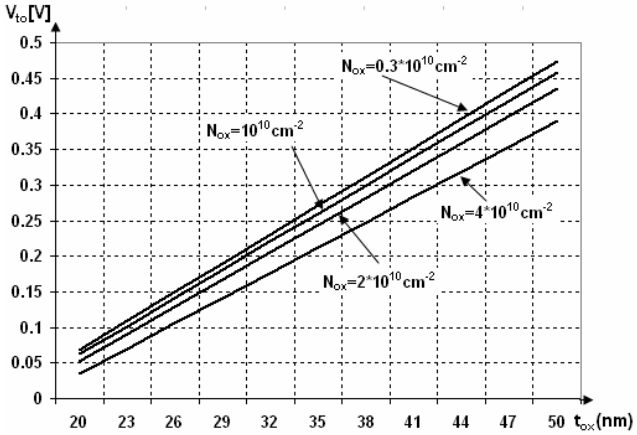


Fig.2. The dependence of the threshold voltage V_{t0} on thickness of oxide layer t_{ox} for parametric values of oxide-interface fixed charge density N_{ox}, when N_A = 10^{16} cm^{-3}.

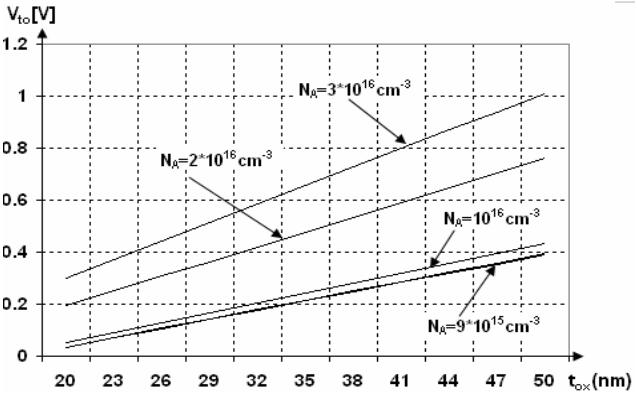


Fig.3. The dependence of the threshold voltage V_{t0} on thickness of oxide layer t_{ox} for parametric values of substrate doping density N_A, when N_{ox} = 2*10^{10} cm^{-2}.

The influence of t_{ox}, N_A and N_{ox} in values of threshold voltage is shown in Fig. 2 and Fig. 3. For larger value of each parameter: $t_{ox,}$ or N_A the value of threshold voltage will increase. But, for larger value of N_{ox} the value of threshold voltage will decrease, which is not significant.

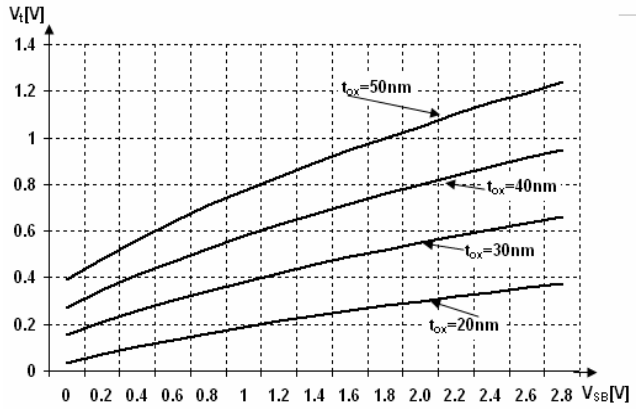


Fig.4. Variation of the threshold voltage V_t as a function of the source-to-substrate (V_{SB}) voltage for parametric values of thickness oxide layers t_{ox}, when N_A = 10^{16} cm^{-3} and N_{ox} = 4*10^{10} cm^{-2}.

Fig. 4 shows dependence of threshold voltage on the polarization voltage V_{SB}, which results in the higher values of the threshold voltage for higher value of V_{SB} compared with V_{t0} (as in case of integrated circuits).
The threshold voltage (V_t) can be adjusted by selective dopant ion implantation into the channel region of the MOSFET transistors during fabrication processes. For n-channel MOSFETs, the threshold voltage will increase by adding extra p-type impurities (acceptor ions) into the cannel region. The threshold voltage of the n-channel MOSFET can be decreased by implanting n-type impurities (dopant ions) into the channel regions. As result of the extra implanting of the type impurities, the threshold voltage will be shifted by a component (Δ_{tI}) which described:

$$\Delta V_{tI} = qN_I / C_{ox} \qquad (3)$$

where:
N_I - is density of implanted impurities into the channel region [cm^{-2}].
Now the threshold voltage will be as:

$$V_{tI} = V_t \pm |\Delta V_{tI}| \qquad (4)$$

The implanted impurities into the channel region will have an irrelevant effect on substrate Fermi potential.
Fig. 5 shows the dependence of the threshold voltage V_{t0} on extra p-type impurities which is added into the channel region.

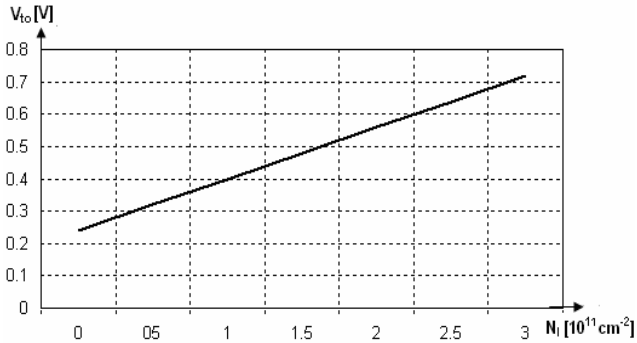


Fig.5. Variation of the threshold voltage V_t as a function of the concentration impurities N_I, when t_{ox} = 35 nm, $N_A = 10^{16}$ cm^{-3} and $N_{ox} = 4*10^{10}$ cm^{-2} and V_{SB} = 0V.

2.2 The threshold voltage of NMOS-transistors with short-channel

When NMOS is defined as a short-channel device the length of channel it will have impact on the threshold voltage. A short-channel will reduce the threshold voltage of ΔV_t compare with long-channel device [2, 5, 9].

V_{t0} (short-channel) = $V_{t0} - \Delta V_{t0}$ (5)

The amount of threshold voltage reduction ΔV_{t0} can be found as [2, 5]:

$$\Delta V_{t0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A\left|-2\phi_f\right|}\,\frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right] \quad (6)$$

where:

x_j – is junction depth of drain (source) region,

x_{dS}, x_{dD} - represent the depth of depletion regions at source and drain as results of pn junction, respectively.

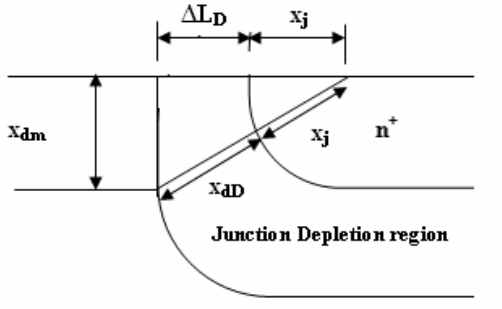


Fig.6 Simplified geometry of the MOSFET channel region. Close-up view of the drain diffusion edge.

Influence of the length channel L, the depth x_j of drain (source) regions and drain-to-source voltage (V_{DS}) on the voltage term ΔV_{t0}, are shown in Fig.7, Fig.8.

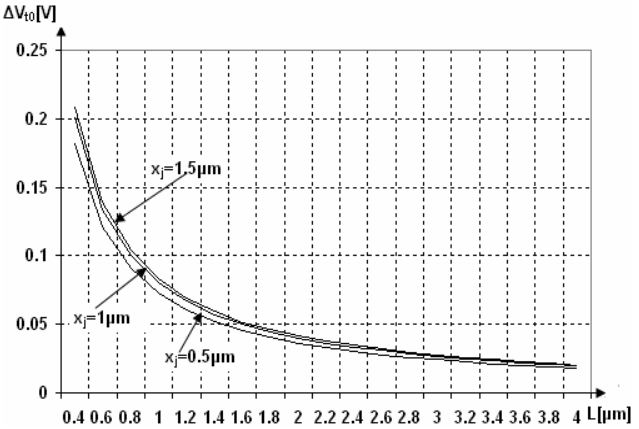


Fig.7 The dependence of the ΔV_{t0} on the length L for parametric values of depth x_j, when $N_A = 10^{16}$ cm^{-3}, $N_D = 10^{19}$ cm^{-3}, t_{ox} = 20 nm and V_{DS} = 0V.

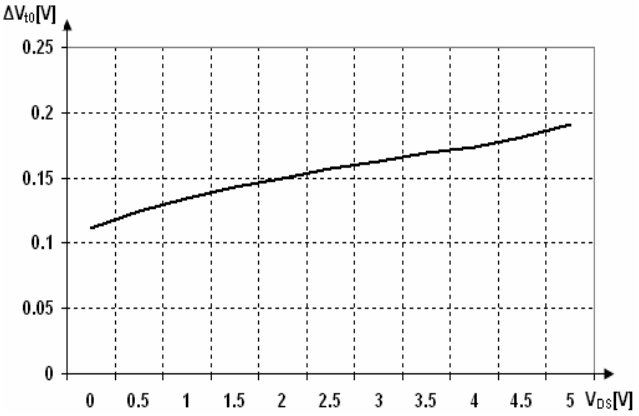


Fig.8 The dependence of ΔV_{t0} on V_{DS} voltage, when $N_A = 10^{16}$ cm^{-3}, $N_D = 10^{18}$ cm^{-3}, t_{ox} = 20 nm, x_j = 1 μm and L = 0.7 μm.

Obtained values are represented in Fig.7 and Fig.8. For $L \approx x_j$ the ΔV_{t0} will have influence in reduction of the threshold voltage V_{t0}. While if $L >> x_j$ the ΔV_{t0} is not significant, the NMOS is defined as long-channel device. The V_{DS} voltage will have significant influence in the term ΔV_{t0}, which results in larger value for higher value of V_{DS}.

2.3 The threshold voltage of NMOS with narrow-channel

When MOSFET transistor is defined as a narrow-channel device, the channel will have influence in the

threshold voltage and results in higher value for ΔV_{t0} if compared with long-channel device [1, 2, 5].

$$V_{t0(\text{narrow-channel})} = V_{t0} + \Delta V_{t0} \quad (7)$$

The voltage term ΔV_{t0} can calculate with expression:

$$\Delta V_{t0} = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{Si} N_A \left| -2\phi_f \right|} \frac{\pi \cdot x_{dm}}{2W} \quad (8)$$

In Fig.9 is shown the dependence of voltage term ΔV_t on the channel width and we can say: when $W \approx x_{dm}$ the ΔV_t term will have influence in the increase of the total threshold voltage, while $W >> x_{dm}$ the ΔV_t term is not significant.

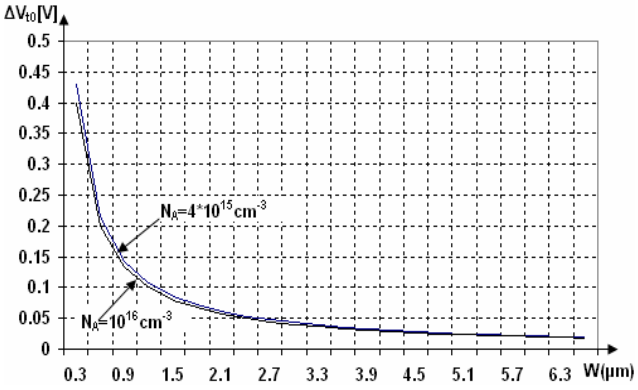


Fig.9 The dependence of ΔV_{t0} on channel width (W) for parametric values of N_A, when $N_D = 10^{18}$ cm^{-3} and t_{ox} = 20 nm.

The values obtained will help to determine the dimensions of MOS transistors and will have the approximate values of threshold voltage. The nominal value and the statistical range of the threshold voltage for any MOS process are ultimately determined by direct measurements.

2.4 Influence of threshold voltage on critical voltage values and delay in digital circuits

In many applications such as MOS inverters, pass-transistor logic circuits, dynamic pass-transistor logic circuits, semiconductor memories and other applications, the NMOS and PMOS transistors are used in order to implement switches. The threshold voltage V_t will have influence on V_{IH}, V_{IL}, V_{OL}, noise margin (NM) and propagation delay [2, 4]. In Fig.10 is illustrated the logic "1" transfer with an NMOS.

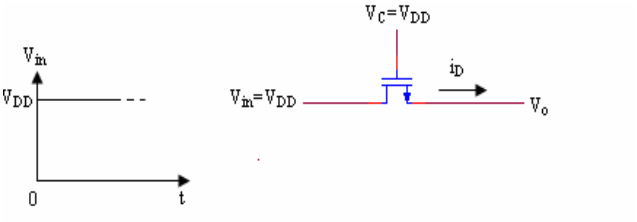


Fig.10 The logic "1" transfer with an NMOS.

After analysis we will have:

$$V_{o\max} = V_{DD} - V_t \quad (9)$$

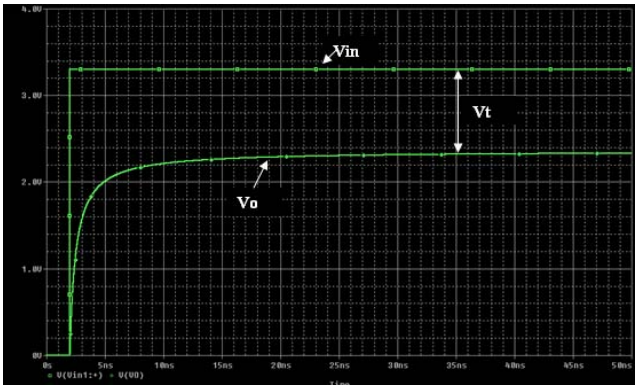
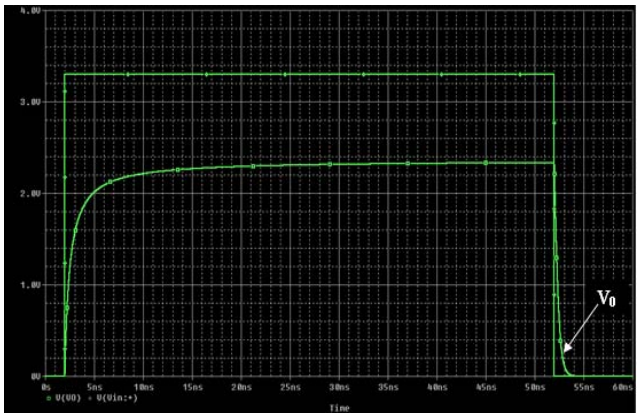


Fig.11 The reduction of output voltage level by threshold voltage, when V_{t0}=0.5V.

The fact that output voltage level will reduce based on threshold voltage, will have significant implication for circuit design. Thus the output voltage introduces the "poor 1". The threshold voltage will have influence on propagation delay (t_{PLH}), where for larger value of threshold voltage V_t the propagation delay (or time rise) will increase.

For logic "0" transfer the threshold voltage will have no influence at output voltage which represent the low voltage level (it will be V_o=0V, or "good 0"), but will have influence in propagation delay (time falls), see Fig.12. For lower value of the threshold voltage the value of propagation delay (t_{PHL}) will be lower.

Now, we will consider different case in which the output of each pass-transistor drives the gate of another pass-transistor, as depicted in Fig.14.



Fg. 12 Waveform of output voltage V_o for logic "0" transfer with one pass-transistor, when V_{t0} = 0.5 V.

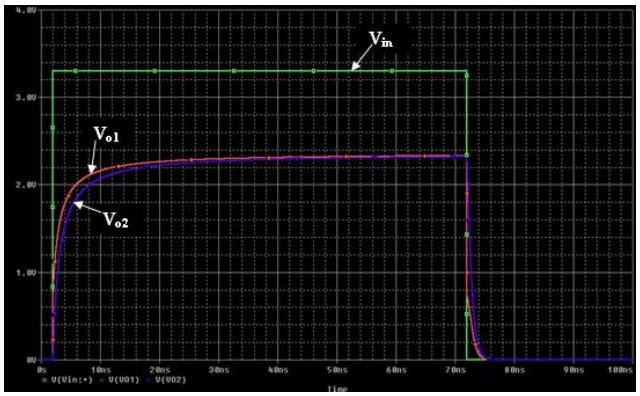


Fig. 13 Waveforms of outputs voltages when two pass-transistors connected in series. Output voltage will reduce according to V_t and propagation voltage will increase from stage to stage.

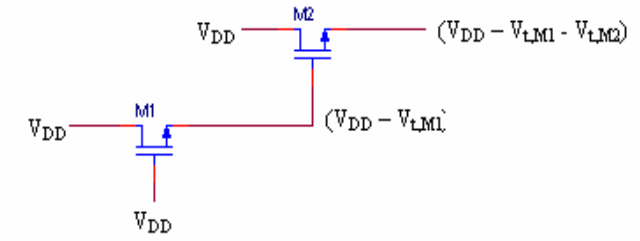


Fig.14 The logic "1" transfer when one pass-transistor is driving another pass-transistor.

After analysis, the Fig.15 shows that the output voltage level will reduce by sum of the threshold voltage of each pass-transistor.
The threshold voltage will have influence on values of critical voltages which characterize MOS inverters and voltage transfer characteristic. The impact of V_t on critical voltages for a symmetric CMOS inverters are represented in below diagrams (for supply voltage V_{DD} = 3.3 V) Fig. 16, Fig. 17, Fig.18.

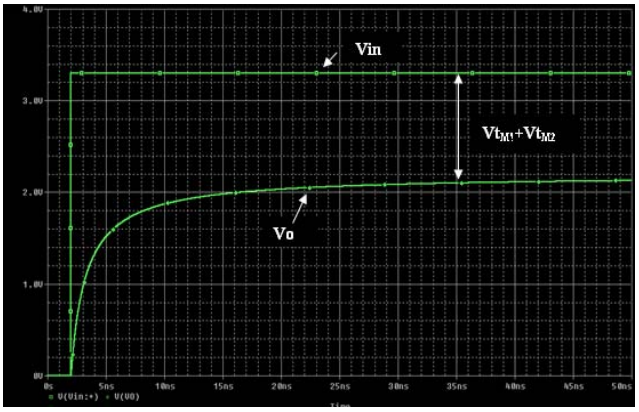


Fig.15 Waveform of output voltage V_o for logic "1" transfer, when each pass-transistor (NMOS) is driving another pass-transistor (NMOS) and V_{t0} = 0.5V.

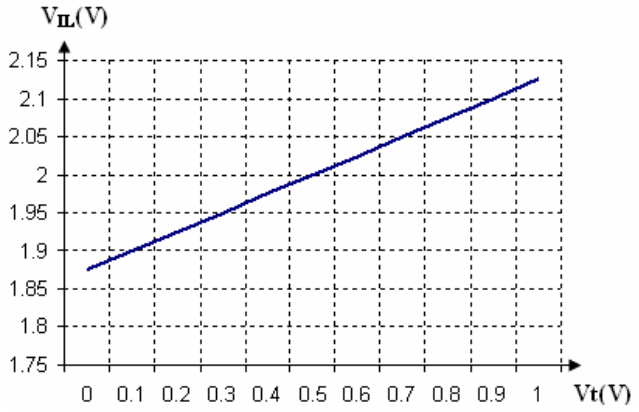


Fig.16 Variation of V_{IL} (maximum input voltage which can be interpreted as logic "0") as function of threshold voltage V_t.

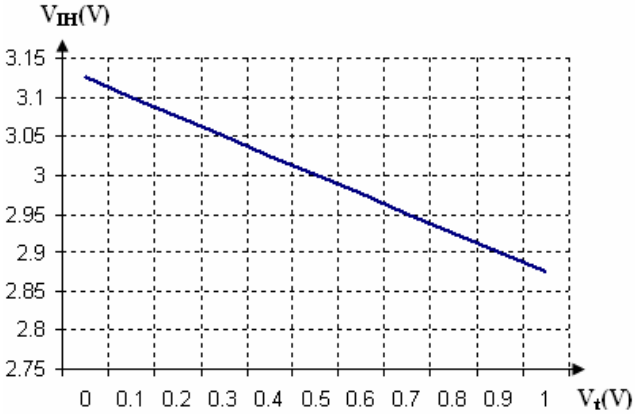


Fig. 17 Variation of V_{IH} (minimum input voltage which can be interpreted as logic "1") as function of threshold voltage V_t.

The voltage value V_{IL} will increase for higher value of threshold, while V_{IH} will decrease for higher value of threshold voltage. The noise margins (NM) for two levels will increase.

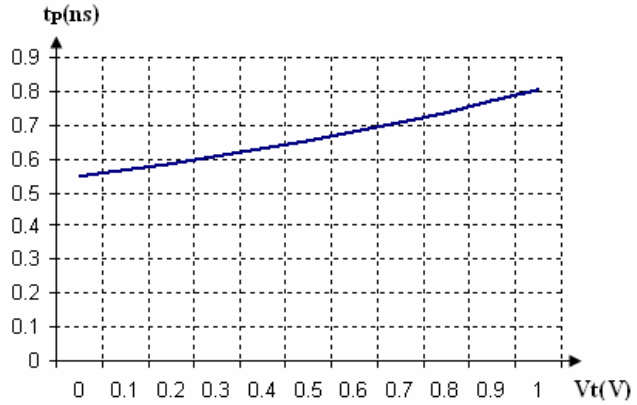


Fig. 18 Variation of propagation delay t_P as function of threshold voltage V_t.

For higher value of threshold voltage will increase of propagation delay. Moreover the threshold voltages determine minimum level of supply voltage on CMOS inverters, which will continue to operate correctly [2].

3 Conclusion

Based on the results obtained, as shown in figures (2-8), we have seen the impact of several physical parameters which characterize the MOSFET transistors (NMOS) on the threshold voltage. Therefore, it can be concluded that for long-channel device the threshold voltage will decrease when: the substrate doping (N_A) decreases, the oxide thickness (t_{ox}) decreases, the oxide-interface charge (N_{ox}) increases (but, will have little effect). For short-channel device we will have reduction of the threshold voltage by ΔV_t term compared with the long-channel device, which depends of: the length of channel (L), the junction depth (x_j), drain diffusion doping (small effect) and drain-to-source voltage (V_{DS}). For narrow-channel device the threshold voltage will increase by ΔV_t term compared with the long-channel device, which is dependent of: the width channel (W), the maximal depletion region thickness (x_{dm}). The positive source-to-substrate voltage V_{SB} (body effect, as in IC) will cause the increment on total value of threshold voltage. For MOSFETs which have a small channel length and a small channel width, the threshold voltage variations due to short- and narrow-channel effects may tend to cancel each other out. The values of the threshold voltage will have significant influence on level of critical voltages which characterise MOS inverters and propagation delay, when for higher value of threshold voltage will have better noise margin (NM) for two logic levels and propagation delays will increase. Also, in pass-transistors logic (PTL) the threshold voltage will reduce level of output voltage during the logic "1" transfer by according the V_t, the propagation delay during transfers logic states will increase for higher value of V_t.

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