Fast Transmission Mechanism of Emergency Data in AFDX Network Systems

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Abstract: - Avionics Full Duplex Switched Ethernet (AFDX) network system deployed in modern aircraft offers higher bandwidth and capability for aircraft data network. AFDX network system adopted IEEE 802.3 Ethernet technology and added some special features to compose deterministic and fault tolerant network. In AFDX network system, every application data is transferred periodically based on many features that include traffic shaping, policing and so on. Emergency data related to safety also is delivered based on traffic shaping and policing, so emergent situation cannot be reported immediately. We propose a fast transmission mechanism of emergency data in AFDX network systems for improving the rapid data delivery. In proposed scheme, emergency data needs not wait until BAG timer expires. In other words, emergency data can be transferred immediately by MAC layer of End System irrespective of allowed bandwidth and traffic policing function of intermediate switches.

Key-Words: - AFDX, Fast Transmission, ARINC664, Ethernet, Emergency data, ADN

1 Introduction

As several digital computing devices had been deployed in aircraft, needs of network system that interconnect these devices had been raised and then digital data bus was adopted.

And since high reliability is required when data is transmitted in aircraft, various fault tolerance technologies were applied to minimize or remove the loss of transferred data.

In the late 1990s, as Internet technologies like Ethernet, IP, TCP, UDP had lead data communication field, development of next-generation Aircraft Data Network (ADN) to apply low cost and higher data rate properties of these technologies to aircraft network was started. And as result, ARINC664 specification was defined [1]-[6].

ARINC664 specification adopted Full Duplex Switched (FDX) Ethernet technology and supports up to 100M bps data transmission rate [7][8].

AFDX defined in part 7 of ARINC664 specification is an Ethernet switching technology that has fault tolerance functionality using two independent physical links and scheduling mechanism to supply bandwidth-guaranteed service [4].

In this paper, we first introduce ARINC664 and AFDX specifications. And then, we propose a fast transmission mechanism that emergency data can be delivered immediately independent of allocated bandwidth.

The paper is structured as follows. In Section 2, we introduce the ARINC664 specification. Following this in Section 3 we describe the concept, functionalities and properties of AFDX technology. In Section 4, we propose a fast transmission mechanism of emergency data in AFDX network systems for improving the rapid delivery of emergency data. In Section 5, we finally provide some concluding remarks.

2 ARINC664

In the late 1990s, work started to develop a next-generation ADN based on IEEE 802.3 Ethernet technology [7].

The goal of next-generation ADN technology was to take advantage of commercial off-the-shelf (COTS) technology to minimize development time and cost, while ensuring compatibility with the need for reliable data transmission and higher data rate.

As a result, ARINC664 defined a profiled IEEE 802.3 Network using TCP/IP technology.

The ARINC664 specification is broken into several parts:

- Part1 - System Concepts and Overview
- Part2 - Ethernet Physical and Data Link Layer Specifications
- Part3 - Internet-Based Protocols and Services
- Part4 - Internet-Based Address Structures and Assigned Numbers
3 Overview of AFDX

AFDX technology composes deterministic network that supports guaranteed bandwidth and Quality of Service (QoS) based on IEEE 802.3 Ethernet technology.

The major aspects of AFDX are as follows:

- Full duplex switched network – the network is wired with a star topology and the physical interconnect medium is twisted pair, with separate pairs for transmit and receive channels. Each switch can connect up to 24 End System (ES)s. And the network operates at either 10 M bps or 100 M bps link speed.
- Redundancy – dual networks provide a higher degree of reliability than a single network scheme provides. Each ES copies a data frame and transfers original data frame and copied data frame via two independent switched networks.
- Virtual Link (VL) – the network separates a physical link into several VLs and multiplexes transferred data frames. Each VL is identified with Virtual Link Identification (VLID).
- Deterministic – the network guarantees configured bandwidth and maximum jitter per each VL.
- Profiled network – parameters for several ESes are defined in configuration tables at switches and ESes. Each ES and switch loads these configuration tables at startup and reset time to operate appropriately.

3.1 Full-duplex Switched Network

In AFDX network, up to 24 ESes can be connected to a switch with a star topology. And AFDX network offers link redundancy functionality using two independent physical links, guaranteed bandwidth and QoS functionality using traffic shaping and policing. Switches are interconnected each other and compose switched network.

3.2 Redundancy

AFDX network has two independent data path between transferring ES and receiving ES. Transferring ES generates two same frames and transfers those frames simultaneously via two separated links.

Those frames are received at receiving ES via two different paths and then receiving ES accepts valid frame that is received first and discards the frame received secondly irrespective of its validity. This operation is called as "first valid message wins" policy. To prevent duplicated reception, sequence number is inserted into MAC header of every transmitted frame.

New fault tolerant functionalities added to legacy Ethernet are as follows:

- Transmitting device – transferring ES inserts 1 byte Sequence Number (SN) in front of Frame Check Sequence (FCS) in MAC frame and transmits the frame simultaneously via two links. SN increases from 1 to 255 and wraps around from 255 to 1. SN '0' is used after reset or startup. VLID is also inserted into Destination Address (DA) field of Ethernet MAC header.
- Receiving device – following function blocks are inserted into Rx block to verify the validation of frames received via two links.
  - Integrity Checker (IC) – IC checks whether the SN value specified in received frames is equal to expected value to verify integrity of received frames. This checking process is performed simultaneously at two links. If the received SN value is not equal to expected SN value, the received frame is discarded and error counter increases.
  - Redundancy Checker (RC) – RC accepts first valid frame and discards another frame received secondly. If the interval of two frames are greater than SkewMax parameter value, RC block drops all frames and waits next valid frames.
3.3 Virtual Links
In AFDX network, each ES that uses 100M bps physical link supports multiple VLs. Such VL scheme makes it possible for several devices to share a physical link by using multiple logical links. So several devices can be interconnected by using multiple VLs. To segregate such devices each other, 2 byte VLID is assigned and up to 2^16 VLs are configurable in a physical link.
VL is a unidirectional logical link and 1 source node can have several destination nodes. Unlike legacy Ethernet switch, AFDX switch multicasts received frame to multiple destination nodes that have same VLID[8].

3.4 Guaranteed Service
The key aspects of AFDX network system is guaranteed service that ensures bandwidth and end-to-end latency. System integrator reserves bandwidth for each VL in advance and each switch monitors the data rate of Ethernet frames to prevent that total data rate exceeds link capacity (for example, 100M bps).

To offer such operation, following parameters are defined:
- Bandwidth Allocation Gap (BAG)
- jitter
- traffic shaping and policing
- allowed latency

3.4.1 Bandwidth Allocation
To allocate bandwidth of each VL, following parameters are used:
- Bandwidth Allocation Gap (BAG) - BAG is interval between two transmitted AFDX frames. BAG value can be in range 1ms to 128ms. These values should satisfy the following formula:

\[ \text{BAG} = 2^k \text{[in ms]} \times k \text{ integer in range 0 to 7}. \] (1)

- \( L_{MAX} - L_{MAX} \) is maximum byte number that can be transmitted.

![Fig. 4 Bandwidth Allocation Gap](image)

The maximum allowed bandwidth for a given VL is defined in equation (2).

\[ \text{BW}_{VL} = \frac{L_{MAX} \times B}{\text{BAG}}. \] (2)

where:
- \( \text{BW}_{VL} \) is the maximum allowed bandwidth for the VL in bps.
- \( L_{MAX} \) is the maximum allowed frame size for the VL in bytes.

3.4.2 Jitter
Jitter is variation of interval between two continuously received frames. Jitter can be occurred due to network environment. And jitter also can be occurred when an ES transmits a frame.

As shown in Fig. 5, the transferred frame experiences delay that is the interval between BAG start time and transmitting time of first bit of the frame.

The maximum allowed jitter for a given ES is defined in equation (3).

\[ \text{Max. Jitter} \leq 40 \mu s + \frac{\sum_{i=1}^{N_{VL}} (20 \text{byte} + L_{MAX}) \times i \text{bits/byte}}{N_{BW}}. \] (3)

where:
- Max. Jitter is in \( \mu s \).
- \( N_{BW} \) is the medium bandwidth in bps.
- \( L_{MAX} \) is the maximum allowed frame size for the VL in bytes.

The specification allows 40 \( \mu s \) for the maximum technological jitter, and in no case shall the total jitter be allowed to exceed 500\( \mu s \).
4 Fast Transmission Mechanism of Emergency Data

AFDX Sub Systems located in ESes generate event data and transfer it to other SSs;
Event data is stored in associated VL queue and is transmitted periodically to destination ES by regulator in MAC layer.

In emergent condition, emergency data that needs to be transmitted immediately also experiences same queuing delay based on BAG of associated VL like other common data.

Proposed scheme guarantees immediate delivery of emergency data by allowing transferring of frames irrespective of BAG value.

In AFDX network system, total delay that the frame experiences is defined in equation (4)

\[ T_{TOTAL} = T_{ES} + T_N. \]  

where:

- \( T_{TOTAL} \) is the end-to-end delay for a given frame.
- \( T_{ES} \) is delay that a frame experiences at ES.
- \( T_N \) is delay that a frame experiences in network.

The delay that a frame experiences at ES is defined in equation (5).

\[ T_{ES} = T_{es,q} + T_{jitter}. \]  

where:

- \( T_{es,q} \) is a queuing delay.
- \( T_{jitter} \) is the jitter that a frame experiences due to transmitting of other VL data.

The delay that a frame experiences in network is defined in equation (6).
\[ T_N = (T_t + T_p) + n(T_{sw,q} + T_t + T_p). \]  

where:

- \( T_t \) is a transmission delay.
- \( T_p \) is a propagation delay.
- \( T_{sw,q} \) is the delay that a frame experiences in queue of intermediate switch.
- \( n \) is the number of intermediate switches.

To simplify comparison between legacy AFDX and proposed scheme, we define some assumptions as follows:

- Process delays in devices are ignored.
- \( T_t \) and \( T_p \) is same at all links.
- \( T_{sw,q} \) is same at all switches.
- Therefore both legacy AFDX system and proposed scheme have same \( T_N \) value.
- Interval between time that a frame is inserted into queue and start time of next cycle is ignored.

In legacy AFDX network system, \( T_{jitter} \) can be in range 0 to 500µs but in proposed scheme, \( T_{jitter} \) is 0.

And in legacy AFDX network system, \( T_{es,q} \) can be in range 0 to \( BAG - 1 \), but in proposed scheme \( T_{es,q} \) is 0.

Table. 1 describes the comparison result of total delay between legacy AFDX and proposed scheme.

<table>
<thead>
<tr>
<th>BAG</th>
<th>Legacy AFDX</th>
<th>Proposed scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>2</td>
<td>1ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>4</td>
<td>3ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>8</td>
<td>7ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>16</td>
<td>15ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>32</td>
<td>31ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>64</td>
<td>63ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
<tr>
<td>128</td>
<td>127ms + 500µs + ( T_N )</td>
<td>( T_N )</td>
</tr>
</tbody>
</table>

5 Conclusion

In this paper, we introduce ARINC664 and AFDX specifications that represent next-generation ADN technology and propose fast transmission mechanism of emergency data.

And we compare the end-to-end delay of legacy AFDX network system and that of proposed scheme that an emergency data experiences.

In case of emergency data, the ES in proposed scheme does not perform common traffic shaping function but transmits data immediately.

As a result, the event subscribers that receive emergency data in proposed scheme can deal with emergent condition more rapidly.

References: