Low Power Shift Register using MTCMOS Edge-Trigger D Flip Flop Transmission Gate in Sub-threshold Region

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Abstract: - low power design is most required nowadays due to scaling down the technology where minimizing the voltage level is the most effective way to minimize the power consumption. This paper presents the design and implementation of a low power Complementary Metal Oxide Semiconductor (CMOS) ten-bit shift register by using negative latch D Flip-Flop (DFF) in the sub-threshold region with high speed in the active mode and low power consumption during the sleep mode using Multi-threshold Complementary Metal Oxide Semiconductor (MTCMOS) technique. The circuit was implemented in 90 nm from STM CMOS technology, with oxide thickness of 16Å, 250 mV power supply, 5 MHz clock frequency with 10 % activity, average power consumption is 6.43 nW and power delay product (PDP) is 24.43 aJ. The shift register has been designed and simulated by using Cadence tools.

Key-words: - leakage, low power, MTCMOS, Sub-threshold, shift register.

1 Introduction
The electronic circuit designers are worried nowadays about decreasing the total power consumption to increase the battery life time and decrease the battery’s size which is reflected on the portability of the devices like the Lap-Top computers and Cellular phone.

\[ P_{\text{dynamic}} = C \cdot V_{dd} \cdot f_{clk} \]  \hspace{1cm} (1)

It is illustrated in equation (1) that the dynamic power consumption (the consumed power during the active mode) is directly proportional to the voltage source, the load capacitance and the clock frequency. So decreasing the voltage source is one of the most effective ways to minimize the power consumption

\[ T_{pd} \propto \frac{V_{dd}}{(V_{dd} - V_{th})^2} \]  \hspace{1cm} (2)

As shown in equation (2) that the propagation delay is reciprocal proportional to the square of the difference between the voltage source and the threshold voltage of the transistor. So scaling down the voltage source without scaling down the threshold voltage decreases the difference and increases the propagation delay. So scaling down the voltage source needs to scale down the threshold voltage to keep the difference still large to minimize the propagation delay.

\[ I_{\text{leakage}} \propto e^{(V_{gs} - V_{th}) / V_{th}} \]  \hspace{1cm} (3)

The problem is that as the device threshold decreases while the leakage current increases [3], where from equation (3) the leakage current is exponential proportional to the threshold voltage, which is the current in the CMOS transistor while it is in off state due to different mechanisms which is sub-threshold current, gate leakage current, reverse-bias p-n junction current, gate-induced drain leakage (GIDL) current, and finally punch-through current. Increasing this current increases the static power consumption.

\[ P_{\text{static}} = I_{\text{leakage}} \cdot V_{dd} \]  \hspace{1cm} (4)

Equation (4) illustrates that the static power consumption (power consumed during the standby mode) is directly proportional to the multiplication of the leakage current and the voltage source. This power was neglected for the high threshold technology but for sub 100 nm, it becomes a dominant part of the total power consumption which could be even more than the dynamic power especially for the devices which are the majority of the time in the standby mode as cell phone [4].

\[ P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} \]  \hspace{1cm} (5)

Equation (5) shows that the total power is the summation of the dynamic and static power which
indicates that scaling down the voltage source leads to lower total power consumption. MTCMOS technique is one of the most effective techniques to reduce the leakage current during the standby mode by using low threshold voltage transistor in the critical paths of the circuit to improve the performance while the high threshold voltage one is in uncritical paths and is used as an isolation switch between the virtual supply lines (Vdd, GND) and the real one [3]. Section 2 presents designing the low and high threshold inverters in sub-threshold. The basic core of DFF negative latch is presented in section 3. The implementation of the shift register is illustrated in section 4 which can be used in CMOS wireless sensor applications and in the Analog Digital Converter (ADC) based on the Successive Approximation Register (SAR) [8], [9]. The results and simulations are discussed more in details in section 5.

2 Optimized Sub-Threshold Inverter

Operating the static CMOS inverter in the sub-threshold region (weak inversion) of the transistor requires (for both PMOS and NMOS) the input level voltage must be lower than the threshold voltage of the transistor itself. The analysis has been done for the typical process corner low threshold transistor (it is assumed that the whole die has the same density) where the threshold voltage for NMOS and PMOS is 169.1 mV and 343.7 mV respectively (defined at 1 µA). Therefore, to make sure the NMOS is in the sub-threshold region; the input level must be lower than 169 mV (when the input signal to the inverter is high), while for the PMOS the supply voltage must be lower than 343 mV (when the input signal to the inverter is low).

Minimum voltage supply operation occurs when the PMOS and NMOS devices have the same current and it can be achieved through sizing the width of PMOS with respect to NMOS to get the same current. Fig-2 illustrates the minimum voltage level regarding to the failure points at which defines the output of the inverter is lower than 10% of the voltage source when the input signal is high and more than 90% of the voltage source when the input signal is low. The upper bound on size occurs because the sub-threshold leakage through a large NMOS device limits the extent to which the smaller NMOS can pull down the voltage at the output. The curve denoted by WP_max where the output of the inverter is lower than 10% of the supply, while the lower bound on size occurs due to the limitation of small PMOS to pull up the voltage at the output because of the sub-threshold leakage through a large NMOS device. The curve marked with WP_min shows the minimum PMOS width for which the high output voltage achieves higher than 90% of voltage source; the point where the two bounds cross indicates the minimum operating voltage level and the PMOS width needed to achieve that. For a typical transistor in the 90 nm technology, the minimum operating voltage is 98 mV, and the PMOS/NMOS sizing ratio (WP/WN) to achieve this minimum voltage is 3.

Since minimum voltage operation occurs for symmetrical PMOS and NMOS currents, this optimum ratio indicates that the PMOS transistor width of the inverter must be 3 times the width of the NMOS to equalize the sub-threshold currents in this technology. The valid functional operation region as shown in Fig.1 is within the shaded area. The low threshold inverter operates at 98 mV voltage source, when the input signal is 98 mV and zero the output level is 2.019 mV (< 10% Vdd) and 93.89 mV (> 90 % Vdd) respectively.

The minimum voltage supply for the high threshold inverter is 63 mV and the PMOS/NMOS sizing ratio (WP/WN) to achieve this value is around 4 as shown in Fig.2.

![Fig.1 Sizing low threshold inverter for min Vdd](image)
3 Low Power MTCMOS Latch

One of the most effective techniques to minimize the leakage power consumption during the standby mode of the device is Multi-threshold CMOS (MTCMOS) [3], [4], [5] where low threshold device is used in the critical path to improve the performance while the high threshold one in uncritical path. The circuit has proposed in [10] as shown in Fig.3. To achieve the minimisation of the leakage power during the standby mode high threshold transistors are used as an isolation switch between the power supply lines and the virtual lines where during the standby mode the sleep signal will be high (1 logic level), so the high threshold PMOS and NMOS will be switched off and the virtual power supply lines will be floated to eliminate the leakage current [9]. The high threshold inverters are used to hold the output during the standby mode (feedback circuit). To improve the noise performance, T1 and T2 must be a transmission gate instead of pass gate where T1 is used to improve the metastability to ensure that the output of Q1 does not have to fight with the output of Q3 while T2 is used as a switch to open the feedback circuit during the active mode and allows output to follow input. The optimum design to eliminate the sneak leakage current is using local sleep devices [7]. Using only one polarity sleep device (whatever PMOS or NMOS) or sharing the sleep devises causes sneak leakage path and increase the leakage current when a MTCMOS gate shares the output with high threshold CMOS. Consequently, Q1 and Q2 each one must have its own sleep device and the sleep device must have both PMOS and NMOS.

Fig.4 depicts that the output follows the input in the active mode (clock is low) and the output is hold in the standby mode even when the input changes.

4 Shift Register

The shift register is the core of the CMOS image sensor operates at low frequency and the core of the SAR operates at medium frequency where the low power consumption is a big issue for both. One bit shift register is designed based on the latch described in the previous section, where to shift the input data by one clock cycle three blocks of the latch are required; the middle block operates with the inverted clock of the first and last block as illustrated in Fig. 5.

For n-bit shift register, the required number of latches can be calculated from the following equation:

\[ N = 2(n - 1) + 3 \]  

Where N is a number of latches, and n is a number
of shifted bits. For instance, a two-bit shift register requires five latches.

![One bit shift register block](image)

Fig.5 One bit shift register block

5 Simulations

To demonstrate the significance of the power reduction, the simulation was done for 10-bit shift register. The experimental result verifies that the virtual power supply lines during the active mode and standby mode are 249.8 mV (virtual $V_{dd}$), 498.3 μV (virtual GND) and 237.4 mV (floating $V_{dd}$), 80.04 mV (floating GND) respectively.

The leakage current depends on the input states [6]. The experimental results in Table 1 shows the leakage current for different input states, where during the active mode (sleep signal is low) the leakage current is in range of pA while during the standby mode (sleep signal is high) the leakage current in range of nA leading to higher static power consumption.

<table>
<thead>
<tr>
<th>Sleep</th>
<th>INPUT</th>
<th>Leakage Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active mode</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>968.3 pA</td>
</tr>
<tr>
<td>Standby mode</td>
<td>1</td>
<td>3.99 nA</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>27.85 nA</td>
</tr>
</tbody>
</table>

From simulation result, it is illustrated in Table 2 that the power consumption has been decreased during the standby mode due to eliminating the leakage current while the device is in the standby mode the majority of the time so the total power consumption is decreased which is reflected on the battery life time. The experimental results shows for the DFF at 30 KHz with 30 % activity, 250 mV power supply that the maximum power consumption during the active mode is 8.565 nW and 1.625 nW during the standby mode as shown in Table 2; where all currents drawn from the supply was taken in account compared to previous work [1] in which they did not take the effect of the Idriver current in the simulation of the flip flop.

Fig.6 illustrates the output waveform of the 10-bit shift register operates at 30 KHz clock frequency with 30 % activity, 250 mV power supply where the maximum power consumption during the active mode is 37.25 nW, 11.85 nW during the standby mode and power delay product of 97.32 fJ.

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Table 1 Leakage current

<table>
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<tr>
<th></th>
<th>Dynamic power (during active mode)</th>
<th>Static power (during standby mode)</th>
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<tbody>
<tr>
<td>latch</td>
<td>8.565</td>
<td>1.625</td>
</tr>
<tr>
<td>One-bit shift register</td>
<td>37.25</td>
<td>11.85</td>
</tr>
<tr>
<td>Ten-bit shift register</td>
<td>45</td>
<td>22.5</td>
</tr>
</tbody>
</table>

Table 2 Dynamic and Static power consumption

Fig.7 shows the simulated output waveform of the 10-bit shift register operates at 250 mV voltage source, 5 MHz clock frequency with 10% activity. The average power consumption is 6.429 nW while the maximum power in the active and sleep mode respectively are 45 nW and 22.5 nW and the PDP is 24.38 aJ.

The power consumption decreases as the activity decreases as illustrates in Fig.8 that is why this technique is very useful for the circuits, which spend the majority of the time in the standby mode waiting for a certain input.
6 Conclusion

This paper illustrates the design of the low-power static latch in the sub-threshold region based on the MTCMOS technique to achieve high performance during the active mode and low power consumption by eliminating the possible leakage paths through combining the high and low threshold to prevent the leakage current during the standby mode which could be a part of wireless sensor, that using the SAR, could get benefits from this part. Finally, the paper proposed this latch to achieve 250mV supply voltage low power and high speed ten-bit shift register design using the 90nm technology, where the analysis and simulation confirmed the design of 10-bit shift register with 250mV at 5MHz for high speed applications and at 30KHz for low speed applications.

References: