Modular design of an adaptive analog filter shaped as an identifier with CMOS of 0.5 µm

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Abstract: This article presents the modular design of an adaptive analog filter with a technology CMOS of HP of 0.5 mm, whose coefficients adapt using the LMS algorithm. The proposed system is liable to be used in applications that require not only high convergence velocity but also a low consumption of power, and that would be integrated. The results were obtained using the system proposed in configuration as an identifier.

Key-words: Adaptive filter, LMS identifier, CMOS circuit design

1 Introduction

In the last decade the interest for the adaptive analog processing has been increasing in such a way that it is considered greatly as a research subject for the present time. This is due to the advance within the design technologies VLSI that has made possible the development of adaptive analog filter structures that have the capability to handle in real time signals of high frequency, and also implies major convergence velocities, less energy consumption and a small integration and linearity area [1].

These factors make the adaptive analog filters an attractive alternative in respect to the digital ones in practical applications such is the case of the equalization or matching of mobile terrestrial communication channels, echo suppressors etc.

The majority of the adaptive analog filters that have been proposed in literature, use the continuous time version of the algorithm of minimum square percentage (LMS), with a constant convergence factor to actualize the vector of the filter coefficients [2] and that should be maintained small enough to avoid the degradation of the convergence due to the fluctuation of the power of the input signal. The adaptive analog filters present several problems, mainly because of the realization limiting of some circuits in VLSI, for example the analog integration circuits that may degrade considerably the yield or efficiency of the global system. This block is fundamental in the LMS algorithm since it is the one that actualizes the coefficients of the filter; if this block is not properly designed the efficiency of the filter diminishes substantially. In many cases, the integrator circuit may be approximated by a low-pass filter with a cutoff frequency less than the minimum of the frequencies that conform the signal that is processed, that is, as close to zero as it is possible for any signal.

This condition is hard to satisfy in many of the practical applications, encouraging a degradation of the adaptive filter behavior, since a cut frequency very close to zero implies capacitors so big that it's not possible the design en VLSI.

2 Algorithm LMS

Consider the output signal of the generalized transverse filter shown in figure 1, whose Laplace transform is given by:

$$Y(s)=\sum_{k=0}^{N-1} A_k G_k(s) X(s) \qquad (2.1)$$

Where $G_k(s)$ is the transference function of the k-th phase, X(t) is the Laplace transform of the input signal and A_k are the weights of the k-th stage.

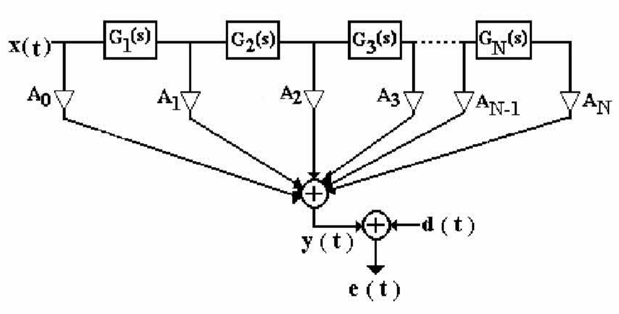

Fig. 1 Generalized transverse filter

2.1 Adaptation Algorithm

Among the most common algorithms used; we have those based in the search of the gradient of which the LMS algorithm is its major exponent. It is due mainly to its robustness and low computing complexity [3]. The expression to calculate the A_k with the LMS continuous time is given by [4].

$$A_k(t) = \beta \int_0^t e(\tau) x_k(\tau) d\tau \qquad (2.1)$$

Where $e(\tau)$ is the output error of the system and $x_k(\tau)$ is the output signal of the k-th phase of the filter shown in figure 1 and β is a factor that controls the stability and adaptation velocity of the algorithm and may be written as:

$$\beta = \frac{\alpha}{X^T(t)X(t)} \qquad (2.2)$$

Where α is the convergence factor of the algorithm and X(t) is the input vector, in this way the algorithm given by the equation (2.1) converges to its optimum value of 0<α<2 [5]. The convergence conditions [6] may be written as:

$$v_k(t) = w_k^* \left[1 - \exp\left(-\beta \lambda_k t\right)\right] \quad k = 1,2,....,N \qquad (2.3)$$

Where λ_k the k-th is own value of the matrix of self-correlation of the input signal and w_k^* is the optimum value of the k-th component of the vector coefficients. The LMS algorithm of continuous time converges if β>0. The condition of convergence derived from the equation (2.3) guarantee that the average value of the vector of the coefficients that converge to the solution of the Wiener-Hopf equation, but do not show the quantity of distortion that will remain in the weights due to the noise produced in the estimate of the instant gradient after the convergence has been obtained. An approximate value, valid for the small values of β is given by [6], [7].

$$E\left[V(t)V^T(t)\right] = \beta \xi_{\min} I \qquad (2.4)$$

Where $\xi_{\min}$ is the value of the minimum half quadratic error which, when the order of the filter is chosen properly is very closed to the power or capacity of the additive noise and I is the identity matrix and $V(t)$ is the error vector [7]. The noise of the weights will cause in addition an error in the output of the system that is given by [8]:

$$\xi_{excess} = \beta \xi_{\min} \left(E\left[X(t)X^T(T)\right]\right) \qquad (2.5)$$

Substituting the equation (2.1) in (2.5) we have:

$$\xi_{excess} = \frac{\xi_{\min} \alpha \left(X^T(t)X(t)\right)}{T^T(t)X(t)} = \alpha \xi_{\min} \qquad (2.6)$$

In that way the power of the additional error in the output of the system due to the noise of the weights of the system, will be proportional to the product of the powers or capacities of additive noise and of the convergence factor α.

3 Modular structure

The structure shown in figure 2 represents the proposal of an adaptable analog modular filter, where each of its basic elements is connected among them. The basic modules of the analog filter are established by: **a)** the delay line, **b)** the analog adaptation LMS algorithm, **c)** multipliers, integrators and analog adders, **d)** the module of velocity control of convergence [8].

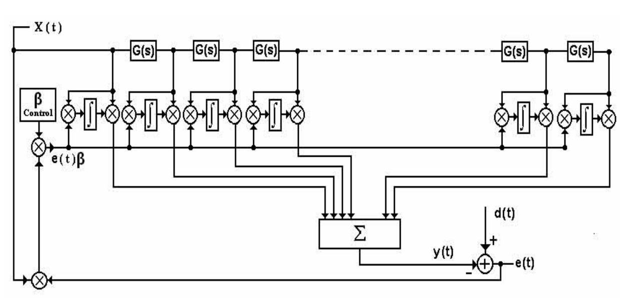

Fig. 2 Adaptive analog modular filter

3.1 Analog delay

For the modules that represent each analog delay, they are designed in such ways that are made with a VLSI circuit. The input signal should be delayed enough so that the LMS algorithm converges.

The analog delay is based in the design of a low-pass filter of a second order with a low frequency pole of 100 KHz in order to process low frequency voice or audio signals (cutoff frequency) type Butterworth [9] as shown in figure 3.

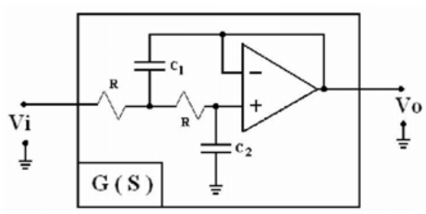

Fig. 3 Structure of an analog delay

The function transference H(s) of the low-pass filter may be written as [10]:

$$H(s)=\frac{k\omega_0^2}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} \qquad (3.1)$$

For the calculation of the capacitors shown in figure 3, its proposed a resistor (R) the 10 KΩ, then 1 the capacitor value that are given in function of the Butterworth polynomials [9] are: $C_1=225pF$, $C_2=112pf$ substituting the capacitors and resistors in equation (3.1) and this may be written as:

$$H(s)=\frac{V_{out}}{V_{in}}=\frac{1}{1-\omega^2\left(R^2C_1C_2\right)+sC_2(2R)} \qquad (3.2)$$

The operational amplifier used in the low-pass filters was designed in a way that it would fulfill or carry out the integration requirements in VLSI. In figure 4 we see the internal structure of the operational amplifier; a CMOS technology [11], of HP of 0.5 μm, was used the electric characteristics of the structure in figure 4 are shown on table 1.

For the operational amplifier design [11], the relation of the width-length transistors (W/L) [12]. The value of L of 4 μm was considered for all the transistors, the calculation of its width of figure 4 is shown on table 2

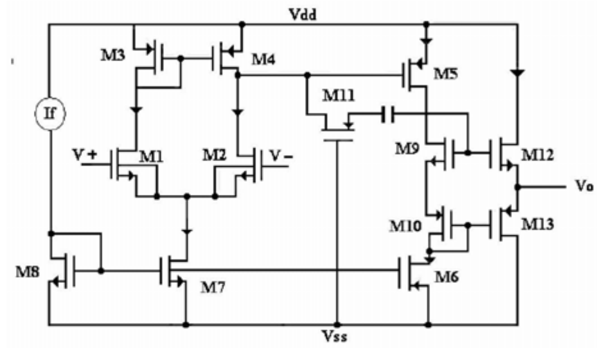

Fig. 4 Internal structure of the operational amplifier.

Table 1 Characteristics of the operational amplifier

Parameters	Values
Unit Gain Frequency	7.41 MHz
Low frequency pole	21.88 Hz
Open loop gain (G)	112.5 dB
Dynamic range differential pair	± 100 mV
Output impedance	111 Ω
Slew rate (Sr)	2.2 v/μs
Power dissipation	7.917 mW
Closed loop gain (-3dB)	7.17 MHz

Table 2 Dimensions of width (W)

$M_1=M_2=225\mu m$	$M_3=M_4=101\mu m$
$M_5=585\mu m$	$M_6=20.7\mu m$
$M_7=M_8=6.3\mu m$	$M_9=30\mu m$
$M_{10}=37\mu m$	$M_{11}=18.3\mu m$
$M_{12}=300\mu m$	$M_{13}=370\mu m$
$C_c=5pF$	

Figure 5 shows the response in the frequency domain analog delay circuit, we may observe that the cutoff frequency in the simulation realized in Pspice is of 100.34 KHz.

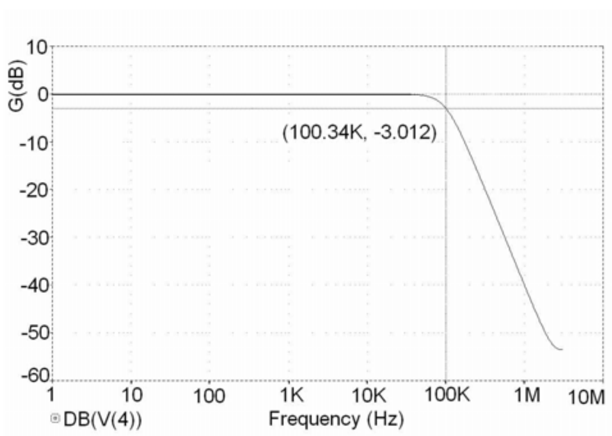

Fig. 5 Response of an analog delay circuit in frequency

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Figure 6 shows the complete delay line, the delay between the input and output signal is of 3.35μs for each of the blocks.

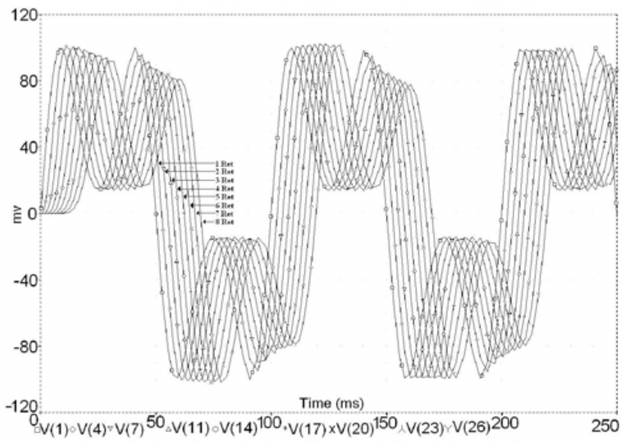

Fig. 6 Analog delay line with eight delays

3.2 Analog Integrator

The proposal of the integrator is shown in figure 7 it is formed by two operational amplifiers, one of them is used in the addition circuit and another as the impedance coupling [7], a first order low-pass net is used.

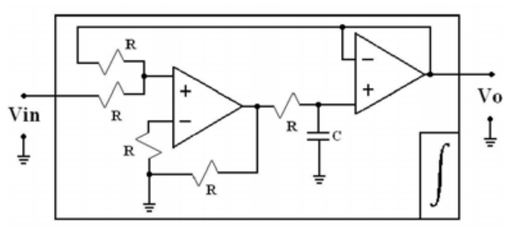

Fig. 7 Structure of the analog integrator

The transference function of figure 7 is:

$$\frac{V_o(s)}{V_i(s)} = \frac{k\frac{A(s)}{A(s)+1}}{s+k-k\frac{A(s)}{A(s)+1}} \tag{3.3}$$

Where A(s) is the open loop gain of the operational amplifier [12] and may be expressed as:

$$A(s) = \frac{GB}{s} \tag{3.4}$$

GB is the gain product band width, substituting the equation (3.4) in (3.3) we obtain:

$$\frac{V_o(s)}{V_i(s)} = \frac{\omega_p}{s^3\frac{1}{(GB)^2}+s^2\left(\frac{2}{GB}+\frac{\omega_p}{(GB)^2}+\left(1+\frac{2\omega_p}{GB}\right)\right)} \tag{3.5}$$

From here ω_p is the cut frequency of the low-pass filter and may be written as:

$$\omega_p = \frac{1}{RC} \tag{3.6}$$

As we are looking for the possibility to integrate this circuit in VLSI, then the capacitor value (C) must be of a few picofarad; for example of 5pF and the resistor (R) could be of a 1KΩ value [2], the operational amplifier used is the same as in figure 5. The response of the integrator in magnitude and phase may be seen in figures 8 and 9, the structure is independent from the position of the low frequency pole, the transference function and it only affects the output signal amplitude it can be observed that the circuit really acts as an integrator from 27 Hz to 5.1 MHz and that the phase is approximately 54.98°.

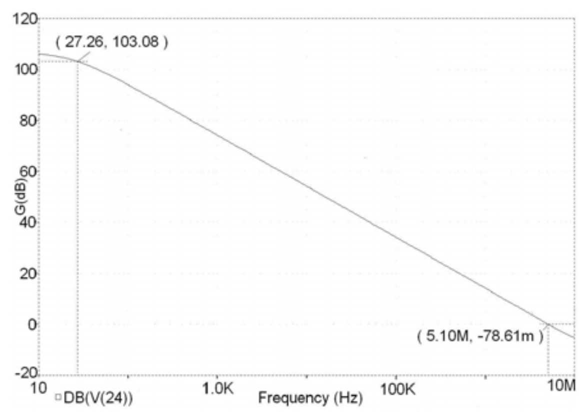

Fig. 8 Response in frequency of the analog integrator

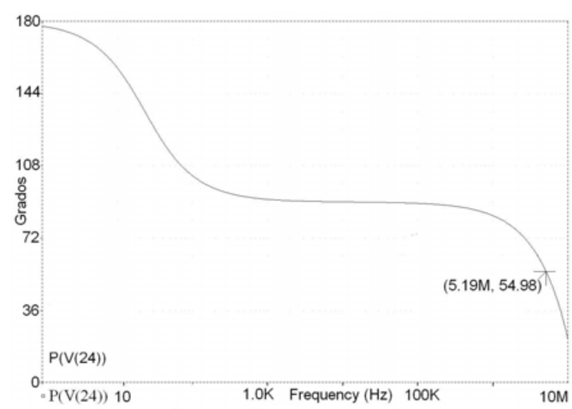

Fig. 9 Phase of the analog integrator

3.3 Analog multiplier of four quadrants in voltage mode.

The analog multipliers have great variety of applications; they are programming elements in systems with analog adaptive filters, digital filters and neural networks. For the application of the identifier a four quadrants multiplier in voltage mode was used. Figure 10 shows the multiplier structure; figure 11 presents the dc behavior response of the multiplier [13]. Table 3 [11], the width dimensions (W) of the transistors are shown and in table 4 the length (L) of the transistors of the analog multiplier.

Table 3 Width dimensions (W) of the transistors and resistors values

$M_{a1,2,3,4}M_{b1,2,3,4} = 60\mu m$	$M_{C1,2,3,4} = 19\mu m$
$R_{b1,2,3,4} = 2.8K\Omega$	$R_{C1,2} = 6.1K\Omega$

Table 4 Length (L) dimensions of the transistors

$M_{a1,2,3,4}M_{b1,2,3,4} = 6\mu m$	$M_{C1,2,3,4} = 2\mu m$

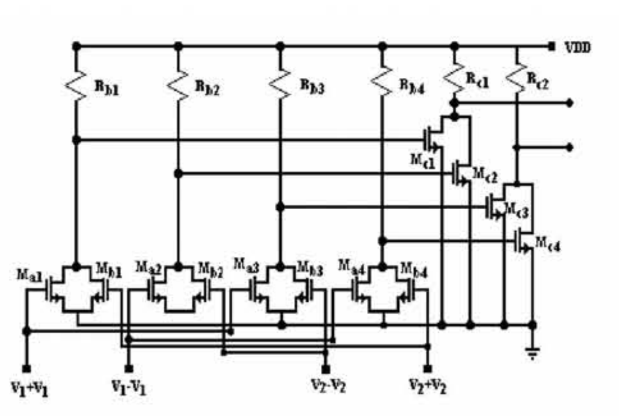

Fig. 10 Structure of four quadrants multiplier

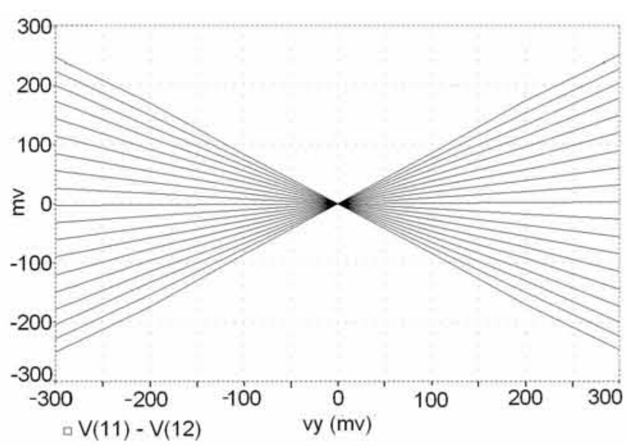

Fig. 11 Multiplier response in dc

The voltage at the output of figure 10 may be written [11], [13] as:

$$V_{out} = \left\{ \begin{array}{l} 1 - \frac{3}{2}(V_1 - V_T)\theta_a - \frac{3}{2}(V_2 - V_T)\theta_b \\ - \left[\begin{array}{l} R_b K_a (V_1 - V_T)^2 + R_b K_b (V_2 - V_T)^2 \\ -V_{DD} + V_T \end{array} \right] \theta_C \end{array} \right\} k' v_1 v_2$$
$$- \left[\frac{1}{2(V_1 - V_2)}\theta_a + 3R_a K_a \theta_c \right] k' v_1^3 v_2 \qquad (3.7)$$
$$- \left[\frac{1}{2(V_2 - V_T)}\theta_b + 3R_b K_b \theta_c \right] k' v_1 v_2^3$$

Where θ_a, θ_b and θ_c is mobility reduction of transistors, k′ multiplication constant, V_t the threshold voltage, v_1 and v_2 the input signals to the multiplier.

3.4 Modeling and simulation of the analog adaptive filter configured as identifier.

Here is presented the module design of an analog adaptive filter configured as an identifier, for this configuration three cases are presented: 1) is a low-pass filter with eight analog delays and eight coefficients for the update of the algorithm weights LMS as shown in figure 12, 2) a low-pass filter with eight analog delays and six coefficients for bringing up to date the weights of the algorithm LMS and 3) a low-pass filter with twelve analog delays and eight coefficients that bring up to date the weights of the LMS algorithm. These three cases were simulated under the following PSpice parameters; an FM input signal (0,100m, 200M, 3, 10K) with a modulation index of 3 and a gain of 0.5 for the weights of the low- pass filter and β.

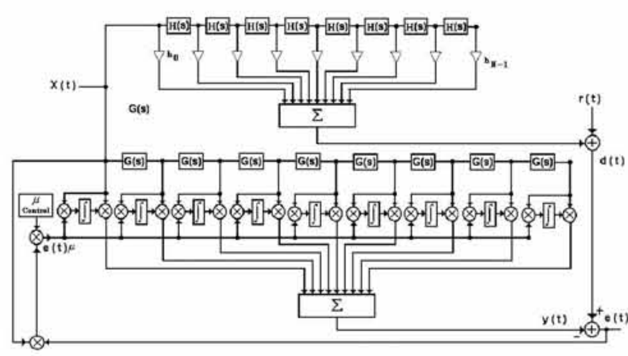

Fig. 12 Adaptive filter used as identifier

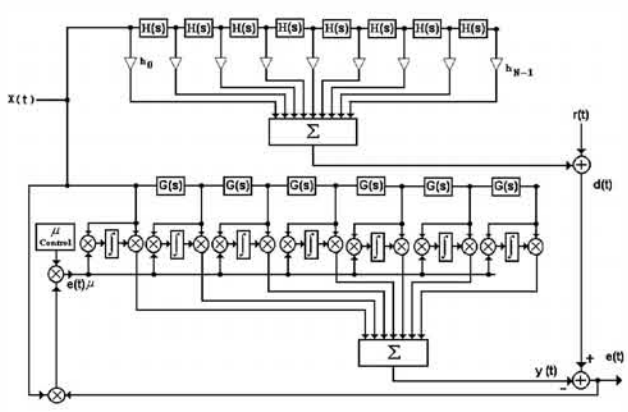

Fig. 13 Adaptive filter with twelve delays in the filter and eight coefficients in the LMS algorithm

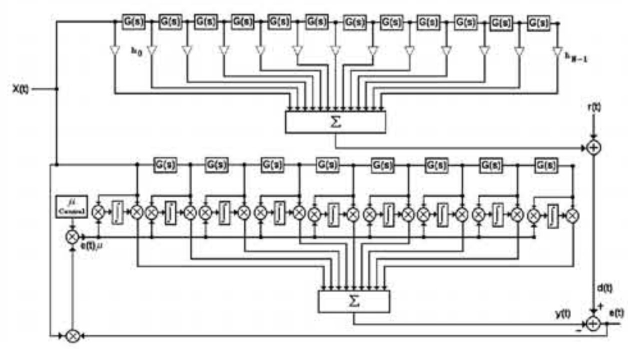

Fig. 14 Adaptive filter with twelve delays in the filter and eight coefficients in the LMS algorithm.

3.5 Results

The next results presented are the evaluation of analog adaptive filter configured as an identifier. Figure 15 shows the response in time of the structure of figure 12. We may appreciate how the estimated signal has a very good approximation to the reference signal; this is reached starting from the 40μs that is when we obtain the convergence of the algorithm.

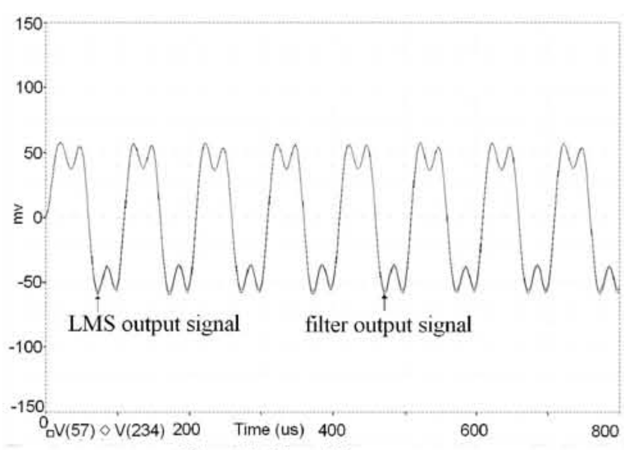

Fig. 15 Identifier output

Figure 16 shows the algorithm error derived from the simulation that is approximately ±2.4mV, the energy consumption is of 0.622 watts.

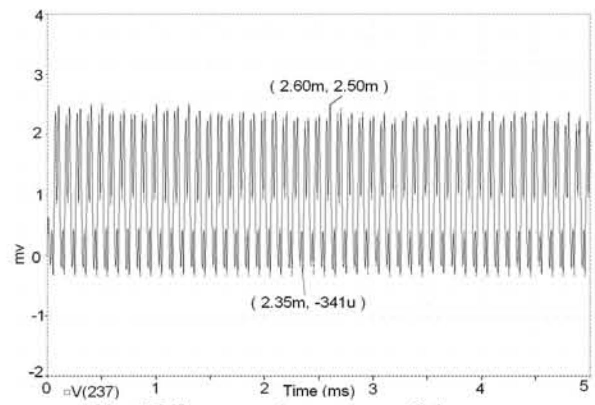

Fig.16 Error at the output of the system

For the second case in figure 17 is shown the response in time domain of the structure of figure 13, we may appreciate how the estimated signal has an approximation to the reference signal, this is reached beginning from 50μs that is when we can obtain the convergence of the algorithm. In figure 18 we observe the error of the shunt or derivative algorithm of the simulation that is approximately ± 20mV, the energy consumption is of 0.520 watts.

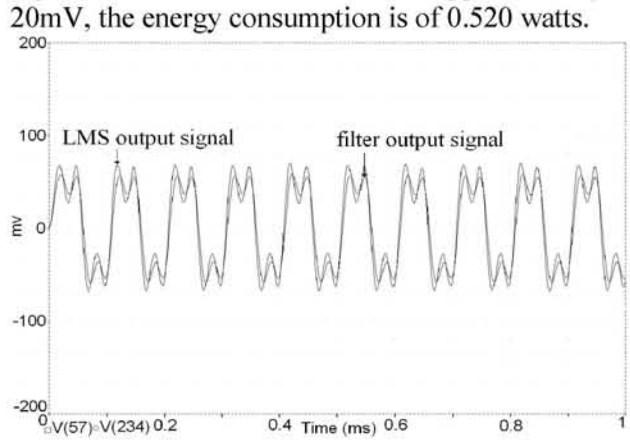

Fig. 17 Output of the LMS algorithm and filter

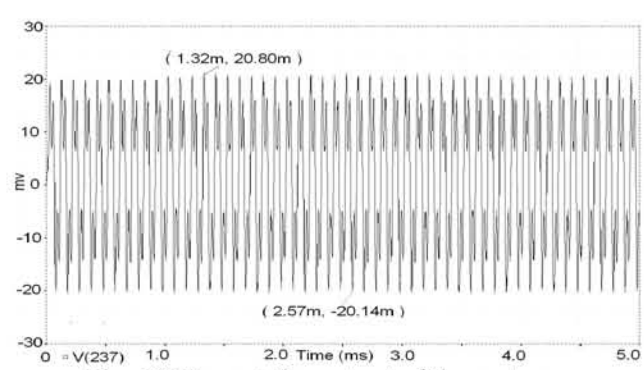

Fig. 18 Error at the output of the system

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For the third case figure 19 shows the response in the time domain of the structure of figure 14, we may appreciate how the estimated signal does not have an approximation to the reference signal this is reached starting from the 60µs that is, when the convergence of the algorithm is obtained. In figure 20 we may see the algorithm error derived from the simulation that is approximately of ± 37.1mV the energy consumption of the circuit is of 0.680 watts.

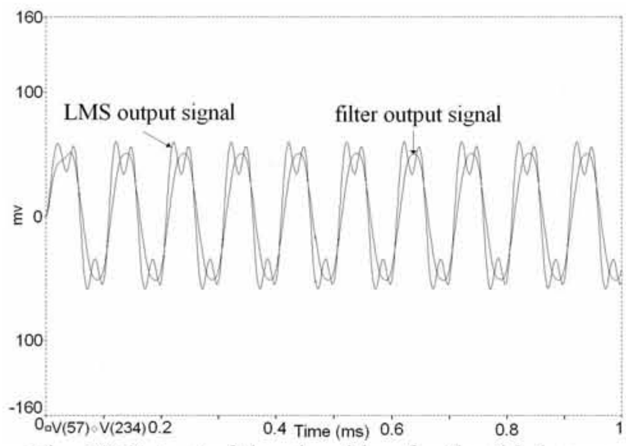

Fig. 19 Output of the algorithm for the third case

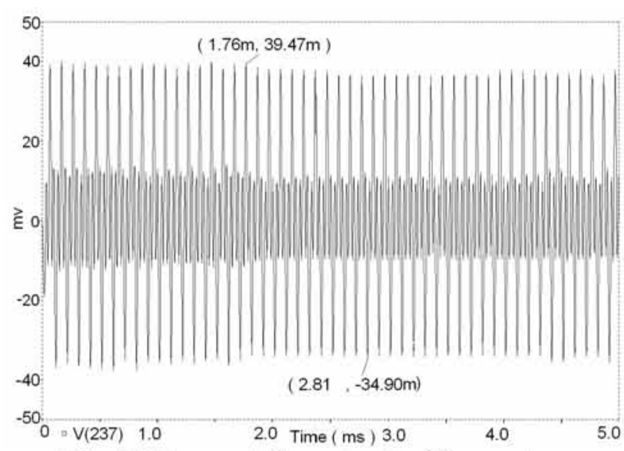

Fig. 20 Error at the output of the system

4. Conclusions

In this study the design is presented in modules concerning the circuits that realize the LMS algorithm in an analog form. The main characteristic of these blocks is that they can be done in a VLSI circuit, carrying out besides the characteristics of low energy consumption, high speed processing with an adequate control of the integration operation that improves the convergence velocity of the algorithm. The results obtained in the configuration as an identifier, show us that the designs presented are a good alternative for the analog adaptive procedure, mainly the first case of section 3.4 that presents a minimum error in comparison to the other two, the structure is possible to apply in portable communication equipment.

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