Optimal Dual Voltage Assignment Algorithm for Low Power under Timing-Constraints

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Abstract—In this paper, we present an optimal voltage assignment algorithm which assigns two supply voltages for each gate in the gate-level netlist. To the best of our knowledge, it is the first work to consider the impact of the level shifter using integer linear programming. The goal is to minimize the total power consumption under the delay constraints. First, we transform the gate-level netlist into a graph which the nodes and edges denote the gates and interconnect between gates, respectively. To speedup the runtime, the node-based concept is incorporated to reduce the timing constraints. All constraints, such as the delay constraints for each path and the total power constraints, are formulated as the linear programming. Hence, the voltage assignment is optimal. Experimental result shows that our proposed algorithm optimizes the power under timing constraints.

Key-Words: Integer linear programming (ILP), low power, dual supply voltage

1 Introduction
Power is the most important concern for the modern IC design. But we usually need to take tradeoff between the power consumption and the chip performance. According the timing-driven low-power researches, the multiple supply voltages technique is regarded the most effective and has been proposed to minimize the power consumption [1].

Recently, most multiple supply voltage techniques were proposed to minimize the power consumption for the design automation, such as the high level synthesis [2], gate level synthesis [3], floorplanning [4] and the placement [5]. Some papers minimized the power consumption by applying the greedy methods [1][5][6][7]. The authors presented the greedy to assign the power for each gate according to the sensitivity of gate [6]. The authors proposed the ECVS-based method to minimize the total power [7]. But some can not handle the multiple supply voltages and usually can not obtain the optimal voltage assignment. In [8], they proposed formulated the statistic voltage scaling problem into a convex optimization and give a methodology to reduce the power. In contrast to the greedy method, some researches proposed the (Integer-Linear Programming) ILP-based method to minimize total power [9][10]. Nguyen et. al presented a three-stage method to reduce power and assigned slack to gates by ILP formulations[9]. [10] provided ILP formulations to reduce leakage and glitch powers. Some methods minimized the power under two supply voltages and some methods were inefficient because they can not reduce the constraints.

The contributions of our proposed methods are as follows. First, we formulate the timing constraints for all paths by listing a set of the linear constraints and obtain the optimal voltage assignment for the given gate level circuits with the timing information. Second, we propose the concept of the node-based method to reduce the redundant timing constraints and we efficiently obtain the voltage assignment for the multiple voltages. Third, we easily extend our ILP formulations to integrate the impacts of the level shifters into the ILP constraints.

The reminder of is as follows. Section 2 formulates the problem and lists terminologies. The ILP-based algorithm is discussed in Section 3. The experimental result and the conclusion are attached in Section 4 and 5, respectively.

Fig. 1 The optimal voltage assignment (C17)
2 Preliminary
In this section, we will describe the motivation of the paper and formulate the low power-driven voltage assignment problem.

2.1 Motivation
For the gate level netlist, we denote the concept of our approach to obtain the optimal voltage assignment under the \( k (=2) \) supply voltages. Because the previous works usually greedily search the current optimal solution, the methods cannot obtain the optimal solution under the three kinds of voltages \((v_h \text{ and } v_l)\), see Figure 1(a). If the timing constraints are transformed into the linear programming, we can obtain the optimal voltage assignment under the given timing constraints. In Figure 1(b), we have the voltage assignment under the 42 ns timing constraint. This example motivates to solve the supply voltage assignment problem by the linear programming to get the optimal solution.

2.2 Problem Definition
The circuit which is composed by the gate can be formulated as a DAG (directly acyclic graph). Given a G = (V, E), which V and E denote the \( n \) gates and the \( m \) interconnects, respectively. For a gate, it has \( k \) supply voltages, \( k \) power consumption and \( k \) gate delays. Under the timing constraints for each path, our objective is to optimize the total power consumption of the gates by multiple supply voltages assigning.

3 An ILP-based Voltage Assignment
In this section, we will describe the ILP-based method in detail. Three advantages of our approach are listed in the next sub-section. Furthermore, we give a simple to demo the concept of our algorithm.

We apply the linear programming to assign the multiple voltages with the objective of minimizing the total power consumption under the given timing constraints. Unlike the traditional greedy method to reduce the power consumption, we can optimize the voltage assignment because we solve the problem by using the linear programming. We discuss the method in the later section.

First, to simplify, we obtain the different gate delay and power consumption under the \( k \) voltages by the delay ratio \((d_{r_{ Delay}} = 2.5)\) and power ratio \((p_{r_{ Power}} = 0.25)\). For a single gate, the power consumption and delay are represented as follows,

\[
\begin{align*}
    d_i &= d_{gate} \times d_{r_{ Delay}}; \\
    p_i &= p_{gate} \times p_{r_{ Power}}; \\
    \end{align*}
\]

For example, let the delay and power for the high supply voltage are 1 ns and 1 mW, delay and power for the low supply voltage are assigned as 2.5 ns and 0.25 mW. In Figure 2, the set of the interconnect wires and gates are denoted by \( E = \{e_i | i > 0, i \leq \text{number of edges}\} \) and \( V = \{v_i | i > 0, i \leq \text{number of nodes}\} \), respectively. Hence, for PI1-g1-g5-PO1 path, the wire delay \( d_{\text{path}} \) is represented as,

\[
    d_{\text{path}} = d_{\text{PI1}} + d_{\text{g1}} + d_{\text{g5}} + d_{\text{PO1}}
\]

Each path in the gate netlist must meet the timing constraints and we have the following:

\[
    d_{\text{path}} \leq \text{delay}_{\text{con}};
\]

We list all constraints for all paths in the netlist and all delays of the paths must be less than the given delay constraints.

\[
\begin{align*}
    d_{\text{path}_1} &= d_{\text{w}_{\text{PI1}}} + d_{\text{g3}} + d_{\text{g5}} + d_{\text{w}_{\text{g3}}} + d_{\text{g5}} + d_{\text{w}_{\text{PO1}}}; \\
    d_{\text{path}_2} &= \leq \text{delay}_{\text{con}}; \\
    d_{\text{path}_3} &= d_{\text{w}_{\text{PI3}}} + d_{\text{g1}} + d_{\text{g5}} + d_{\text{w}_{\text{g1}}} + d_{\text{g5}} + d_{\text{w}_{\text{PO1}}}; \\
    d_{\text{path}_5} &= \leq \text{delay}_{\text{con}};
\end{align*}
\]

However, for the large-size circuits, the edges information is very complex. Hence, we have the huge ILP constraints. For the problem, we propose a node-based method to reduce the number of the constraints. If we describe the timing constraints by the concept of the routing paths, the number of the corresponding constraints is huge. Hence, we only check the timing for the different neighbor gates.
In Figure 3, the delay of the primary output in a gate is defined and used to reduce the volumes of the ILP constraint. For gates 5 and 9, the delay of the primary output is named as “S5” and “S9”, respectively. Unlike the formula (2), the relationships between the gate 5 and 9 are as follows,

\[ S5 + w_{g5}g9 \leq S9 \]
\[ S7 + d_{g7}g9 \leq S9; \]
\[ d_{g9} \leq \text{delay}_{-\text{con}}; \] 
(5)

For the second problem, we will check the voltage relationship and determine if we need to add the level shifter for the edge \( b_{ij} \) which connects the nodes \( x_i \) and \( y_j \). We assume that the \( k(=2) \) supply voltages are \( x_i \) ( \( x_i = 1 \) and \( x_i = 2 \) denote the low and high supply voltages, respectively). It is useful to translate the if-else statement into the ILP constraints. The following is the conditional constraint,

\[ \text{If} \quad (x_i - x_j \geq 0) \quad \text{Then} \quad b_{ij} = 0; \]
\[ \text{Else} \quad b_{ij} = 1; \] 
(6)

where \( x \)'s are integral variables and \( b \)'s are 0/1 variables. To formulate the above statement, we must add an upper bound \( M \), which is a constant over the value of \(|x_i - x_j|\). Hence, we have the following ILP constraints,

\[
\begin{cases}
M \times (b_{ij}) + (x_i - x_j) \geq 0 \\
M \times (1 - b_{ij}) + (x_j - x_i) > 0
\end{cases}
\] 
(7)

According to the formula (5) we can easily add a level shifter if the \( x_i \) and \( x_j \) are low and high supply voltage, respectively. In the paper, we assume that the delay and power statistics are the same. For \( j \) wires, the total penalty of level shifters are computed as follows,

\[ P_{\text{level\_shifter}} = P_{\text{ls}} \times \sum_j b_j \] 
(8)

where \( P_2 \) and \( P_{\text{ls}} \) denote the total power penalty and the power consumption of level shifters, respectively.

Finally, to minimize the power consumption, we optimize the objective function as follows,

\[ \text{minimize} \quad (\alpha \times \sum_{i=1}^{n} p_i + \beta \times P_{\text{level\_shifter}}) \] 
(9)

4 Experimental Result

The proposed algorithms were implemented by using C++ language on an Intel 1.87G machine with 3GB memory. The objective is to optimize the total power consumption under the given timing constraints. Because of the lack of the delay information for the ISCAS benchmarks, the delays of the wires and the gates are randomly assigned form 1 to user-defined upper bound. Besides, we ignore the loading effects of the level shifters after adding them on the routing paths and just add the impacts of the level shifters into the ILP constraints. Due to lack of the LC’s delay and power information, we let the weight \( \beta \) of the penalty is zero. In section 3, we have explained that our optimal assignment can handle two supply voltages.

First, we compare the improvement on total power consumption among the different supply voltage. In table 1, A denotes the number of gates in a circuit. The symbols, I and II denote the one and two supply voltages. Compared to one supply voltage, the improvement on power consumption of II is 46.6%.

Second, we investigate the improvement on the CPU runtime. In table 1, the sixth and seventh columns are the CPU runtime for each benchmark. By using the concept of the node-based ILP constraints in Figure 3, the volumes of the ILP constraints are significantly reduced. For the benchmark with one supply voltage, we can obtain the feasible solution efficiently. For the large benchmarks under the II, we can obtain the results in accepted runtime.
Table 1  Improvement on the total power consumption under one and two supply voltages.

<table>
<thead>
<tr>
<th>No. of gate</th>
<th>Total power consumption</th>
<th>Runtime(sec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I</td>
<td>II</td>
</tr>
<tr>
<td>c17</td>
<td>13</td>
<td>57704</td>
</tr>
<tr>
<td>c432</td>
<td>203</td>
<td>798112</td>
</tr>
<tr>
<td>c499</td>
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<td>2564292</td>
</tr>
<tr>
<td>c1908</td>
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<td>3925828</td>
</tr>
<tr>
<td>c2670</td>
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<td>6584296</td>
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<tr>
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<td>2480</td>
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<tr>
<td>c7552</td>
<td>3827</td>
<td>16213990</td>
</tr>
<tr>
<td>avg</td>
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</tr>
</tbody>
</table>

1 and II denote the one and two supply voltage. IMP(%) denotes the improvement on the power consumption.

5 Conclusion and Future Work

In the paper, we present an optimal voltage assignment algorithm to minimize total power consumption. From the multiple supply voltages in the cell library, the polynomial-time optimal algorithm assigns the proper voltage for each gate. Compared to the traditional method, the proposed algorithm can achieve the optimal assignment solution efficiently. Besides, we discover that the power consumption will be further minimized by 46.6% with the accepted runtime because we reduce the volume of ILP constraints by the node-based concept.

The method can easily extend to handle the multiple supply voltages to optimize the maximum source-to-terminal delay under the power constraints. Besides, we will incorporate the impact on the different level shifters into our ILP-based method.

References:


