A Dual-Edge Triggered Phase Detector for Fast-Lock DLL

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Abstract: - DLL is used as a clock generator due to its stable operation and relatively simple design. Analog DLL has the advantages of lower phase offset and lower clock jitter than digital DLL. However, locking speed is slow in analog DLL. This paper proposes a dual edge triggered phase detector to enhance the locking speed of analog DLL and suggests a closed-form expression of locking speed which can correctly estimate the locking speed. Simulation results show that the locking speed of DLL, which includes the proposed phase detector, is 2~2.5 times better than that of DLL, which includes a single edge triggered phase detector.

Key-Words: Dual-Edge Triggered, Dual-Edge Checking, Phase Detector, PD, DLL, Analog DLL, Locking Speed

1 Introduction

Recently, DLL has been widely used as a clock generator in system on a chip (SOC), since it is simpler and more stable than PLL [1]. Since clock gating is heavily used in SOC to achieve low power consumption, low locking time becomes an important design parameter to minimize recovery time from clock gating. Low jitter and skew of the clock is also required to achieve high performance. Thus, improving locking speed and lowering jitter are main focuses in DLL design [2].

DLL is classified into two types, analog DLL and digital DLL, according to the method used to control the variable delay line. In general, analog DLL has a lower static phase offset and clock jitter than digital DLL. However, analog DLL has the disadvantage of a higher locking time [3]. Several methods have been suggested to reduce the locking time of analog DLL. One of the methods is to use a double-edge triggered phase detector (DET-PD) which samples the DLL input clock at the positive and negative edges [4],[5],[6],[7]. However, DET-PD in [4],[5] have potential problems such as false or harmonic lock and locking speed that are not efficiently improved due to low PD output characteristic in [6],[7].

This paper proposes a high output characteristic DET-PD by utilizing widely used TSPC-PD and also suggests a closed-form expression of locking speed. In Section 2, the architecture and operation principle of the proposed high output characteristic DET-PD is described and a closed-form of locking speed is derived. The performance of a single edge triggered PD (SET-PD) and the proposed DET-PD are compared through HSPICE simulation with the model parameter of industry 0.18um CMOS technology in Section 3, and finally, the conclusion is in Section 4.

2 Circuit Design and Analysis

2.1 Circuit Design of the proposed DET-PD

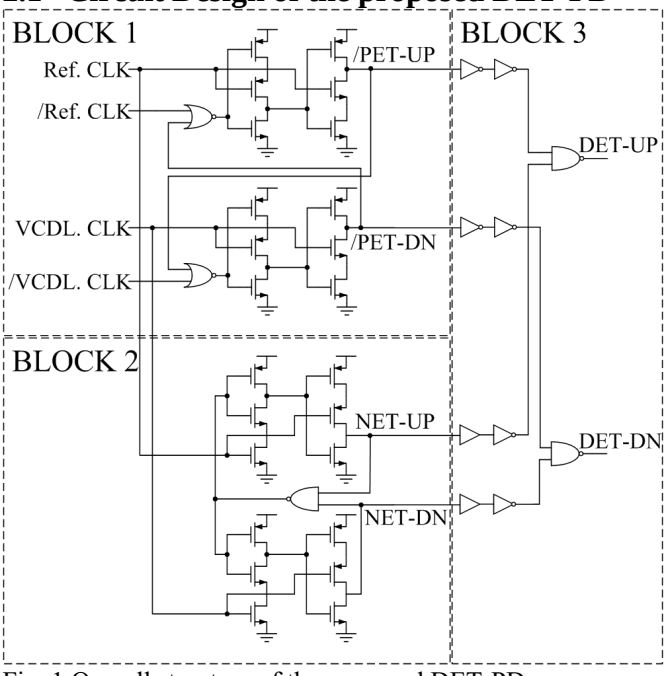

Fig. 1 Overall structure of the proposed DET-PD

Fig.1 shows the overall structure of the proposed DET-PD. Block 1 is the positive edge triggered phase detector (PET-PD), which produces the comparison result between the positive edge of the reference clock and that of the voltage controlled delay line (VCDL)

output. Block 2 is the negative edge triggered phase detector (NET-PD), which produces the comparison result between the negative edge of the reference clock and that of VCDL output. Finally, Block 3 merges the signals from Block 1 and Block 2 and sends a merged signal to the charge pump.

The PET-PD used in Block 1 is a modified TSPC-PD [8], which has a linear output characteristic identical to the conventional TSPC-PD when the input phase difference ranges from $-\pi$ to π and has constant output characteristic when input phase difference ranges from -2π (π) to $-\pi$ (2π). In addition, while the reset path of the conventional TSPC-PD uses one NOR gate, which results in loss of the phase capture range around $n\pi$ [9], the proposed PET-PD reduces the loss of the phase capture range by separating the reset path into two paths. The NET-PD used in Block 2 is built by reconstructing PMOS and NMOS positions from the conventional TSPC-PD [7]. The operation of NET-PD is the same as that of the conventional TSPC-PD except that it detects the phase difference at the negative edge instead of the positive edge.

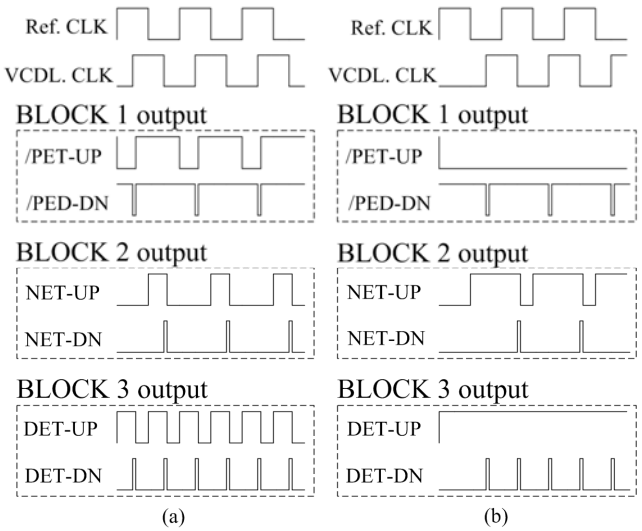

Fig. 2 Timing Diagram (a) $-\pi \sim \pi$ range (b) $-2\pi \sim -\pi$ and $\pi \sim 2\pi$ range

Fig.2 shows the timing diagram of the proposed DET-PD. Since UP and DN are generated by PET-PD and NET-PD alternatively when the phase difference is from $-\pi$ to π and the /PET-DN (/PED-UP) is a constant of GND when the phase difference is from -2π (π) to $-\pi$ (2π). Thus, combination of some NAND gates, inverters and buffers can merge the outputs of PET-PD and NET-PD.

The output characteristics of several DET-PDs are shown in Fig.3. The output characteristic of PD in [4],[5] is the same as that of the proposed DET-PD when the phase difference is from $-\pi$ to π, but the phase capture range is limited to $-\pi \sim \pi$, which results in a fatal problem, such as false or harmonic lock, if the initial phase difference is outside the range of $-\pi \sim \pi$ [10]. Since the PD in [6] has infinite phase capture range, there is no false or harmonic lock issue. However, the locking speed is slow since the output characteristic is the same as the conventional SET-PD.

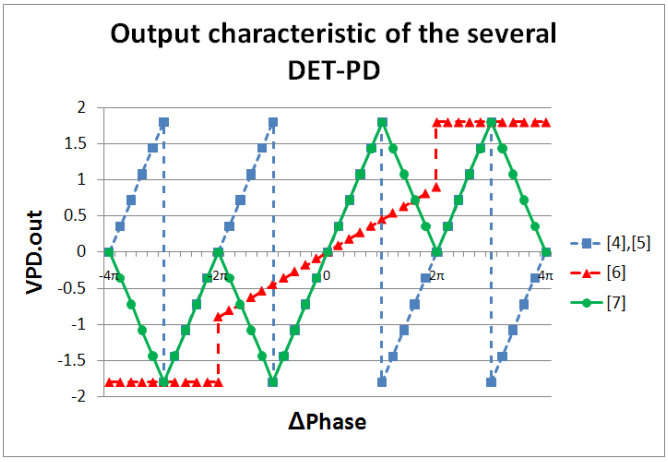

Fig. 3 Output Characteristics of the several DET-PDs

The PD in [7] has the same output characteristic as the proposed DET-PD when the phase difference ranges from $-\pi$ to π but the output characteristic is significantly degraded when the phase difference ranges from -2π (π) to $-\pi$ (2π). Thus, locking speed slows down if the initial phase difference is in the range of -2π (π) to $-\pi$ (2π). The proposed DET-PD's output characteristic doubles when the phase difference ranges from $-\pi$ to π compared to the SET-PD since two UP and DN are generated and it has the constant output characteristic of –VDD (VDD) when the phase difference ranges from -2π (π) to $-\pi$ (2π). Therefore, the proposed DET-PD can achieve a wide phase capture range of $-2\pi \sim 2\pi$ and high output characteristic, which results in a fast locking speed in the range of $-2\pi \sim 2\pi$.

2.2 Numerical Analysis

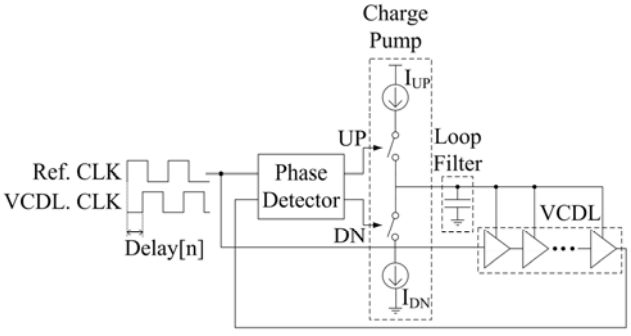

Fig. 4 Block Duagram of Analog DLL

Fig.4 shows the block diagram of analog DLL. The increase of PD output characteristic has direct impact on the locking speed of DLL and can be mathematically analyzed. It is assumed that DN (UP) is generated to increase (decrease) VCDL control voltage if the DLL delay needs to be increased (decrease). In other words, the gain of the VCDL has positive polarity.

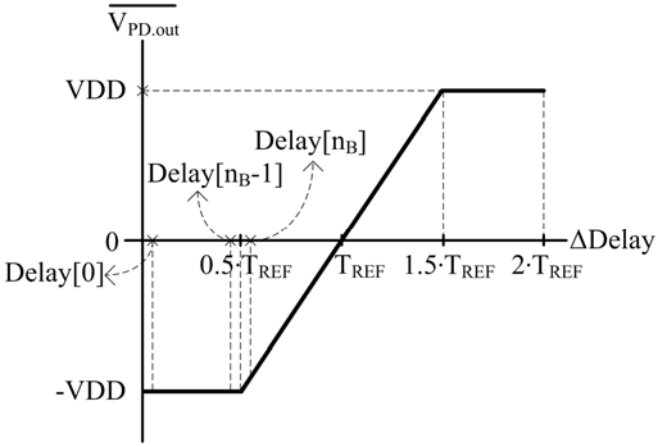

Fig. 5 Output Characteristic of the proposed DET-PD

Fig.5 shows the output characteristic of the proposed DET-PD in terms of delay. The change of VCDL control voltage, ΔV_{CTRL}, charged on the loop filter by the charge pump during one period of the reference clock is given by the following equation.

$$\Delta V_{CTRL} = \frac{\Delta Q}{C_{LF}} = -\frac{(I_{UP} \cdot T_{UP} - I_{DN} \cdot T_{DN})}{C_{LF}} \quad (1)$$

where C_{LF} is a capacitance of the loop filter.

Since ($T_{UP} - T_{DN}$) is the time the net current flows through the loop filer during one period of the reference clock, it can be represented by a portion of the reference clock period, T_{REF}. The proportional coefficient of α between ($T_{UP} - T_{DN}$) and T_{REF} can be obtained by the ratio of the average voltage value of UP pulse minus DN pulse over VDD, with the assumption that $I_{UP} = I_{DN} = I_{CP}$, ΔV_{CTRL} is

$$\Delta V_{CTRL} = \frac{\Delta Q}{C_{LF}} = -\frac{I_{CP} \cdot (T_{UP} - T_{DN})}{C_{LF}} = -\frac{I_{CP} \cdot \alpha T_{REF}}{C_{LF}} \quad (2)$$

where, $\alpha = \frac{\overline{V_{PD.out}}(delay[n])}{V_{DD}}$ (3)

The change of VCDL delay according to the change in VCDL control voltage is

$$\Delta delay = K_{VCDL} \cdot \Delta V_{CTRL} \quad (4)$$

Then, the delay of the DLL at $(n+1)^{th}$ iteration is

$$delay[n+1] = delay[n] + \Delta delay$$

$$= delay[n] - \frac{I_{CP} \cdot K_{VCDL}}{C_{LF}} \cdot \alpha T_{ref} \quad (5)$$

$I_{CP} \cdot K_{VCDL} / C_{LF}$ is equal to the DLL bandwidth divided by the reference clock frequency [11] and thus (5) is simplified as the following equation, which is applied to all operation regions of the general DLL shown in Fig.4.

$$delay[n+1] = delay[n] - \frac{w_n}{F_{REF}} \cdot \alpha T_{ref} \quad (6)$$

Since the output characteristic of the proposed DET-PD is different according to the delay of the DLL, the locking time analysis must be performed with consideration to the output characteristic difference. If delay[n] is between 0 and $0.5 \cdot T_{REF}$, the output characteristic is a constant of –VDD and thus α is -1 from the following equation.

$$\alpha = \frac{\overline{V_{PD.out}}(delay[n])}{V_{DD}} = \frac{-V_{DD}}{V_{DD}} = -1 \quad (7)$$

By combining (6) and (7), the delay[n] when delay[n] is between 0 and $0.5T_{REF}$ is

$$delay[n] = delay[0] + n \cdot (\frac{w_n}{F_{REF}} \cdot T_{REF}) \quad (8)$$

where, delay[0] is the initial delay of DLL

If delay[n] is between $0.5 \cdot T_{REF}$ and T_{REF}, the output characteristic is linear. In this case, α is given by

$$\alpha = \frac{V_{PD.out}(delay[n])}{V_{DD}} = 2 \cdot \frac{V_{DD}}{T_{REF} \cdot V_{DD}} (delay[n] - T_{REF})$$

$$= \frac{2}{T_{REF}} (delay[n] - T_{REF}) \quad (9)$$

If delay[0] is between 0 and $0.5 \cdot T_{REF}$ as shown in Fig.5, the constant output characteristic is applied up to n_B^{th} iteration and the linear output characteristic is applied to iterations after n_B^{th} iteration. From (8), n_B^{th} delay is

$$delay[n_B] = delay[0] + n_B \cdot (\frac{w_n}{F_{REF}} \cdot T_{REF}) \quad (10)$$

With (9) and (10), (6) is,

$$delay[n] - T_{REF} = (1 - \frac{2 \cdot w_n}{F_{REF}})^{n - n_B} \cdot (delay[n_B] - T_{REF})$$

$$= (1 - \frac{2 \cdot w_n}{F_{REF}})^{n - n_B} \cdot (delay[0] + n_B \cdot (\frac{w_n}{F_{REF}} \cdot T_{REF}) - T_{REF}) \quad (11)$$

If delay[n] becomes T_{REF}, the DLL is called locked. However, it requires infinite iterations from (11). Since infinite iterations are meaningless, (11) can be analyzed with the following equation.

$$| delay[n_T] - T_{REF} |$$

$$= | (1 - \frac{2 \cdot w_n}{F_{REF}})^{n_T - n_B} \cdot (delay[0] + n_B \cdot (\frac{w_n}{F_{REF}} \cdot T_{REF}) - T_{REF}) | < \varepsilon \quad (12)$$

Thus, if the difference between the delay of DLL at the n_T^{th} iteration and one period of the reference clock is less than ε, DLL can be considered locked. Since $0.5 \cdot T_{REF}$ exists between delay[n_B-1] and delay[n_B] and n_B is an integer, n_B is obtained by the following equations.

$$n_B - 1 < \frac{0.5 \cdot T_{REF} - delay[0]}{\frac{w_n}{F_{REF}} \cdot T_{REF}} < n_B \quad (13)$$

$$n_B = \left\lceil \frac{0.5 \cdot T_{REF} - delay[0]}{\frac{w_n}{F_{REF}} \cdot T_{REF}} \right\rceil \quad (14)$$

n_B exists at the boundary between constant output characteristic and linear output characteristic and thus n_B is 0 in the case of delay[0] > $0.5 \cdot T_{REF}$

On the other hand, DLL is considered locked if the following equation is satisfied for DLL using SED-PD which has linear output characteristic in range of 0 ~ $2 \cdot T_{REF}$.

$$| delay[n_T] - T_{REF} | = | (1 - \frac{w_n}{F_{REF}})^{n_T} \cdot (delay[0] - T_{REF}) | < \varepsilon \quad (15)$$

The relative locking speed can be obtained by the following equation when SET-PD and the proposed DET-PD are used in DLL.

$$n_{T_{DET-PD}} = \frac{n_{T_{SET-PD}} \cdot \ln(1 - \frac{w_n}{F_{REF}}) + \ln(\frac{delay[0] - T_{REF}}{delay[0] + n_B \cdot T_{REF} - T_{REF}})}{\ln(1 - \frac{2 \cdot w_n}{F_{REF}})} \quad (16)$$

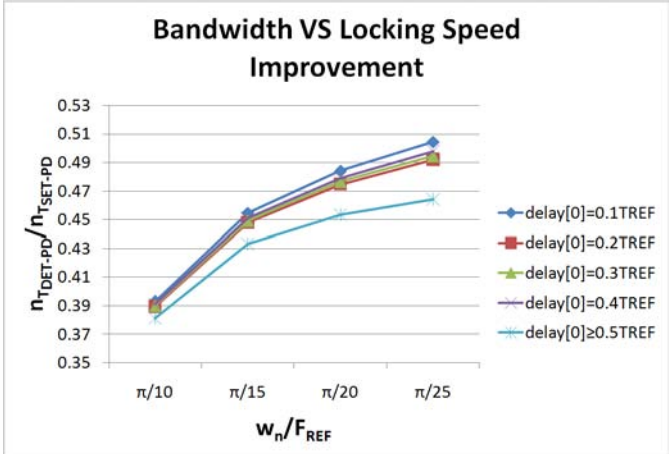

Fig. 6 Locking time improvement according to delay[0] and DLL bandwidth

Fig.6 shows locking time improvement according to delay[0] and DLL bandwidth. In the case of delay[0] ≥ $0.5 \cdot T_{REF}$, the output characteristic of the proposed DET-PD is always two times greater than that of SET-PD. Thus the locking time reduction rate is constant regardless of delay[0] with a given DLL frequency. In the case of delay[0] < $0.5 \cdot T_{REF}$, output characteristic improvement of the proposed DET-PD is reduced, since the output characteristic of the proposed DET-PD is constant. Thus, the locking time reduction rate is reduced and changed according to delay[0]. As shown in Fig.6, the proposed DET-PD can reduce locking time by 50~60%.

3 Simulation Result & Comparison

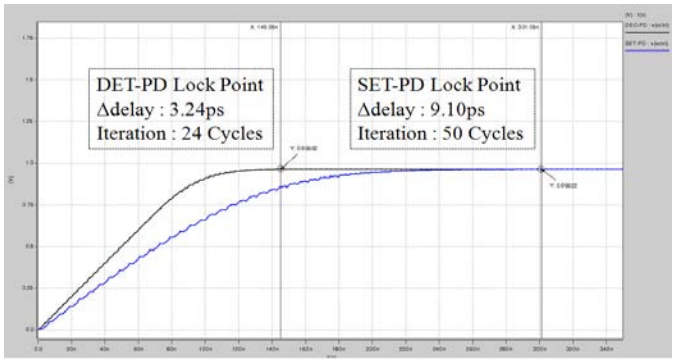

Fig. 7 Comparison of DLL locking process between DLL with DET-PD and DLL with SET-PD

Fig.7 shows the locking process of DLL with DET-PD and DLL with SET-PD. This simulation is performed on the condition that w_n/F_{REF} is limited to π /20 and initial delay is about $0.3 \cdot T_{REF}$. It is assumed that DLL is locked when $|delay[n]-T_{REF}|$ is less than 10ps (i.e. ε=10ps at Eq.(12)). Simulation results show that the locking time of DLL with DET-PD is 52% faster than that of DLL with SET-PD. This simulation result is matches well with the calculated result by Eq.(16).

Table. 1 Comparison of locking time reduction between calculated result and simulation result

Initial delay	$0.3 \cdot T_{REF}$				$0.4 \cdot T_{REF}$			
w_n/F_{REF}	π/10	π/15	π/20	π/25	π/10	π/15	π/20	π/25
Calculated result - (A)	39.0%	44.9%	47.7%	49.5%	39.1%	45.1%	47.9%	49.8%
Simulation result - (B)	46.7%	46.8%	48.0%	49.0%	40.0%	41.7%	43.2%	43.6%
| (A) - (B) |	5.70%	1.90%	0.30%	0.50%	0.90%	3.40%	4.70%	6.20%

Table.1 shows caluclated and simulated locking time reduction in the case of initial delay of $0.3 \cdot T_{REF}$ and $0.4 \cdot T_{REF}$. The calculated locking time reduction using Eq.(16) tracks the simulated locking time reduction quite well.

Meanwhile, the reasons for the difference between calculated locking time reduction and simulated locking time reduction can be summarized by the following two factors. First, preceding equations are derived under the assumption that the pull-up path current and pull-down path current of the charge pump are perfectly matched. However, in general, the charge pump has current mismatch and a simple charge pump is used in this simulation. If current-matching charge pump [12] is used, the difference between the calculated result and simulation result can be reduced. Second, preceding equations also assume that the gain of the VCDL is constant. However, the gain of the VCDL is constant in a limited VCDL control voltage range. This condition also causes an imperfection in preceding equations.

4 Conclusion

Analog DLL is inherently suitable for clock generators because of its low jitter, small static phase offet and stable operation. Slow locking speed is the main shortcoming of analog DLL. This paper suggests a dual-edge triggering phase detector structure to improve the locking speed of analog DLL. The proposed dual-edge triggered phase detector performs better than previous dual-edge triggering phase detectors in regard to locking speed. Also, the locking speed of DLL, which includes proposed double-edge triggered phase detector is mathmatically analyzed. Simulation results show that locking speed of DLL with the proposed double-edge triggered phase detector is 50%~60% faster than that of DLL with a single-edge triggered phase detector and mathmetical analysis effectively tracks real DLL operation.

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References:

[1] C.Kim, I-C.Hwang and S-M.Kang, "A Low-Power Small-Area 7.28-ps-Jitter 1-GHz DLL-Based Clock Generator." *IEEE J. Solid-State Circuits*, Vol.37, No.11, 2002, pp. 1414-1420.

[2] J-S Wang, Y-M Wang, C-H chen and Y-C Liu, "An Ultra-Low-Power Fast-Lock-in Small-Jitter All-Digital DLL." in *IEEE Int. Solid-State Circuits Conf.*, 2005, pp. 422-423.

[3] G-K Dehng, J-W Lin and S-I Liu, "A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm" *IEEE J. Solid-State Circuits*, Vol.36, No.10, 2001, pp. 1464-1471.

[4] C-P Chou, Z-M Lin, J-D Chen, "A 3-ps dead-zone double-edge-checking phase-frequency-detector with 4.78 GHz operating frequencies." in *IEEE Asian-Pacific Conference on Circuits and Systems*, 2004, pp. 937-940

[5] Y Ge, W Feng, Z Chen, S Jia, L ji, "A fast locking charge-pump PLL with adaptive bandwidth." in *Int. Conference on ASIC*, 2005, pp. 383-946

[6] S.I. Ahmed and R.D. Mason, "A dual edge-triggered phase-frequency detector architecture." in *Int. Symposium on Circuits and Systems*, 2003, pp. 721-724

[7] Y-P Zhou, Z-Q Lu and Y-Z Ye, "A Double-Edge-Triggered Phase Frequency Detector for Low Jitter PLL." in *Int. Conference on Solid-State and Integrated Circuit Technology, 2006*, pp. 1963-1965

[8] B-G Kim and L-S Kim, "A 250-MHz-2-GHz wide-range delay-locked loop." *IEEE J. Solid-State Circuits*, Vol.40, No.6, 2005, pp. 1310-1321.

[9] M Mansuri, D Liu and C-K Ken Yang, "Fast Frequency Acquisition Phase-Frequency Detectors for GSamples/s Phase-Locked Loops." *IEEE J. Solid-State Circuits*, Vol.37, No.10, 2002, pp. 1331-1334.

[10] H-H Chang, J-W Lin, C-Y Yang and S-I Liu, "A Wide-Range Delay-Locked Loop With a Fixed Latency of One Clock Cycle." *IEEE J. Solid-State Circuits*, Vol.37, No.8, 2002, pp. 1021-1027.

[11] A. Chandrakasan, W.J.Bowhill, F.Fox, "design of high performance microprocessor circuits", IEEE PRESS, 2000

[12] J-S Lee, M-S Keel, S-I Lim and S Kim, "Charge pump with perfect current matching characteristics in phase-locked loops", *Electronics Letter,* Vol.36, No.23, 2000, pp. 1907-1908