

Efficiency Optimized, EMI-Reduced Solar Inverter Power Stage

K. H. Edelmoser,
Institute of Electrical Drives and Machines
Technical University Vienna
Gusshausstr. 27-29, A-1040 Wien
AUSTRIA

F. A. Himmelstoss
Technikum Wien
University of Applied Science
Hochstaedtplatz 5, A-1200 Wien
AUSTRIA

Abstract: - In the field of electrical solar power conversion efficiency is the most important topic. In most applications a special DC-to-DC converter is necessary to couple the solar cells, operating at low DC-voltages, to the inverter's DC-link. These converters with rather low input respectively high output voltage ratings have, due to the high current ratings, a relatively low efficiency. Furthermore conventional power inverters used in mains connected applications fight with the disadvantage of the hard switched PWM power stage. Alternatively, also soft switching topologies would not give full benefits. A simple modification in output section of a hard-switched topology, however, can lead to a significant improvement of the system losses. Only two additional components (diodes) are necessary to optimize the power stages for usage in a mains coupled inverters. The topology presented in this paper shows a remarkable improvement of the switching losses as well as a significantly enhanced EMC. Consequently, it is well suited for solar power inverter applications.

Key-Words: - EMI-Reduction, Inverter, Switching Leg, Solar Energy, PWM, Losses

1. Introduction

State of the art switching mode PWM converters are industrial standard in the field of power conversion for renewable energy applications. The starting point of our investigations was a solar inverter with the goal of excellent efficiency operating at the European power grid (230V). Power stages for highly dynamic actuators and servo motor drives up to several kilowatts are another field of application for such inverters. In this paper a new concept is shown which increases the converter output voltage quality to meet high mains quality and reduce EMC problematic.

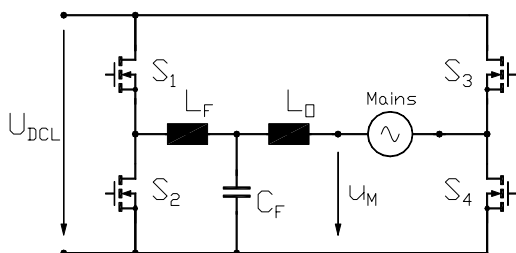


Figure 1.a: State-of-the-art solar inverter, basic topology (PWM power stage represented by S_1 & S_2 , inverter-stage build by S_3 & S_4)

The main drawback of conventional PWM-inverters (cf. Fig. 1) operating from a 400V DC-link is the wide variation of the output voltage (0..325V in this case) as well as the high switching frequency in order to

minimize the energy storage elements (inductors / capacitors) [1,2]. The switching ripple of the output voltage caused by the limited switching frequency of the inverter leads to the requirement of a complex EMC-filter. A further big problem is the high DC-link voltage (based on the buck-principle of the half-bridge topology) leading to remarkable switching losses. (For all further shown inverter topologies only the left stage is drawn.)

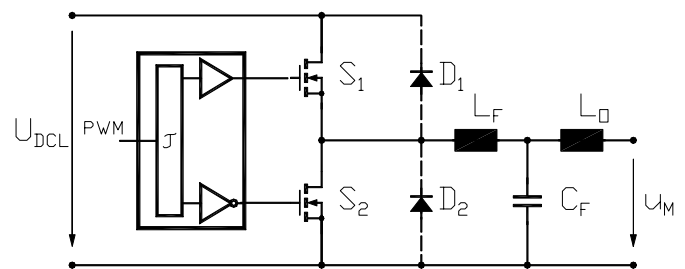


Figure 1.b: State-of-the-art PWM power stage of a DC-to AC solar inverter

To overcome the drawbacks mentioned above, for high performance solar power converters four possible solutions are given [3,4]:

1. Conventional PWM stages operating at an increased switching frequency. With this solution, the design and realization of the output filter is simple. Disadvantages, however, in this case are the significant

switching losses as well as the switching noise (EMC problematic caused by high dv/dt -rates) of the inverter stages.

2. Multi-phase PWM solution. This concept reduces the output voltage ripple of the converter and its input ripple current stress if the individual converter branches are operated in an phase-shifted (interleaved) manner. The disadvantage of this solution, however, is the much more complex control stage and the increased component count.

3. A resonant operated switching. In this case additional control and power circuit requirements are necessary which leads to a much more complex design. Furthermore, the power components show an additional resonant current/voltage stress. In addition, it has to be noticed that usually the efficiency at partial load is lowered by the additional resonant currents.

4. Optimized hard switching structure. Alternatively, a partial separation of the switching leg components as proposed by this paper can be used to fulfill all mentioned design requirements. Here a conventional control scheme (similar to normal PWM operation) can be applied while the system efficiency is maximized.

In practice there are two possible approaches: Optimization of the switch and optimization of the switching stage. A possible solution described in [5] is to pinch-off the MOSFET body diode (worse reverse recovery) by a blocking diode D_S in order to use an additional explicit fast free-wheeling diode D as shown in Fig. 2. However, especially in case of low operation voltage the additional forward losses caused by D_S have to be pointed out. Here also a further improvement by shorting D_S using an additional low-voltage MOSFET would be of advantage.

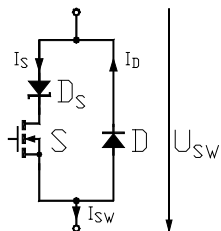


Fig. 2: Power switch with pinch-off of the MOSFET's body diode.

A second possibility for improving the switching leg is the load current path separation as depicted in its principal solution by Fig. 3. The drawback of this method is that two identical inductors (L_{F1} & L_{F2}) are

required, so the filter component exploitation is reduced to 50% compared to classic solutions.

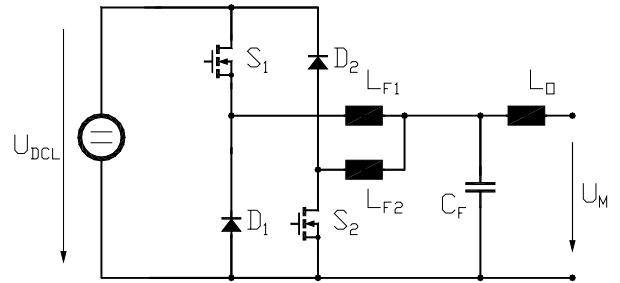


Fig. 3: Power switching stage improved by current path separation.

Based on this topology two further possible types of realization can be achieved: In Fig. 4 an optimized switching leg using a single inductor with two windings is shown. A principal disadvantage, however, comes from the stray inductance of the inductor windings leading to a less efficient design.

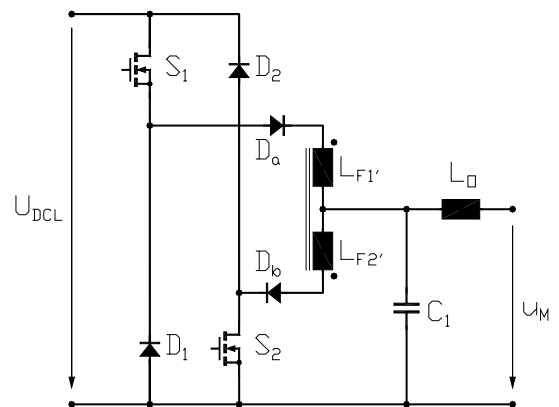


Figure 4.a: Modified Power stage of a DC- to AC solar inverter.

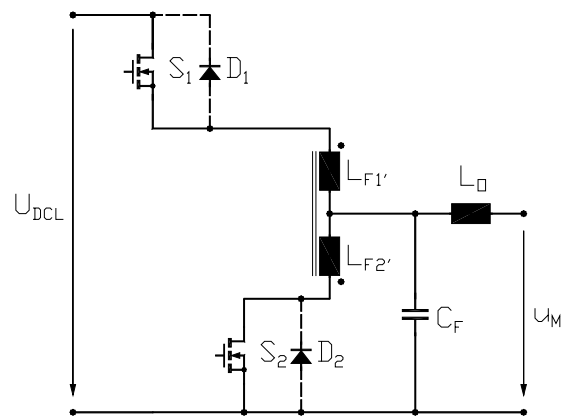


Figure 4.b: Simplified Power stage for PWM-inverter usage.

2. EMI optimized switching leg

Figure 5 depicts the circuit topology proposed by this paper which shows additional benefits in EMC characteristics and efficiency compared to the given solutions. Here the originally separated current paths are partly combined again, similar to Fig. 3, but due to the voltage divider (L_{Fa} , L_{Fb}) the dynamic component stress of S_2 and D_2 can be controlled by the designer. The result is a simple 4-q structure with an asymmetric filter depending on output current direction.

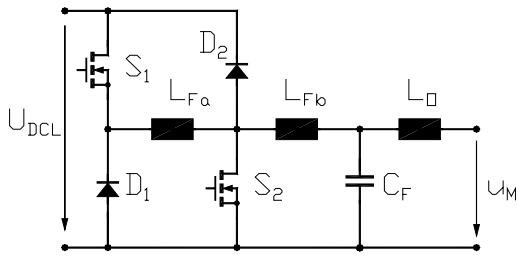


Fig. 5: Efficiency Optimized inverter power stage.

In practice, especially in local grid inverter applications the load factor $\cos(\varphi)$ can vary in a range from typically $[-0.7...1...+0.7]$. This leads to a maximum of approximately 30% of the output power resulting from the reactive behaviour has to be handled from the step-up structure build by S_2 & D_2 and the inductor L_{Fb} . This fact can be used to optimize the structure and to select the components.

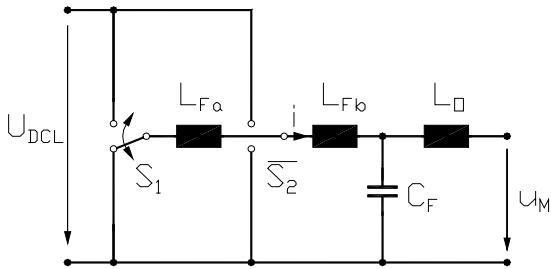


Fig. 6.a: Step-down operation.

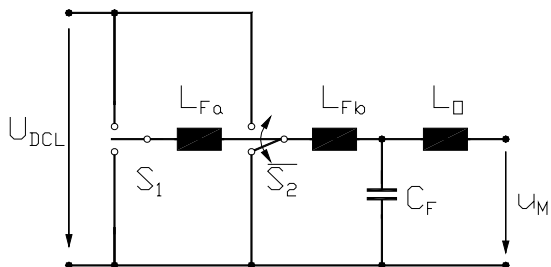


Fig. 6.b: Step-up operation.

As indicated in Fig. 6.a during normal operation (i.e., positive load current) the step-down converter operates

to ($L_{Fa} + L_{Fb}$) leading to a quite smooth output current ripple (1). Depending on the load factor $\cos(\varphi)$ negative output current will occur. The amount of the reactive load is usually only a fraction of the nominal rated current. So the smaller negative output current can also be handled by a smaller inductor L_{1b} (c.f. Fig. 6.b), (2). The advantage of this solution is the reduction of the switching losses of the second switching stage (S_2 & D_2) and the minimization of the magnetic components as compared to Fig. 2.

The rise of the current of the active switches can be described by

$$\frac{di_{S1}}{dt} = \frac{U_{DCL} - U_{CF}}{L_{Fa} + L_{Fb}} \quad (1)$$

$$\frac{di_{S2}}{dt} = \frac{U_{DCL} - U_{CF}}{L_{Fb}} \quad (2)$$

The relationship in between L_{Fa} and L_{Fb} can be used for system optimization, which also has to keep in mind filtering size, cost, and weight. In our case we use a relation of $L_{Fa} = L_{Fb}/3$ leading to satisfying results. In the practical design the inductor L_{Fa} controls the reverse current peak of the opposite MOSFET during reactive operation.

Detailed simulation results shows, that the losses can be reduced by a factor of more then 6 compared to the standard solution given in Fig. 1 when modern components (CoolMOS, fast diodes) are used. Furthermore the inductive components can be minimized.

3. Simulation of the switching leg

As can be seen in Fig. 7 significant losses due to the distinctive current peaks of a hard-switched low-side

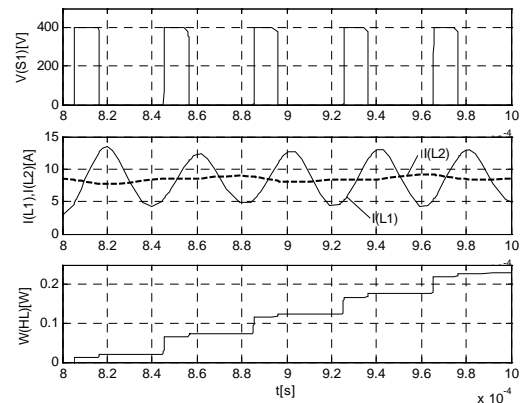


Fig. 7: Switching behaviour of the conventional hard switched power stage (half bridge, $L_1 = L_{F1}, \dots$).

diode in the power MOSFETs during step down operation in conventional half-bridge inverters appear. Contrary to this solution the improved topology according to Fig. 5 leads to a significant reduction of the peak current in the opposite switch leading to a remarkable improvement of the switching losses (Fig. 8).

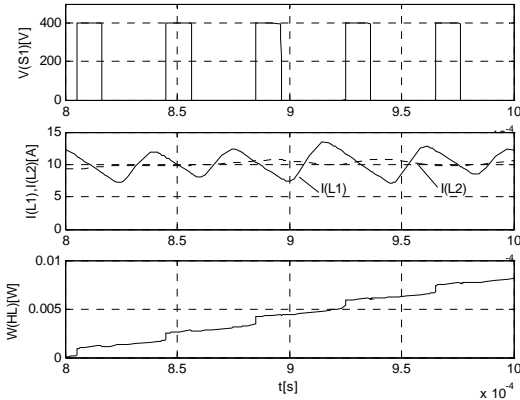


Fig. 8: Switching behaviour of the improved power stage ($L_1 = L_{F1}, \dots$).

As one can see by the comparison of Tables 1 and 2, the system losses can be reduced remarkably.

Table 1: Losses of the conventional full bridge inverter.

d	0.25	0.5	0.75
I_L	10A	20A	30A
d_w	24m	51.5m	70m
S_1	85%	87%	81%
S_2	14%	20%	10%
D	1%	3%	9%

Table 2: Losses of the improved inverter topology.

d	0.25	0.5	0.75
I_L	10A	20A	30A
d_w	2m	5.8m	14.3m
S_1	66%	42%	40%
D_1	6%	4%	13%
S_2	4%	4%	4%
D_2	12%	50%	43%

Simulation results for sinusoidal control (averaging) show a loss reduction by a factor of four. This leads to an enhancement of the inverter efficiency by approximately 2.5% (2kW rated power). Consequently, a reduction of the necessary cooling capacity of about 50W can be achieved resulting in a much more compact and cheaper design.

Figure 9 & 10 depicts the improvement of the switching behaviour in detail. One can see the pronounced current

peaks of the opposite (inactive) power switch in the conventional stage in Fig. 9.

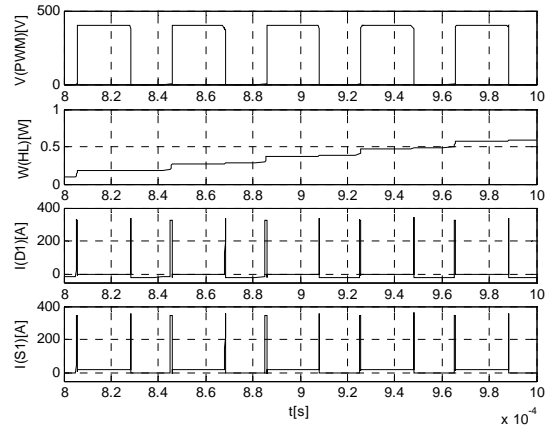


Fig. 9: Switching behaviour of the conventional power stage (half bridge): Output voltage (upper trace), power dissipation in the semiconductors, opposite switch - diode current I_{D1} , current of the active switch S_1 (lower trace).

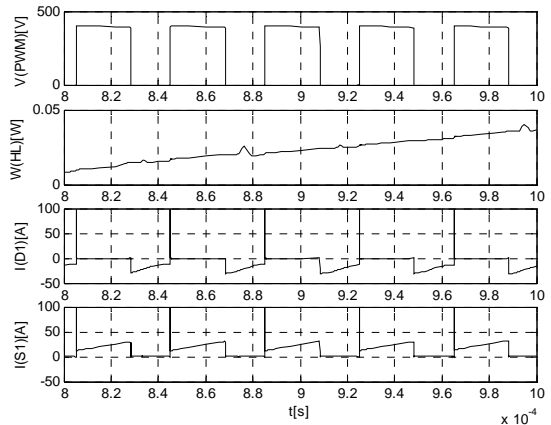


Fig. 10: Switching behaviour of the improved inverter stage: Output voltage (upper trace), power dissipation in the semiconductors, diode current I_{D1} , current of the power switch S_1 (lower trace).

The improved topology uses an optimized diode separated from the MOSFET leading to a remarkable improvement of the switching behaviour.

Potential of additional improvements:

By usage of a non-linear saturation core in case of L_{Fa} the switching characteristics can be further optimized. In this case the fact of the time limited influence of the body diode has been considered. The inductor has to be designed for a defined voltage-time-area. During the

remaining PWM-period it shows less (mostly ohmic insertion losses) influence. This can help to achieve a symmetric operation scheme.

4. The Control of the Inverter

Due to the rather simple topology, the proposed structure is very easy to control. Practical tests show acceptable results with a simple bang-bang dead band controller. Only little additional logic is required to complete the system. To obtain a more silent design and to eliminate unnecessary switching cycles the maximum switching frequency has been limited to 30kHz. This leads to a remarkable reduction of the switching losses and helps to minimize the mains coupling filter.

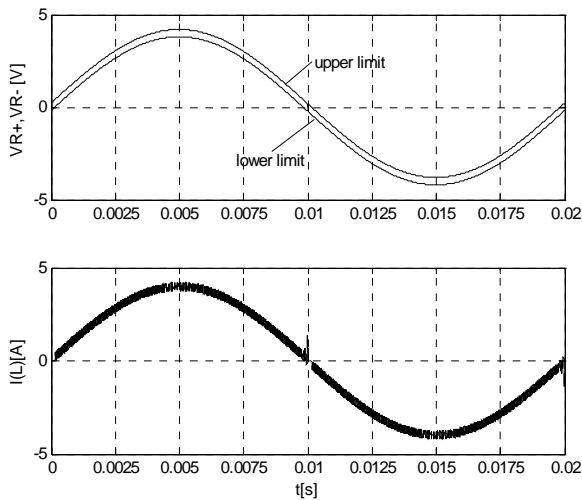


Fig. 11: Simulation results of the bang-bang controller: control voltage band (upper traces), output current (lower trace).

Figure 11 shows the simulation results of the inverter. Here no additional filter is taken into consideration. In practice the coupling filter will lead to a further reduction of the output ripple. The current spike near the zero crossing originates from the very simple control scheme which uses two threshold levels to detect the required output polarity leading to a discontinuous current flow.

In Fig. 12 the harmonics of the DC-link (supply) current of a state-of-the-art switching leg and the proposed topology (c.f. Fig. 5) are compared. One can see the significant reduction of the higher frequency sections (more than a factor of ten). Due to the relationship of current harmonics and resulting EMC-problematic the improvements can be denominated as remarkable.

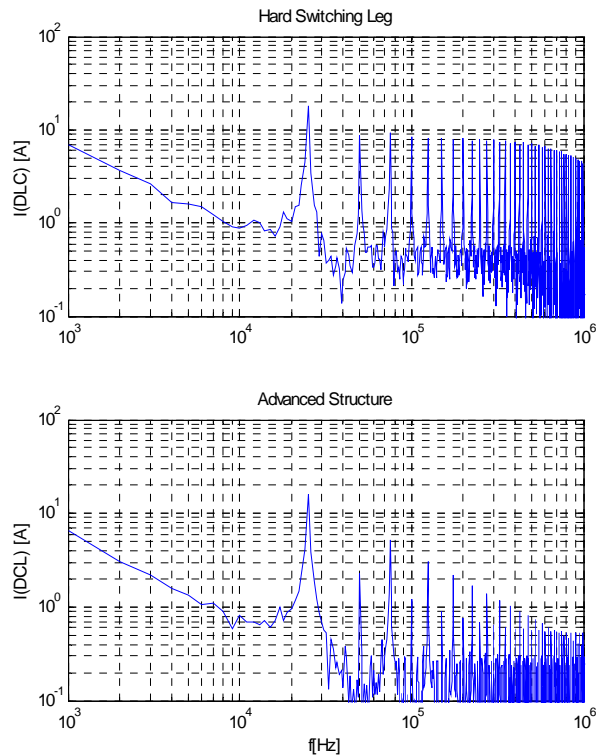


Fig. 12: DC-link current spectrum (EMC) comparison of a conventional topology (upper figure) and the advanced structure (lower figure).

5. Measurement Results

To verify the simulation results given in topic 3 a 2kW inverter stage has been bread boarded. It has been compared to a conventional PWM power stage operating on full bridge topology. Both switching stages are supplied by a 400V DC-link, and are operating at 30kHz. Depending on the operation point the efficiency of the converters has been acquired. Table 3 shows the measurement results.

Table 3: Efficiency comparisons

P_L	100W	200W	500W	1kW	2kW
PWM-Top.	82.1%	85.7%	88.1%	94%	92.8%
Adv. Top.	84.0%	86.1%	88.2%	93.8%	93.2%

The comparison clarifies the improvements resulting from the altered topology. The partly separation of the Buck- and Boost-section of the inverter lead to the given efficiency improvement.

6. Conclusion

The proposed solution improves efficiency as well as EMC characteristics of DC-to-AC power inverters by partly separation of the output current path in the inverter power stage. The proposed separation helps to control the reverse recovery current peak in the opposite switch of the switching leg during the reactive phase. In addition, the efficiency is improved due to the reduction of the turn-on losses. The proposed topology can be used as an alternative to converters formed by several parallel arranged switching branches driven in an interleaved PWM mode in order to enhance the efficiency and to reduce the output voltage ripple.

The power stage of the new topology consists of a simple buck and boost arrangement feeding the mains current. The converter is operated at several 10kHz leading to a tolerable low output current ripple. The maximum peak current of the output stage operating at European mains condition (e.g. 13A for 2kW output power) can be easily handled by modern power semiconductors.

Cheap TO-247 or even TO-220 packages can be used leading to a compact and efficient system design.

The simple control principle of the power stage can easily be implemented using state-of-the-art microcontrollers without additional logic support for the pulse pattern generator; a simple PWM stage fulfills all the requirements. Also the maximum power point tracking for the solar generator can be easily implemented by monitoring the system signals (U_{DCL} and i_M).

Moreover, it should be clearly pointed out that the proposed topology is optimized for grid connected as well as for isolated mains operation. Due to the separated storage inductor only a restricted power factor can be handled which, however, is not a severe limitation for usual practical applications. Simulation show good compatibility with most electrical loads used in practice.

The inverter presented in this paper is a simple and effective solution for small to medium power grid coupled applications. The concept is well suited for wind-, solar- and renewable energy as well as for aerospace applications and for laboratory power amplifiers.

References:

- [1] Hung, J.-C.; Wu, T.-F.; Tsai, J.-Z.; Tsai, C.-T.; Chen, Y.-M.: An active-clamp push-pull converter for battery sourcing applications. Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2005. Volume 2, March 6-10, 2005, pp.1186-1192.
- [2] N. Mohan, T. Undeland, W. Robbins, Power Electronics, New York: John Wiley & Sons, 1995.
- [3] M. Ryan, R. Lorenz, A Synchronous-Frame Controller for a Single-Phase Sine Wave Inverter, Applied Power Electronics Conference APEC '97, pp. 813-819, Atlanta, Georgia
- [4] H. Schmidt, Single Cell Module Integrated Converter (SCMIC), 14th European Photovoltaic Solar Energy Conference, June 30 - July 4, Barcelona, pp. 355-360.
- [5] K. H. Edelmoser, H. Ertl, F. C. Zach, The Optimized Power Switch, Proceedings of the 7th WSEAS International Conference on Circuits, Systems, Communications and Computers CSCC '05, July 11.-16. 2004, Athen, Greece, CD-ROM, ISBN: 960-8457-29-7, 497-540.pdf.