# The Determination of the Bipolar Transistor Commutation Time Components by Using a Virtual Circuit

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A*bstract*. The paper describes a series of theoretical aspects referring to the bipolar transistor commutation mode, the physical parameters having influence over the value of the commutation time and proposes a measuring method for the delay, storage, falling and hoisting times. The commutation time of bipolar transistor components represents the determinant of the memories processing speed.

The proposed method is one at the disposal of students who study the semiconductors, allowing the determination of the commutation time components in order to correlate the microscopic physical parameters of the bipolar transistor (e.g. $\tau$ ) with the macroscopic ones.

*Key-words*. commutation time, carriers lifetime, virtual laboratory.

## 1 Introduction. Problem statement

For the manufacturers of memories, the increase of the computers processing speed implies the creation of memories that include components commutatoring quickly from state 1 to state 0 and vice-versa, replying as fast as possible to the received orders. The research on the level of semiconductor memories is achieved on the level of the memories basic cell, realized on transistors basis, whether they are bipolar or MOS transistors.

The reduction of the commutation time from the active state to the locked state of transistor represents the base of the research referring to the processing speed of semiconductor memories. For improving the transistors commutation time it is required to study the commutation time of the bipolar or unipolar transistor, from *locked state* to *saturated state*, states which are associated to the logical levels 1 and 0.

The temporal parameters related for example to the writing operations within a static RAM are presented in figure 1 (SRAM). The significance of the representation elements is the following [5]:

$t_{AS}$ *– time of preparing the addresses before writing.* All the addressees' inputs should be stable with this time interval before confirming the *CS* and *WE* inputs. Otherwise, the data stored in transit locations may be altered;

$t_{AH}$ *– time of maintaining the addresses after writing.* Analog with $t_{AS}$, all the addressees' inputs should be maintained stable with this time interval after denying one of *CS* or *WE* signals;

$t_{CSW}$ *– time of preparing for the chip selection before closing the writing operation. CS* should be confirmed within at least this time interval before closing the writing cycle so that a certain memory cell can be selected;

$t_{WP}$ *– width of writing pulses. WE* should be confirmed within at least this time interval so that the storage of data in the selected cells latch circuits should be reliable;

$t_{DS}$ *– time of preparing the data of writing operation closing.* All the data inputs should be stable with this time interval before closing the writing cycle. Otherwise, it is possible that data will not be stored in the latch circuits;

$t_{DH}$ *– time of maintaining the data after closing the writing operation.*

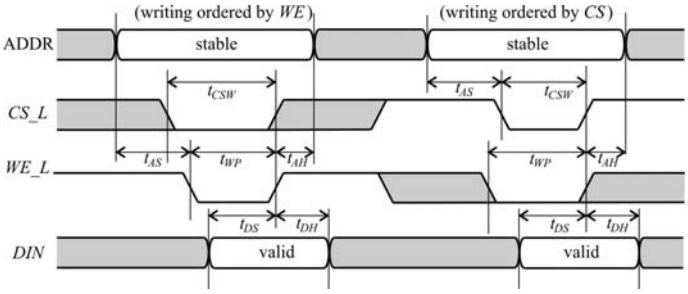


**Figure 1.** Temporal parameters for the writing operations within a static RAM (SRAM).

The commutation time is related to the device specific physical parameters such as lifetime of majority and minority carriers, their mobility and obviously to the sizes of the active zones and chosen manufacturing technologies.

The expression of electrons current density in a type n semiconductor under the influence of an applied electric field *E* is given by the formula:

$$j_n = \frac{e^2 nE}{m_n^*} \cdot \frac{\int_0^\infty W^{3/2} \cdot \tau_n(W)\, \mathrm{e}^{-W/k_0 T}\, \mathrm{d}W}{\int_0^\infty W^{3/2} \mathrm{e}^{-W/k_0 T}\, \mathrm{d}W}, \qquad (1)$$

where:

$\tau_n(W)$ - lifetime of electrons;

$e$ – electron charge;

$n$ – number of electrons participating in carry;

$E$ – applied electric field;

W - electron energy;

$k_0$ - Boltzmann constant;

d$W$ – variation of electron energy.

By replacing the ratio of the two integrals with $\langle \tau_n \rangle$ representing the mediate value of the electrons lifetime,

$$\langle \tau_n \rangle = \frac{\int_0^\infty \tau_n(W) W^{3/2}\, \mathrm{e}^{-W/k_0 T}\, \mathrm{d}W}{\int_0^\infty W^{3/2} \mathrm{e}^{-W/k_0 T}\, \mathrm{d}W}, \qquad (2)$$

the expression of electrons current density may be written:

$$j_n = \frac{e^2 n \langle \tau \rangle E}{m_n^*}. \qquad (3)$$

where $m_n^*$ is the effectivness mass of electrons [1].

The above relations are valid if it is considered that the isoenergetic areas are spherical. For using the formulas obtained for $j_n$ it is necessary to establish the dependency of $\tau_n$ to energy and to make the corresponding averaging according to the semiconductor dispersal mechanisms, but these are aspects not covered by this paper [1].

On macroscopic level, in discrete semiconductor devices the current density is not measured, but determined based on measuring some macroscopic parameters, such as collector, basic or emitter currents, residual currents in a bipolar transistor.

## 2 Presentation bipolar transistor commutation mode

The transistor commutation mode means a dynamic mode in which the transistor is working *alternatively saturated-locked* when a pulses form signal is applied on its log in.

Under locking state both bipolar transistor junctions (base-emitter junction and the base-collector one) are reversely polarized and only emitter-base and collector-base ($I_{CE0}$ and $I_{CB0}$) residual currents are flowing through transistor; these are very low and didactically can be neglected.

Under conductibility state, the transistor has direct polarized emitter-base junction while the collector-base junction is either locked (in case of operating in the active area) or direct polarized (in case of operating on saturation).

Figure 2 shows the diagram of an *EC* connection commutator in created with a bipolar transistor $n-p-n$.

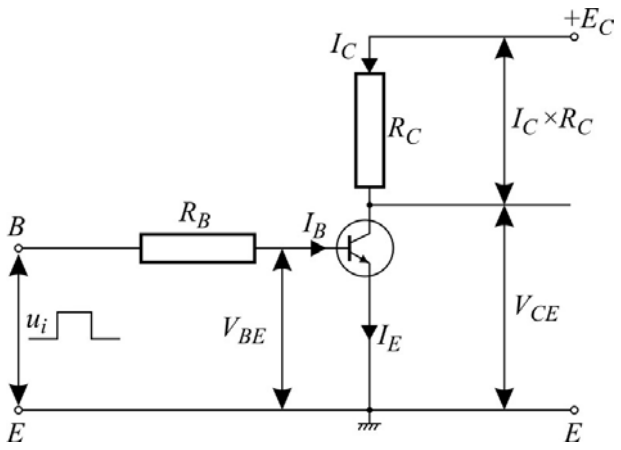


**Figure 2.** Diagram of EC connection commutator with a transistor $n-p-n$

The power failures on each junction and the currents are represented in the figure.

Figure 3 presents the family of output characteristics and the load line of this commutator, of which ends are characterized by:

$$\begin{aligned} &S: \quad V_{CE} = 0 \qquad I_C = \frac{V_{CC}}{R_C} \\ &B: \quad I_C = 0 \qquad V_{CE} = V_{CC}. \end{aligned} \qquad (4)$$

Considering the circuit from figure 2, the supply voltage $V_{CC}$ is divided on $R_C$ and on transistor, between collector and emitter, according to relation:

$$V_{CC} = R_C I_C + V_{CE}. \qquad (5)$$

The transistor *locking* is characterized by the load line in operating point *B,* where the collector current has value 0 ($I_C = 0$) and $V_{CE} = V_{CC}$, while a static operating

point $S$ corresponds to the transistor *saturation*. The transistor saturation is obtained by infusing a minimum base current $I_{BS\,\min}$, called *Base current on incipient saturation.*

A proportional current to this saturation current is obtained in collector, $I_{CS}$ :

$$I_{CS} = \beta I_{BS\ \min}. \qquad (6)$$

A current $I_{BS} > I_{BS\,\min}$ is applied in practice, while the collector current can not increase and then:

$$I_{CS} < \beta I_{BS}. \qquad (6')$$

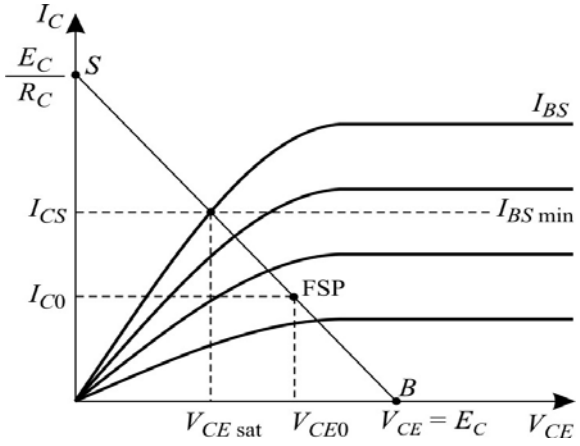


**Figure 3.** Family of output characteristics and relieving the commutation of the operating static point between locked and saturated

It is considered that the transistor is an efficient commutator if a pulse (voltage) is applied on base, making the rapid passing of the operating point from B (the logical state 0) up to $S$ (logical state 1), without transistor maintaining in the active zone (of amplification).

In figure 4, there are represented the applied input voltage pulse (a) and respectively the current one (b) as well as the time variation mode of the collector $I_C$ by relieving the commutation times (direct and reverse) (c).

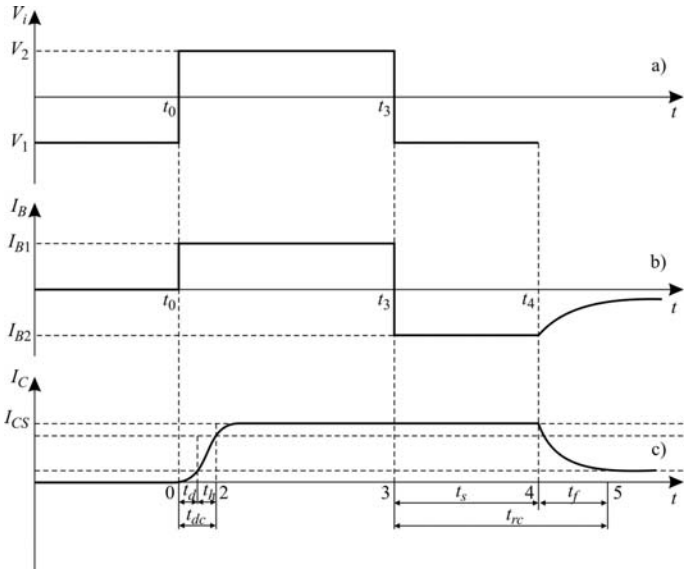


**Figure 4.** The applied input voltage pulse (a), the current pulse on transistor in commutation mode (b), variation way of current $I_C$ by relieving the commutation times (direct and reverse) (c)

## 3 The components of commutation time

It is known that the transistor commutation time is determined by the transition processes related to the displacements of the basic carriers and accumulation of loads infused in base.

It is considered that before moment $t_0$ the transistor is locked by the value $V_1$ of the input signal $V_i$ applied on base. A transition of input voltage takes place from value $V_1$ to positive value $V_2$, followed promptly by the transition of the base current from 0 to $I_{B1} > I_{BS}$.

Due to the fact that the carriers, infused rapidly by emitter in base, need time to reach the collector, the current $I_C$ will be maintained at value 0 for a ***delay time***, noted $t_{d,}$ after which is increasing to the stationary value $I_{CS}$. The time in which the current increases from 0,1 $I_{CS}$ to 0,9 $I_{CS}$ is called ***hoisting time*** and is noted with $t_h$ (or rise time).

The time which passed from the moment when the saturation order has been applied ($t_0$) until the collector current reached 0,9 of the maximum value is called ***direct commutation time*** $t_{dc}$ and is formed by the delay time and the hoisting time according to relation:

$$t_{dc} = t_d + t_h. \qquad (7)$$

The delay time ($t_d$) is usually insignificant in regard with the hoisting time, so that the relation 4.2.3 may be written:

$$t_{dc} = t_h = 2{,}3\tau_n = \tau_n \ln \frac{1}{1 - \frac{0{,}9 I_{CS}}{I_{B1}}}, \qquad (8)$$

where $\tau_n$ is the lifetime of electrons in the transistor base.

Still, if the input signal decreases rapidly on the moment $t_3$ from the positive value $V_2$ to the negative value $V_1$, the base current will tend to rapid decreasing as well from value $I_{B1}$ to $I_{B2,}$ changing its direction.

The role of the resistance $R_B$ is to limit the base current to the value $I_{B2}$ and to protect in this way the base-emitter junction.

The excess of the load stored in base will make $I_{CS}$ to be further maintained for a time called ***storage*** time, noted $t_s$, after which this starts to decrease. The storage time is given by relation:

$$t_s = \tau_s \ln \frac{I_{B1} + I_{B2}}{I_{CS} + I_{B2}}, \qquad (9)$$

where $\tau_s$ is the storage time constant of the electrons in base.

At moment $t_4$ the transistor is outgoing from saturation state and the operating point will move from $S$ to $B$, in a time called ***falling time***, noted $t_f$. This time is defined as the time in which the collector current decreases from value $I_{CS}$ to 0,1 $I_{CS}$ and is expressed by:

$$t_f = \tau_n \ln\left(1 + \frac{I_{CS}}{I_{B2}}\right). \qquad (10)$$

***The reverse commutation time*** ($t_{rc}$) is the time interval from the moment of applying the locking order until when the collector current decreases from 0,1 of its maximum value and is formed by the storage time and the falling time:

$$t_{rc} = t_s + t_f. \qquad (11)$$

If it is considered that $\tau_n = \tau_s$, the reverse commutation time can be written:

$$t_{rc} = \tau_n \ln\left(1 + \frac{I_{B1}}{I_{B2}}\right). \qquad (12)$$

***The total commutation time*** of transistor is given by the sum between the direct commutation time and the reverse commutation one:

$$t = t_{dc} + t_{rc} = t_d + t_h + t_s + t_f. \qquad (13)$$

In general, the reverse commutation time is higher than the direct commutation one, the essential difference being given by the storage time, which has the highest value among all the components of the commutation time.

In order to create transistors with low commutation times utilized in semiconductor memories it is searching to reduce the storage time by avoiding the ingress of the device under deep saturation mode; transistors $n - p - n$ are preferred, in which the operating carriers are the electrons having higher mobility than the no-loads and commutation acceleration diagrams are used.

## 4. Measurement of commutation time by using a virtual circuit

The required circuit is created by using the program *Circuit Maker*. The ***Circuit Maker*** program***, Student variant***, is available free of charge on the Internet and can be utilized by students for study in a virtual laboratory [2,3,4] for creating an electronic circuit with passive, active (analogical or digital) elements, signal sources (continuous, alternative, various forms pulses etc.), for modifying an existent circuit, analyzing some output signals (or in certain points of the complex circuits), according to the input signals or other circuit parameters, of time and direct capture of images on the monitor screen etc.

A measuring circuit is presented in figure 5 as exemplification, which allows the measurement of the commutation time for a bipolar transistor $n - p - n$. This transistor may be of any type and comparative determinations can be done on several types of transistors.

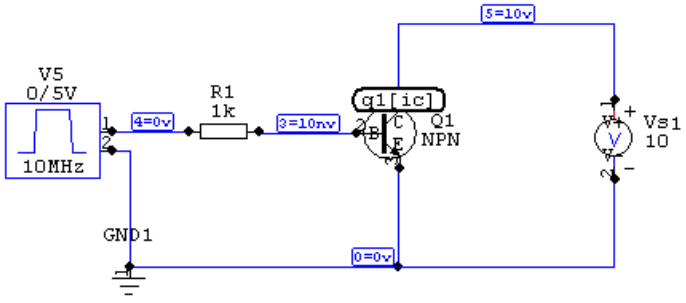


**Figure 5.** Laboratory circuit for measuring the commutation time of a bipolar transistor

The proposed working method was the following [2]

**a)** Supplying the circuit with $V_{CC} = 10$ V. Applying on input positive voltage pulses $V_g = 5$ V with period of 10 μs order.

**b)** Visualizing *the collector current according to time* $I_C = f(t)$ by positioning the measuring tester in the transistor's collector until sign A appears on tester. Adjusting the time and collector current variation ranges until a significant difference (of time) can be noticed for the passing of current from value 0 to maximum value and vice-versa. Such characteristic is presented in figure 6.

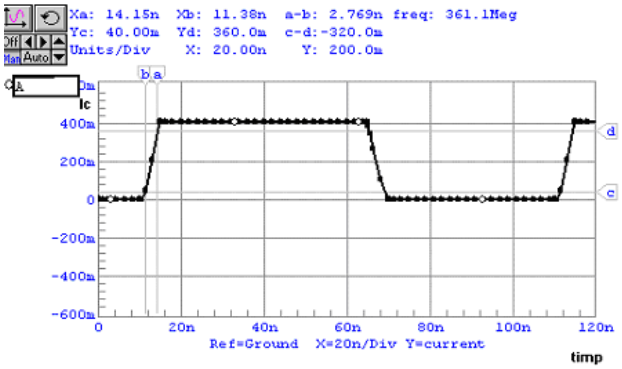


**Figure 6**. Dependency of time output current: detail for measurement of commutation times

**c)** Measuring the current value at saturation on the obtained characteristic. Calculating then the values corresponding to 0,1 $I_{CS}$ and respectively 0,9 $I_{CS}$. Positioning the two cursors, c and d, on the two calculated values as shown in figure 6.

Positioning then one of the vertical cursors (cursor b in figure) on the minimum value of the collector current, measuring the time values on the OX axis correspondingly, and the other vertical cursor, in point corresponding to 0,9 $I_{CS}$, on the characteristic ascending inclination. Reading the value of the direct commutation.

**c)** Proceeding similarly for measuring the falling (falling) time, of reverse commutation, according to the things presented in the theoretical part of this paper, by measuring the difference between the time corresponding to the collector current maximum value and the value 0,1 $I_{CS}$, on the descending inclination.

The value of the average lifetime of carriers in base can be calculated by using the relation 7.

The circuit can be modified for another type of transistor which is selected from the library of program components. A series of small adjustments of the existent circuit are required and the direct and reverse commutation times can be measured similarly.

A similar circuit can be realized also for relieving the commutation of flip-flop circuits realized with transistors (bipolar or MOS) forming part of semiconductor memories. Output signals obtained in laboratory for a flip-flop circuits are presented in figure 7. Both overlapped outputs for the studied circuit are represented and the perfect balance of both signals can be noticed.

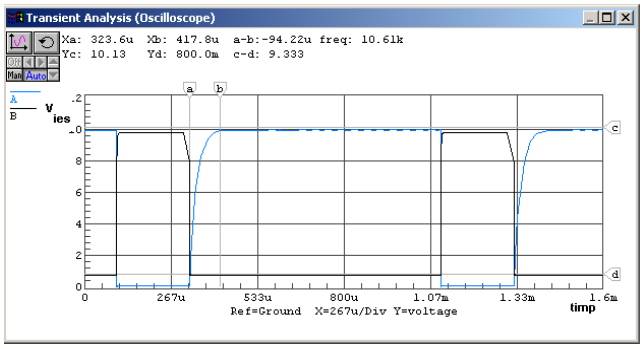


**Figure 7.** Output signals obtained in virtual laboratory for a flip-flop circuit

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