Study of Matching Errors in Unit Element Approach of Current-Steering Segmented DAC Design

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Abstract: - In this paper we aim to optimize the splitting of the input control code of a current-steering segmented digital-to-analog converter which uses identical unit current sources only. Both matching error and area are taken into discussion to analyze the static and dynamic performances of the converter. Power consumption considerations are presented and the final optimized code segmentation will be offered for a 10-b 0.35-μm CMOS DAC included in a sub-bandgap mechanism.

*Keywords:*Current-steering DAC, segmented DAC, unit current source, matching error, sub-bandgap reference.

1 Introduction

In the current-steering DACs design the unit element approach leads to a regular layout where special layout techniques can be used to reduce the effect of matching errors [1], [2]. Furthermore, in order to obtain a better dynamic performance, especially regarding SFDR, the dynamic randomization of the unit current sources or dynamic element matching (DEM) has been intensively studied and implemented. Thus, the matching errors become signal-independent and the linearity of the converter is significantly improved. Consequently, switching-sequence mapping algorithms have been recently developed and used in both Nyquist-rate data conversion, [2], [3] and oversampling-rate data conversion [4].

Very interesting segmented architectures of current-steering digital-to-analog converters were presented in [2], [5] and [6], but there the dynamic randomization is made at most inside each segment of the code because the current sources are not identical over the segments. Typically, the full-randomization techniques are used in lower-bit DACs and for example in the feedback DACs in sigma-delta ADCs [2], [4]. Only few works [2], [3] discuss or implement the full randomization, but there the number of input bits is still limited.

However, the current-steering segmented DAC proposed in [7] allows the implementation of the full randomization because both segments control identical current-source blocks. Moreover, this converter presents very good immunity to the switching activity. The feature is extremely important because it is known that the randomization techniques, for the thermometer case, basically destroy the low-glitch properties.

So, in section 2 of the paper we will present briefly the principle of the converter described in [7] and in section 3 we will determine, theoretically and by simulation, the influence of matching errors in the standard deviation σ of the maximum output voltage of the converter. Our approach will follow the Pelgrom's rules [8], sustained and confirmed over the years [9], especially regarding the mismatch-generating process caused by the short correlation distance. This means that the distance between events which cause mismatch (local mobility fluctuation, oxide granularity, etc.) is much smaller than the transistor dimensions and the transistors are located close to each other. Many known processes present in first order this behavior.

The mismatch-generating process caused by the long correlation distance (the matching is dependent of the distance between transistors over the wafer and originates from wafer fabrication and oxidation process) is a deterministic process, but, as the original placement of dies on a wafer is unknown after packaging it is modeled as an additional stochastic process, [8] and its parameters can be included in the process specification parameters which characterize the first type of behavior.

In section 4 a more general analysis, for different segmentations of the input code, will be presented. Both matching error and area will be considered to analyze the performances of the converter. Power consumption features are estimated and the final optimized code segmentation will be offered for a 10-b 0.35-μm CMOS DAC.

Section 5 will conclude the paper.

2 Current-Steering DAC Overlapping the Sub-Bandgap Reference

As it was shown in [7] the sub-bandgap reference taken into consideration allows us to obtain a current independent of temperature which is mirrored in the last branch of the circuit and injected in the resistor R_3 (see fig.1). The way to obtain a 10-b segmented digital-to-analog converter is to mirror the output current of the reference in $2\times(2^5-1)$ branches (grouped on two identical blocks) through which the currents are switched or not towards the resistors R_8 and R_9 connected as in fig.2. In each block the unit current sources are controlled by 5 switches in such a way that the LSB will control a single unit current source, the next will control two unit current sources, while the MSB of each segment will control 2^{5-1} unit current sources. For simplicity, we omitted from fig.2 the switches located in the drain of pMOS transistors and the complementary current outputs too. In order to ensure the weighting of 2^5:1 in the output voltage contribution the ratio of resistor values R_9 and R_8 must be 2^5-1. The number of transistors used as unit current sources is 62 instead of 1023 if no segmentation is performed.

Of course this converter was conceived in order to be controlled by a modified digital input according to DEM techniques, case in which each unit current source will be controlled by a switch.

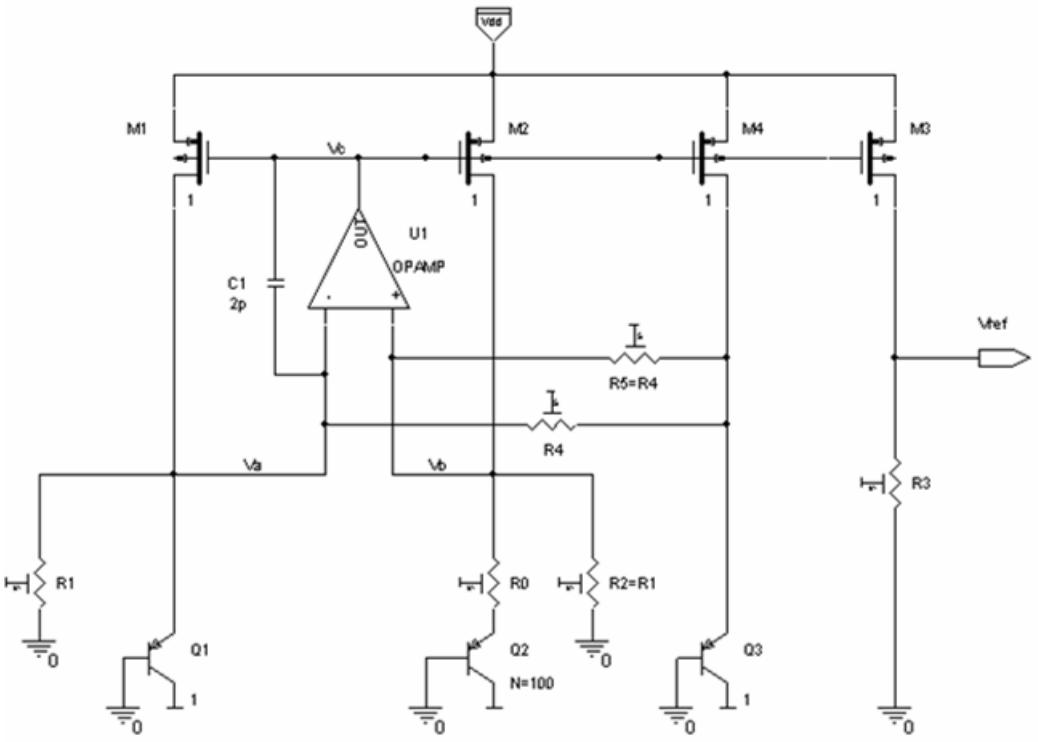

Fig.1 Sub-bandgap voltage reference with curvature compensation

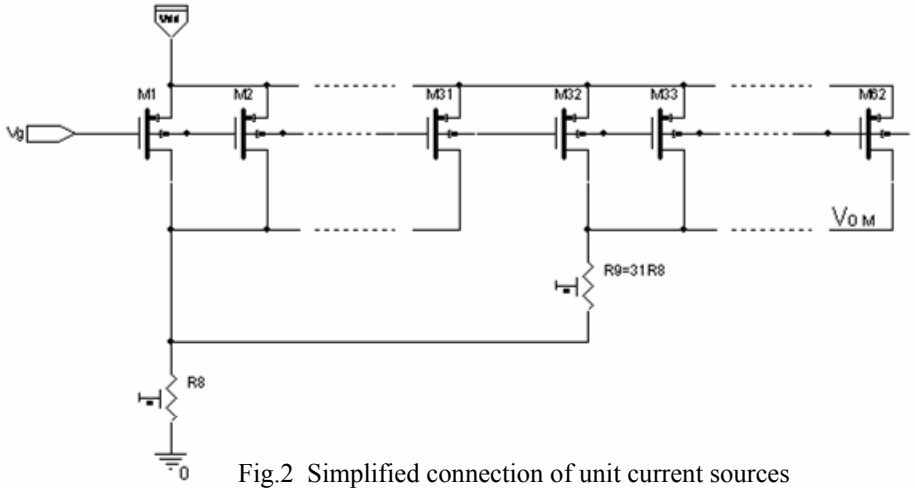

Fig.2 Simplified connection of unit current sources

3 Standard deviation of the maximum output voltage

Our purpose is to calculate and verify by simulation the standard deviation σ_M of the maximum output voltage V_{oM} of the converter presented in section 2, corresponding to the maximum digital input code. In this most unfavorable case all the unit current sources will inject currents trough the resistors R_8 and R_9 and all transistors will statistically contribute with matching errors to the expected value of the output voltage. This gives us important information regarding the integral nonlinearity of the DAC.

First, we calculate the standard deviation σ_o of the smallest output voltage of the converter, V_{o_u}, corresponding to its resolution, when only the LSB of the input code is set to 1. This situation is presented in fig.3. Then, based on the manner in which the maximum output voltage is obtained, and by using the properties of the normal distributions, we calculate σ_M.

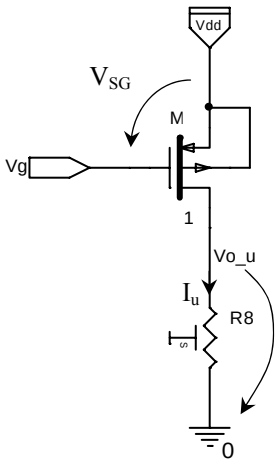

Fig.3 Unit current source controlled by the LSB

The unit current source is realized with a pMOS transistor whose control voltage V_{SG} is supplied by the sub-bandgap mechanism. The aspect ratio of the transistor is W/L. The dimensions of the resistor R_8 are W_{R8} and L_{R8} respectively. For simplicity, we omitted from fig.3 the switch located in the transistor drain and the complementary output too. Then, V_{o_u} is:

$$V_{o\_u} = I_u \cdot R_8, \quad (1)$$

where I_u is the current of the transistor working in the saturation region :

$$I_u = \frac{\beta_u}{2}(V_{SG} - V_{th})^2, \quad (2)$$

where β_u is the transconductance parameter and V_{th} is the treshold voltage. Differentiating (2) and combining with equation (2) we obtain the absolute error of the unit current[2] :

$$\Delta I_u = \Delta\beta_u \cdot \frac{I_u}{\beta_u} - \Delta V_{th} \cdot \frac{2I_u}{V_{SG} - V_{th}}. \quad (3)$$

Further, differentiating equation (1) and using equation (3), we can find, after normalization, the relative error of the output voltage :

$$\frac{\Delta V_{o\_u}}{V_{o\_u}} = \frac{\Delta\beta_u}{\beta_u} - \frac{2}{V_{SG} - V_{th}} \cdot \Delta V_{th} + \frac{\Delta R_8}{R_8}. \quad (4)$$

Considering that β_u, V_{th} and R_8 follow normal distributions, we can write [8]:

$$\sigma^2\left(\frac{\Delta\beta_u}{\beta_u}\right) = \frac{A_\beta^2}{WL}; \quad \sigma^2(\Delta V_{th}) = \frac{A_{VT}^2}{WL};$$

$$\sigma^2\left(\frac{\Delta R_8}{R_8}\right) = \frac{A_R^2}{W_{R8}L_{R8}}. \quad (5)$$

Equations (5) give us the variances of β_u, V_{th} and R_8 depending on the process parameters A_β, A_{VT} and A_R (Pelgrom coefficients) and on the area of the devices.

Because β_u, V_{th} and R_8 are mutually independent, the variance of the output-voltage relative error is:

$$\sigma^2\left(\frac{\Delta V_{o\_u}}{V_{o\_u}}\right) = \frac{A_\beta^2}{WL} + \frac{4}{(V_{SG} - V_{th})^2} \cdot \frac{A_{VT}^2}{WL} + \frac{A_R^2}{W_{R8}L_{R8}}. \quad (6)$$

Now, we can deduce the practical formula which gives us the standard deviation $\sigma_0 = \sigma(\Delta V_{o\_u})$:

$$\sigma_0 = V_{o\_u}\left(\frac{A_\beta^2}{WL} + \frac{2\beta_u' \frac{W}{L} R_8}{V_{o\_u}} \cdot \frac{A_{VT}^2}{WL} + \frac{A_R^2}{W_{R8}L_{R8}}\right)^{\frac{1}{2}} \quad (7)$$

where β_u' is the process transconductance and V_{o_u} is the resolution of the DAC. Because V_{o_u} can be regarded as a sub-bandgap voltage, according to [7], R_1 from fig.1 and R_8 satisfy the equation:

$$\frac{R_1}{R_8} = \frac{V_{BG}}{V_{o\_u}} \cdot \frac{(W/L)_{unit\_current\_sources}}{(W/L)_{sub-bandgap}}. \quad (8)$$

where V_{BG} is the band-gap voltage and $(W/L)_{sub\_bandgap}$ is the aspect ratio of the pMOS transistors from fig.1. The design specifications of the sub-bandgap reference can be found in [7].

In our design we adopted V_{o_u}=0.5mV, R_8=85Ω, W/L=250u/25u and $W_{R8} \cdot L_{R8}$=2W·L. From our process specification (***0.35μm CMOS) we have: A_β=1,13 %·μm, A_{VT}=10,87 mV·μm, A_R =6,7%·μm and β_u'=67,4 μA/V^2. Thus, we obtain the standard deviation σ_0 :

σ_o=0,5mV×10^{-3}×$(0.02+4.33+0.36)^{0.5}$≅1.085μV. (9)

We observe, as in the conclusions formulated in [8] that the predominant term in the square root is the second one (if the resistor area is at least twice the transistor area) and this means that the main cause of the matching errors is the variation of the oxide thickness which modify the threshold voltage of the pMOS transistor.

Further, the maximum output voltage of the converter V_{oM} is the voltage across the resistors R_8 and R_9 (fig.2):

$$V_{oM} = \sum_{j=1}^{62} I_{uj} R_8 + \sum_{k=32}^{62} I_{uk} R_9 \,. \qquad (10)$$

Bearing in mind that R_9=31R_8, to keep low the third term in the square root of the calculation (9) we must build R_9 with unit resistors with equal area of R_8. In this way V_{oM} becomes:

$$V_{oM} = \sum_{j=1}^{62} I_{uj} R_8 + \sum_{k=32}^{62} \left(I_{uk} \sum_{i=1}^{31} R_{8i} \right) \cong$$

$$\cong \sum_{j=1}^{62} I_{uj} R_8 + \sum_{k=32}^{62} \left(I_{uk} 31 R_8 \right) = \qquad (11)$$

$$= \sum_{j=1}^{62} V_{oMj} + \sum_{k=32}^{62} \left(31 V_{oMk} \right)$$

and all the 62+31 terms are mutually independent. It is known that the variance of the sum of terms with normal distribution is the sum of the variances of each term and, more important, the variance of the product of a positive number with a term with normal distribution is given by the product of the number square with the variance of the term. Thus, the variance of the maximum output voltage becomes:

$$\sigma_M^2 = 62\sigma_o^2 + 31 \cdot 31^2 \sigma_o^2 = 29853\sigma_o^2 , \quad \text{and}$$

consequently the standard deviation of V_{oM} is:

$\sigma_M \cong 173\,\sigma_o$ =0.187mV.

The whole converter was designed (for n=10) and simulated using the OrCAD program and a library including PSPICE models of the 0.35μm CMOS technology. Special parameters were included in the PSPICE models of the pMOS transistors (as in the case of the default resistor tolerance) which allowed the Monte Carlo analysis using these active components with stochastic matching. The Monte Carlo analysis included 200 runs and the simulation results are presented in fig.4.

As we can observe in fig.4, the standard deviation σ of the maximum output voltage is 0.18mV, so it is very close of the calculated value. In roughly 85% of cases (of chips) the maximum deviation of the output voltage is under half of the DAC resolution. 3σ is 0.54mV i.e. in 99,7% of cases the maximum output voltage deviation is roughly under its resolution (<0.5mV). The expected value of the Vout is 511.57mV instead of 511.5mV.

4 Study of matching errors for different code segmentations

In this section we will analyze the effect of the modification of the code segmentation. We consider a converter with N bits, out of which N_{LS} bits for the less significant segment and N_{MS}=N- N_{LS} bits for the most significant segment. We obtain the maximum output voltage of the converter by using the same

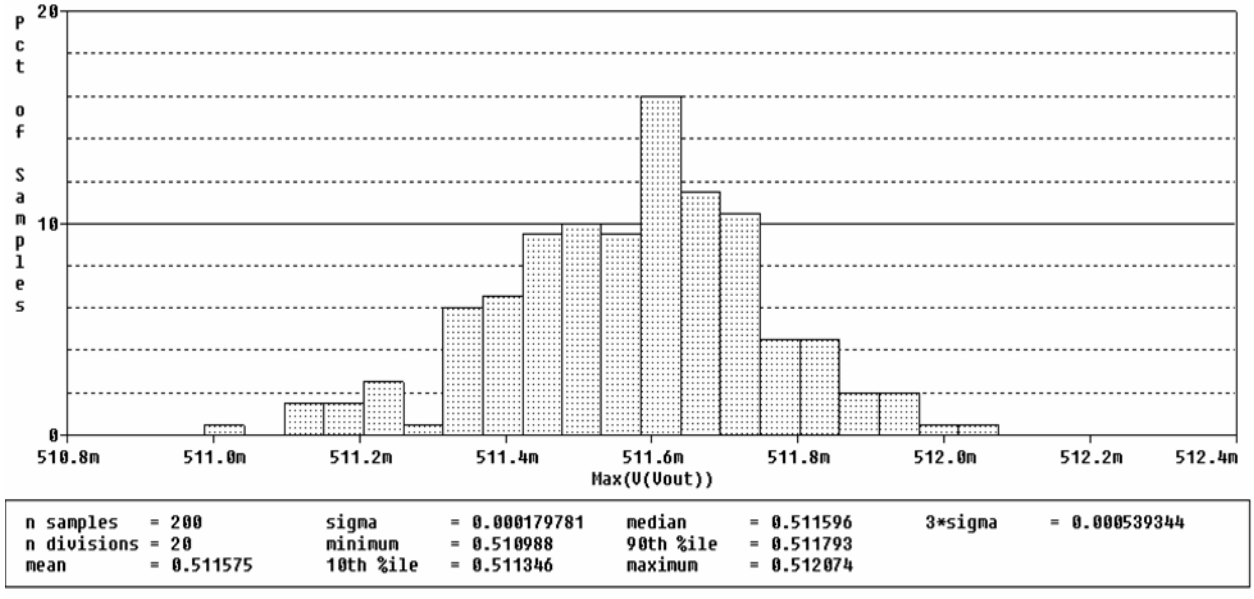

Fig.4 Results of the Monte Carlo simulation of the DAC

arrangement of terms as in equation (11):

$$V_{oM} = \left(2^N - 1\right)V_{o\_u} = \\ = \left[\left(2^{N_{LS}} - 1\right) + \left(2^{N-N_{LS}} - 1\right)\right]V_{o\_u} + \\ + \left(2^{N-N_{LS}} - 1\right)\left[\left(2^{N_{LS}} - 1\right)V_{o\_u}\right] \quad (12)$$

and we used N_{tr} pMOS transistors:

$$N_{tr} = \left(2^{N_{LS}} - 1\right) + \left(2^{N-N_{LS}} - 1\right), \quad (13)$$

and N_{res} unit resistors:

$$N_{res} = 2^{N_{LS}}. \quad (14)$$

In the special case in which N_{LS}=N, then $2^N - 1$ unit resistors become open-circuit and N_{res}=1.

Following the same approach as in the previous section, the variance of the maximum output voltage will be:

$$\sigma_{oM}^2 = \left[\left(2^{N_{LS}} - 1\right) + \left(2^{N-N_{LS}} - 1\right)\right]\sigma_o^2 + \\ + \left(2^{N-N_{LS}} - 1\right)\left(2^{N_{LS}} - 1\right)^2 \sigma_o^2 \quad (15)$$

If N_{LS}=0, or N_{LS}=N we have no segmentation.

For N=10 and different values of N_{LS} we calculated σ_{oM}, $3\sigma_{oM}$, N_{tr} and N_{res}. We verified σ_{oM} and $3\sigma_{oM}$ by simulation and the results were very close to the calculated values. These results are synthesized in Table 1. In the last but one column the number of generic unit elements $N_u=N_{tr}+2N_{res}$ is done.

Table 1

N_{LS}	σ_{oM} [mV]	$3\sigma_{oM}$ [mV]	N_{tr}	N_{res}	N_u	A_Z
0	0,034	0,102	1023	1	1025	4.8
1						
2	0,052	0,156	258	4	266	0.73
3	0,086	0.26	134	8	150	0.587
4	0,13	0.39	78	16	110	0.571
5	0,18	0.54	62	32	126	1
6	0.265	0.795	78	64	186	4
7	0.363	1.09	134	128		
8						
9						
10	0,033	0,1	1023	1	1025	

To establish a criteria of comparison between the different segmentations we first considered the segmentation with N_{LS}=5 as reference design with a normalized area A_Z of 1 relative unit, and with a power budget in static conditions determined by the sum of all unit currents of the reference design. Then we impose to the other segmented architectures to have the same power consumption. By examining the equation (7) we observe how the modification of the current $I_u = V_{0\_u}/R_8$ produces a new standard deviation value. Further, we modify the device area W·L in such a way that σ_0 changes from the last value to that corresponding to the reference design. The product of the new device area with the number of unit element in the segmented architecture, expressed in relative units, will tell us what design needs the smallest area for the same performances in precision and power consumption. The computed results of this algorithm can be found in the last column of Table 1. We observe that from the point of view of the adopted performance criteria the best segmented architectures correspond to N_{LS}=4 and N_{LS}=3. But, for the reason of the complexity of the switching circuitry needed for the implementation of the dynamic randomization techniques we can say that the best variant correspond to N_{LS}=4 because it uses the smallest number of transistors which must be switched.

5 Conclusions

In this paper we optimized the splitting of the input control code of a current-steering segmented digital-to-analog converter which uses identical unit current sources only. The analysis of matching errors, area and power consumption led to an optimum segmentation of a 10-bit DAC with N_{LS}=4 and N_{MS}=6. The converter allows the implementation of the full dinamic randomization and presents a very good imunity to the switching activity involved in DEM techniques.

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