New Polymorphic NAND/XOR Gate

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Abstract: - Polymorphic digital circuits are circuits composed of polymorphic (multifunctional) as well as ordinary gates. In addition to its standard logic function (such as NAND), a polymorphic gate exhibits another logic function which is activated under a specific condition, for example, when Vdd, temperature, illumination or a special signal reaches a certain level. This paper describes newly proposed two-input gate for polymorphic circuit. The gate produces NAND or XOR function according to a special signal. The proposed gate is effective in terms of area overhead – it consists of 9 transistors only, while corresponding circuit employing conventional gates consists of more than 10 transistors.

Key-Words: hardware engineering, digital circuits, CMOS logic gates, polymorphic electronics, VLSI, reconfigurable digital circuits

1 Introduction

Polymorphic digital circuits are circuits composed of polymorphic (multifunctional) gates. In addition to its standard function (e.g. NAND), a polymorphic gate exhibits another logic function (e.g. NOR) which is activated under a specific condition, for example, when Vdd, temperature or a special signal reaches a certain level. The concept of polymorphic gates was proposed by Stoica et al [1]. Polymorphic gates are able to perform one or more additional functions in addition to the "main" function of the circuit. A function change does not require switches/reconfiguration as in traditional approaches. Instead, the change comes from modifications in the characteristics of devices involved in the circuit (mainly transistor operation point), in response to controls such as temperature, power supply voltage (Vdd), control signals, light, etc. The structure of the circuit remains the same. For example, NAND/NOR gate was proposed which operates as NAND when Vdd = 3.3V and as NOR when Vdd = 1.8V. It consists of 6 transistors connected in an unconventional structure [2]. In theory, it could be possible to build a polymorphic gate that implements k different logic functions in k different environments. Practically, k is 2 or 3 nowadays.

Research papers indicate many areas in which polymorphic gates could be utilized. The following list provides some examples (see a thorough analysis in [1, 3]):

• The automatic control of power consumption when battery voltage decreases (a circuit realizes another function for lower battery voltage; however, its structure remains unchanged).
• Implementation of a hidden function, invisible to the user, which can be activated in a specific environment (e.g. watermarking at the hardware level).
• Intelligent sensors for biometrics, robotics, industrial measurement, etc.
• Reverse engineering protection.
• Implementation of low-cost adaptive systems that are able to adjust the behavior inherently.

There are two main problems in polymorphic circuit design:

1. design of generally usable polymorphic gates as building blocks of digital polymorphic circuits and
2. suitable and efficient design techniques for design of digital polymorphic circuits.

Considering polymorphic gates as building blocks offers an opportunity to design digital polymorphic circuit at gate level. Almost all existing circuits [6,7,8] were designed by some unconventional design techniques such as evolvable hardware [5] etc. So solution of the 2nd problem is still under research. This paper proposes contribution to the solution of the 1st problem. Note that no circuits more complex than a single gate have been reported that are designed at the transistor level.

The paper is organized as follows: Section II. presents known and published polymorphic gates, its advantages and disadvantages, section III. describes newly proposed polymorphic NAND/XOR gate, in section IV., results of simulation of the gate is presented. Section V. shows some example of the gate utilization and section VI. concludes the paper.

Table 1 - Published Polymorphic Gates

Gate	Conditions of Function Change	No. of Transistors	Published In
AND/OR	27/125°C Temperature	6	[3]
AND/OR/XOR	3.3/0.0/1.5V External signal	10	[3]
AND/OR	3.3/0.0V External signal	6	[1]
NAND/NOR/XOR/AND	0.0/0.9/1.1/1.8V External signal	11	[4]
AND/OR	1.2/3.3V – Vdd	8	[3]
NAND/NOR	3.3/1.8V – Vdd	6 (fabricated)	[2]

2 Known Polymorphic Gates

In the recent years, several polymorphic gates have been discovered. Table I shows existing polymorphic gates. Practically all of them are proposed by authors of polymorphic electronics approach – Adrian Stoica, Ricardo Zebulum and Didier Keymeulen from NASA JPL. These gates are designed by evolutionary approach, some of them in FPTA.

Lot of these gates has very unconventional structure - for example, see Fig. 1. The NAND/NOR gate shown in this figure is probably the most famous example of a polymorphic gate. This gate and also practically all gates shown in the Table 1 permits low transistor count (note that the common NAND and NOR gates cost 4 transistors, the XOR gate can be implemented using 6-10 transistors and 2 transistors are needed to create the inverter in the standard CMOS technology) but their structure brings some problems such as weak output logic levels, higher power consumption and lower input impedance. Some of gates from Table 1 were simulated and results were not very satisfactory. Furthermore, lots of them are also strongly dependent on used technology (predominantly HP 0.35 micron) and parameters of transistors. It can be one of reasons why simulations were not too successful.

Note that for example AND/OR gate controlled by an ext. signal behaves as three-input logic gate, where the third input serves as input of the signal that controls the function. When this input is at high, the gate produces AND function, when the third input is at low, the gate produces OR function of two remaining inputs.

3 Newly Proposed Polymorphic Gate

A new polymorphic gate was proposed for our purposes. The gate has two optional functions – NAND and XOR. Both these functions are widely applicable, besides it, NAND is logic-complete. It predetermines the gate for wide usage in many applications. The function of the gate depends on a special signal similarly to AND/OR gate mentioned in the previous chapter. It makes the gate more flexible in terms of conditions under which the function is changed. If the function may be depending on Vdd ore temperature, certain level may be detected by a detector and the detector then may control the function-switching input of the gate. Of course, only one detector can be employed for the whole circuit. If the proposed gate functions switching may be used for some kind of reconfiguration (circuit function change on demand), it may be simply reached by controlling of function-switching inputs of all employed polymorphic gates.

The gate consists of 9 P-MOS and N-MOS transistors. It is CMOS-compatible. Output of the gate is designed as true complementary pair. It guarantees good quality of output signal under usual conditions. The structure of the gate is shown in Fig. 2. The mode switching signal should be connected to input “In_C”, then inputs “In_A” and “In_B” are logic variables inputs (see Fig. 1). When the input “In_C” is at low, the gate produces “In_A” NAND “In_B” at the output “Out”, when the input “In_C” is at high, the gate produces “In_A” XOR “In_B” at the output “Out”.

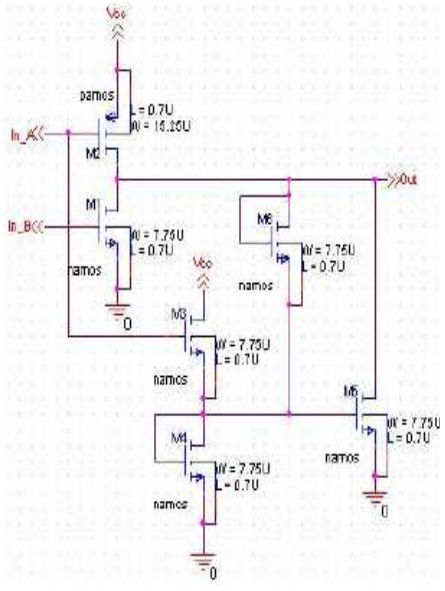

Figure 1: Structure of NAND/NOR gate proposed in [2]

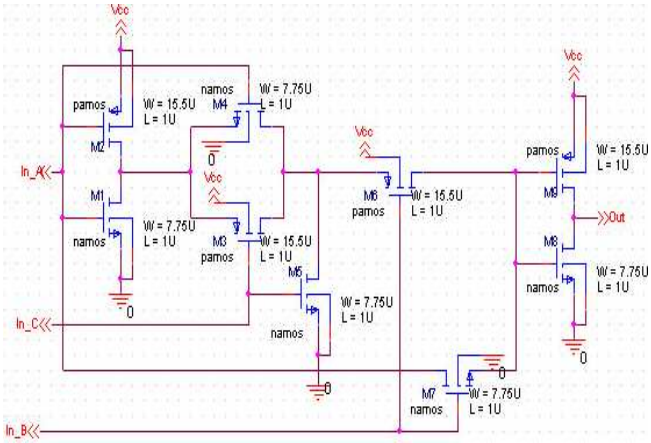

Figure 2: Structure of a newly proposed NAND/XOR gate

4 Simulation and Experiments

The proposed gate (see Fig. 2) was simulated using OrCAD PSpice 10.3 from Cadence and BSIM2 MOS transistor model from AMIS07 library. In Fig. 3 simulated waveforms for the proposed gate can be seen. Simulations show that the proposed gate meets requirements set in the first assignment. The gate operates reliably for Vdd > 2.5V and up to hundreds of MHz. The gate is not too temperature dependent, of course, higher temperature causes lower operation frequency. Generally, the gate overcomes previously published gates in many parameters and it appears to be really applicable in real circuits. One minor disadvantage could be slightly higher power consumption in some states. This is also feature inherited from 6-transistors XOR gate. When the transistor M6 (see Fig. 2) is used to transfer low logic level, then transistor M9 is not fully opened and M8 is not fully closed. Then the gate consumes 15 – 20 μA (see Fig. 3). In my opinion this is acceptable and it is very good result in comparison with previously proposed polymorphic gates. Fig. 3 shows simulated waveforms for the proposed gate.

5 Example of Gate Utilisation

Here is a little example of utilization of the proposed polymorphic NAND/XOR gate. It is sequential digital circuit, which can be used as a controller. The circuit in Fig. 3 is a kind of three-bit counter. It changes its state (state of three D-type flip-flops) each clock pulse. Glue logic, 2 two-input gates, reduces the number of states.

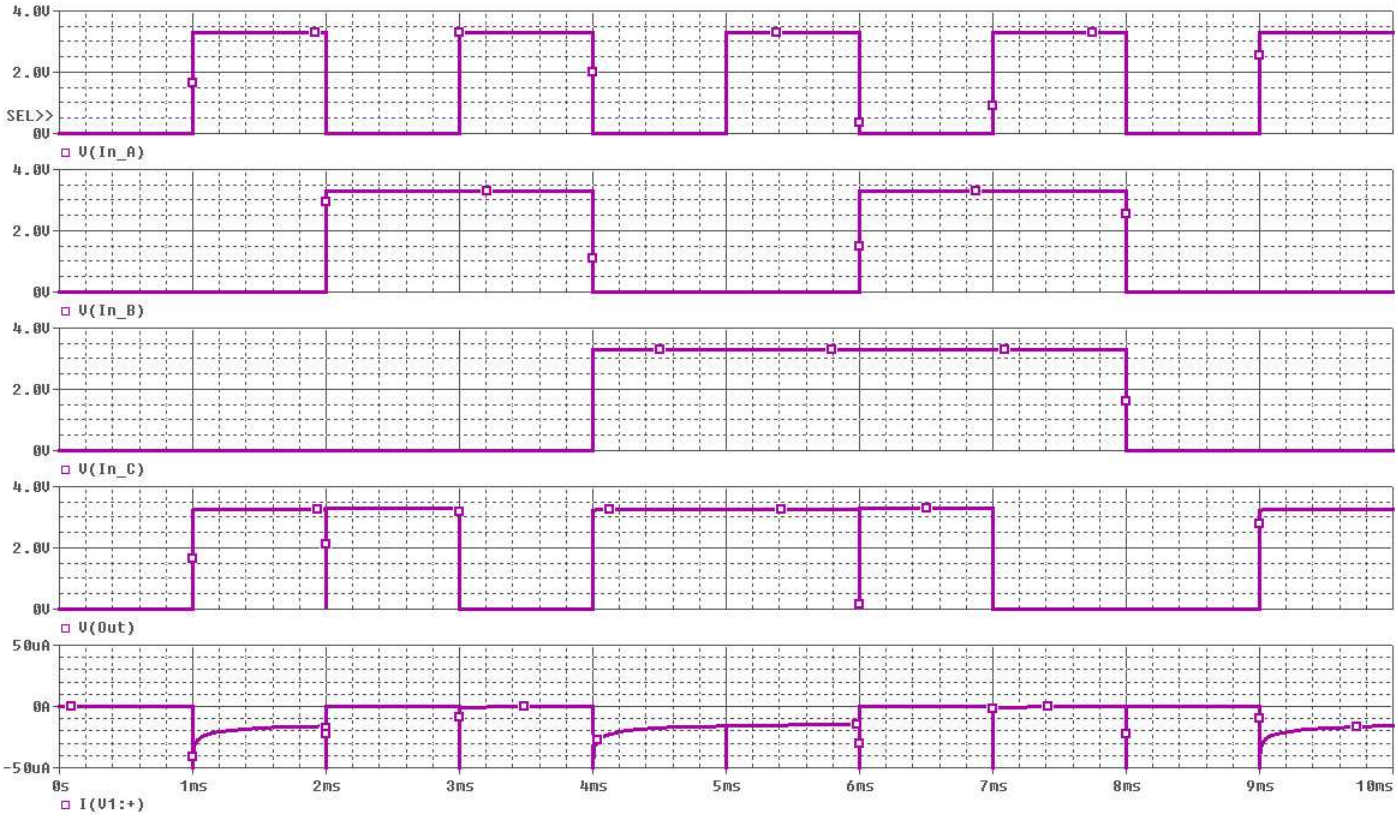

Figure 3: Simulation waveform for the proposed NAND/XOR polymorphic gate (Vdd = 3.3V, f = 1kHz, T = 20˚C)

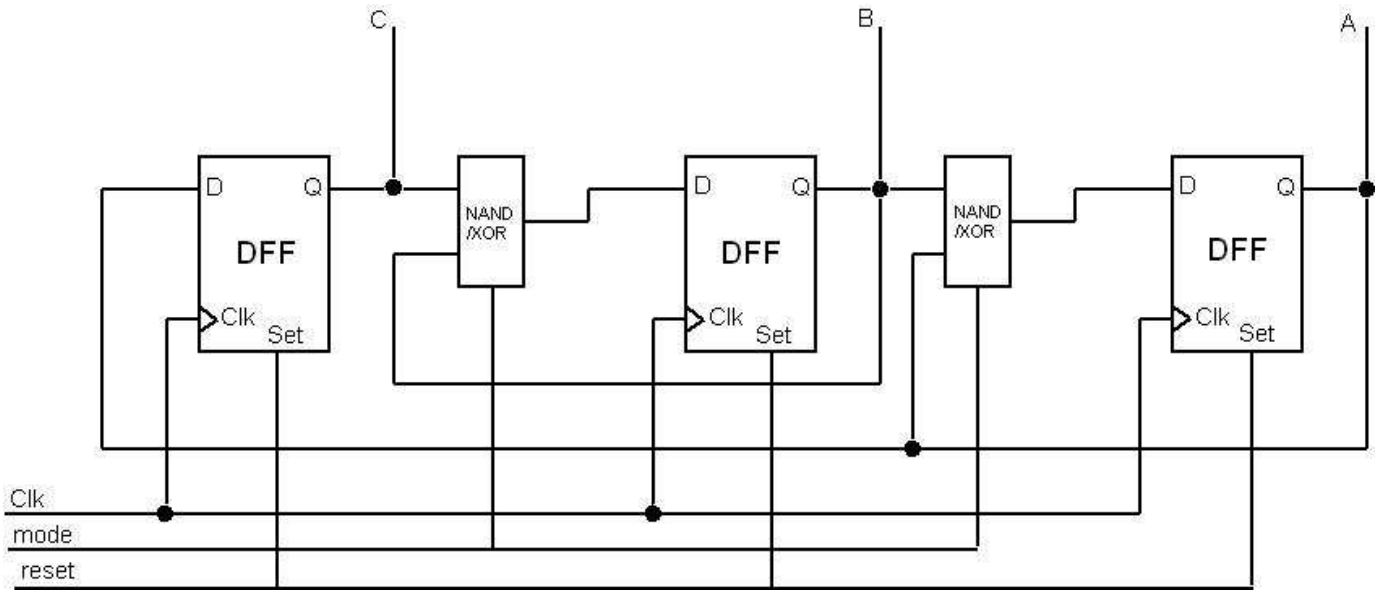

Figure 4: An example of polymorphic counter/controller employing proposed polymorphic NAND/XOR gate

Let us imagine that a seven-state controller is needed for an application, but under special conditions (e.g. when battery is low or circuit temperature is high), it is needed to skip two less important states. So under special conditions, only five-state counter is needed. In the conventional design approach, multiplexing of two separated counters/controllers or at least two glue/logic blocks of one counter to reconfigure the controller is needed. But polymorphic electronics offers more cheaper and smarter solution of the problem. Fig. 4 shows ordinary three/bit counter at the first sight. If two gates in the circuit shown in Fig. 4 are XORs, the counter has seven states. If these gates are NANDs, the counter has five states. If proposed polymorphic NAND/XOR gates are employed, the counter should be easily switched between two modes – seven- or five-state counter. Note that no structure reconfiguration or change is needed. Circuit function switching is done by changing of gate function only. Structure remains unchanged. This is typical attribute of polymorphic circuits.

Of course, above-described seven/five-state counter could be implemented using standard logic. But solution employing proposed polymorphic NAND/XOR gates is cheaper than any conventional solution in terms of transistor count/chip area. While one proposed polymorphic NAND/XOR gate consists of 9 transistors, ordinary NAND gate consists of 4 and ordinary XOR consist typically of 6 transistors [9]. Moreover several transistors are needed to switch between these two gates/functions (2-input multiplexer is typically implemented using 6 transistors). In comparison with solution employing two switched complete controllers more than 50% of chip area is saved. In comparison with solution employing switched glue logic with ordinary NAND and XOR gates, more than 20% of chip area is saved.

In Fig. 5, transition diagram is shown. Each transition is executed by a clock pulse. There are two states in the figure, for which the next state depends on the mode of polymorphic gates – state “001” and “100”. Dashed transitions show what happens when polymorphic gates are in “NAND” mode. In this mode, states “010” and “101” are skipped and the counter passes directly to states “110” and “111” respectively. Dotted transitions show full cycle of the counter (all seven states) when polymorphic gates are in “XOR” mode. When the counter is in one of “extended” states (“010” or “101”), next clock pulse causes transition to “110” or “111” regardless of the mode of polymorphic gates.

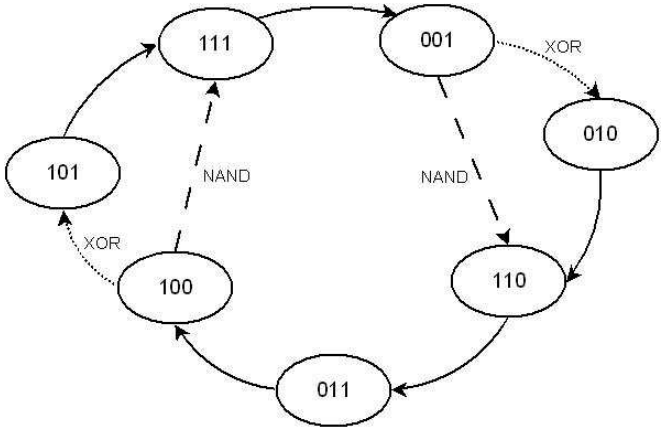

Figure 5: Transition diagram of the counter from Fig. 4

6 Conclusion

In the paper, a new gate was proposed. The gate has three inputs. From my point of view, it can be used as polymorphic two-mode, two-input gate, which performs NAND or XOR function according to the mode expressed by the state of the third input. In contrary to previously introduced polymorphic gates, the gate is robust; it inherits features from ordinary CMOS 6-transistors XOR gate [9]. The proposed gate has CMOS compatible output. The main contribution of this newly proposed gate lies in implementation cost. As a replacement of both NAND and XOR gates with switch, it consists of 9 transistors only. Ordinary NAND gate consists of 4 and ordinary XOR gate consists of 6 transistors. It is 10 transistors without the switch. The gate was simulated using Cadence OrCAD PSpice 10.3 and BSIM2 transistor model from AMIS07 library (0.7 micron technology). A small example shows how the utilisation of the proposed gate in a small and simple but frequently used circuit can save a significant number of transistors in compare with the conventional solution. For future work, fabrication of proposed gate is intended using CMOS 0.7 micron technology.

Acknowledgements

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