A Direct Digital Synthesis Firmware Development Framework

I. JIVET, B. DRAGOI, M. OTESTEANU, L. JURCA
Applied Electronics Department
University "Politechnica" Timisoara
V. Parvan 2, Timisoara
ROMANIA

Abstract: - The paper presents a development framework for direct digital signal synthesis targeting FPGA using the novel amplitude sequencing architecture. An analysis of the frequency purity and timing characteristics of the architecture is presented as key elements in the design process. An emulator for the generator circuit using the Xilinx picoBlaze microprocessor is proposed as a development framework in early design. The emulation of the generator in Xilinx picoBlaze code for single and double byte word length was used. Timing delays for the generator module were implemented as add on logic. The design of a three frequencies pack synthesizer using the integrated development environment is presented as a practical validation test. The flexible solution determined using the framework for a three frequency case sample application exemplifies the versatility of the proposed framework.

Keywords: amplitude based DDFS, picoBlaze emulated frequency synthesis, DDFS development framework.

1 Introduction

Direct digital synthesis is a technique that has been adopted in many fields of applications due to the advantages and characteristics hard to match with classical analog solutions [1][4]. The technology of choice for prototype or final implementation is shifting increasingly to FPGA devises [6].

The classical DDFS phase accumulator architecture has one major drawback in the explosive ROM size necessary in the case of high resolution signals. The literature in recent years presents new architectures promoting different methods to generate sine/cosine signals among which the CORDIC or angle rotation algorithms are more frequently used [4] [5].

A novel architecture based on algorithmic amplitude generation was proposed recently that distinguishes from the rest by its very efficient implementation [1].

Designing with DDFS cores is not a simple task due to the need of tuning the architecture to a particular application. Exploration of the design space and configuration of the architecture led solution providers to offer specialized software tools for the task [8][9].

The paper introduces a development environment for the amplitude based DDFS architecture. The main characteristics of the architecture are reviewed from the design process perspective. An in depth analysis of architecture output capabilities like frequency purity and phase timing compensation is also given.

A PicoBlaze emulation environment is introduced as a tool in the design process to help in the design space exploration for the amplitude based architecture. The framework provides a versatile mean for tuning the architecture and variable tracking in the design process.

Finally a design case for a sample application using the proposed environment is also presented as a proof of concept.

Further work needed and conclusions are presented in the final part of the paper.

2 Amplitude Based DDFS Architecture

The distinctive characteristic of the DDFS amplitude based architecture is the replacement of the phase to sine look up table translator module by a direct algorithmic amplitude generating core. The module generates algorithmically sequences of values by tracking the trajectory of a rotating vector on a circle, in a Cartesian coordinate frame. The successive vector positions projections on the two axis form the

sine and cosine value sequences.

It is known since the original paper that the sample values are non uniformly distributed with respect to phase[5]. Immediate use of the algorithmically determined values under uniform timing for the generation of sine and cosine samples results in phase distortions of the generated signal.

The extension of the algorithm with a correction in the phase for the use in sine and cosine function sequences generation is the following:

Loop:

Select the x or y direction for the next step;
Generate coordinates, as sampled values for sine and cosine functions;
Determine the phase angle advancement;
Output samples with sample timing delay;
For an opposite axis step keep the sample value constant.

End Loop;

In Fig. 1 a block diagram of the architecture is presented indicating the main modules and associated input control words.

The algorithm receives as inputs *AT* and *FT*, respectively the amplitude and frequency tuning words of length n, m. Register *r* and counters *c* implement storage and general system clock *Ck* counting. The x, y phase compensations counters *c* resolution can be adjusted to any value smaller then *n* trading accuracy to higher maximum generated signal frequency.

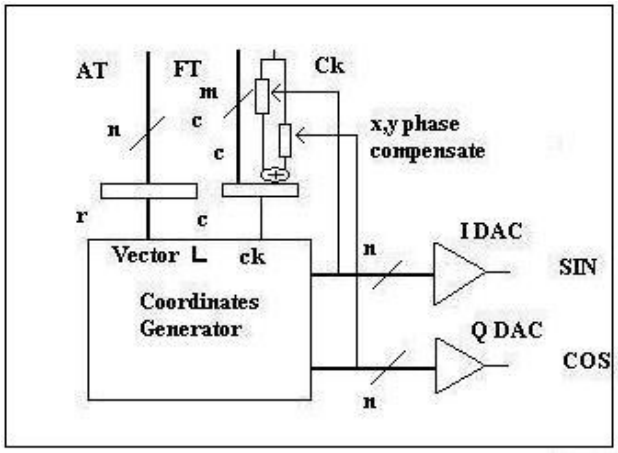

Fig.1 Amplitude based DDFS architecture block diagram with two input tuning words for amplitude and frequency.

The most sensitive element in the DDFS architecture remains the DAC converter and its linearity for wide word length in order to generate pure signals.

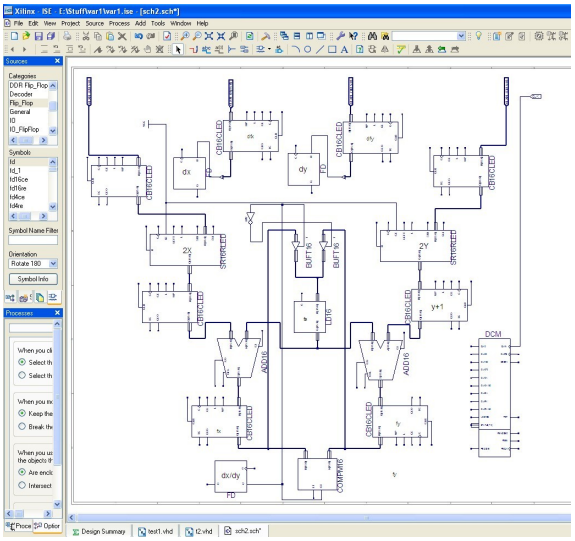

Fig. 2. Symmetric manual implementation of the amplitude generator algorithm at RTL level.

As it can be seen from the schematic above the circuit uses only one compare, two additions and several increments to be executed for each coordinate pair determination.

3 Designing using Amplitude Centered DDFS Architecture

Tuning the architecture to best suit a particular application is an important step in the design process. Variants of both the algorithm and the particular implementation must be coordinated to fit the requirements of the application.

Before committing to a HDL description for synthesis a PicoBlaze emulation of the generator is proposed to be used to determine a set of initial instantiations of the main components. This key design choices are determined by the design engineer as best suited to the application and become synthesis constrains.

The PicoBlaze processor from Xilinx was chosen as a digital generator emulator medium for samples tracking during generation. Variables for output timing as well as multiplexing and buffering requirements can be easily followed with accuracy and more insight.

The PicoBlaze architecture is of the same order of complexity as the amplitude based digital synthesizer

module and the flexibility to add extensions makes the PicoBlaze a good choice as an emulator nucleus of the digital synthesizer development framework. The use of the PicoBlaze in digital synthesis projects is also well supported and encouraged by Xilinx [12].

Additional loading, modulation and mirroring circuits, specific to different applications can also be emulated and validated in the same environment.

3.1 Amplitude, Frequency and Phase Tuning of the Amplitude Centered Architecture

The main advantage of the amplitude based DDFS architecture is the very reduced circuit resources requirement. Also the circuit gate count is linear in amplitude precision word length not exponential like in the case of classical architectures.

Frequency tuning must be loaded at cycle start as an input digital variable.

The very accurate and versatile FSK capacity of DDFS architectures is preserved.

The quadrature output inherent to DDFS architectures is retained in the new amplitude based architectures since the hardware implementation of the algorithm generates both sine and cosine.

2.2 Spectral Purity and Maximum Frequency of the Generated Signals

The spectral purity characteristic of the generated signals is very important for successful application of the architecture in practice.

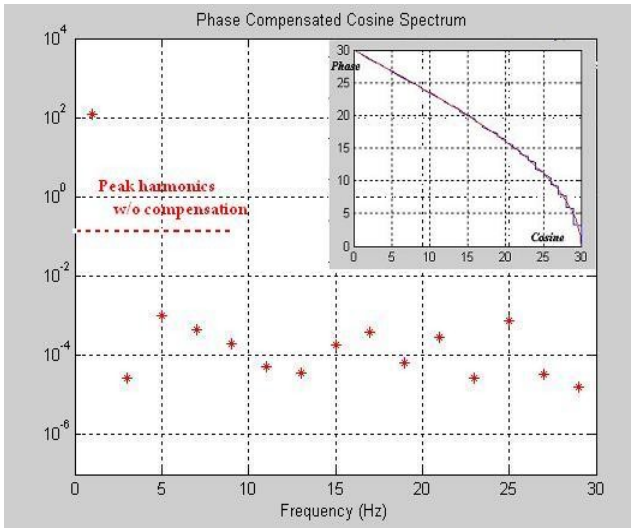

Fig. 3. Estimated power spectrum of the signal with amplitude algorithm and timing compensation.

High quality signals can be generated with the extended algorithm that includes phase timing compensation.

The FFT analysis of the generated signals using the original algorithm reveals a spectrum with first odd harmonics are a factor of about -35 dB below the central frequency.

Signal of even lower harmonics content can be obtained using more elaborate phase timing compensation methods.

Phase truncation before conversion to amplitude is not necessary in the amplitude based architecture and the problem of spur frequencies thus generated in the output is eliminated.

The upper frequency limit is given by the maximum clock frequency available in the target technology scaled down by the phase compensation counters length. As a result the maximum frequency of the generated signal is reduced accordingly.

In order to increase the maximum frequency of the generated signal timing delay truncation is one option.

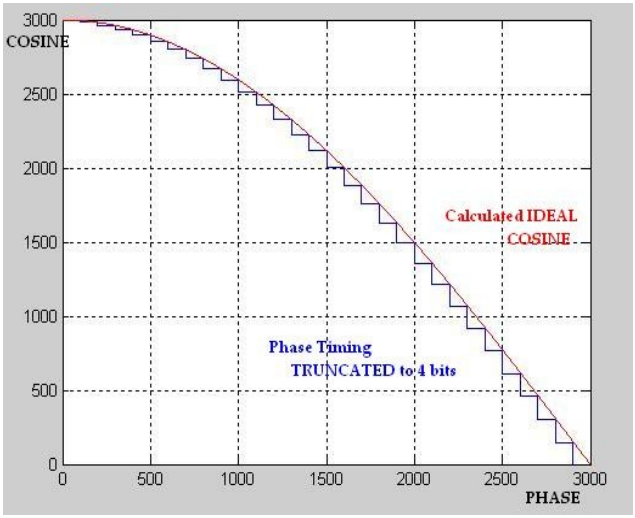

Fig. 4. Sample truncated timing in order to increase the maxim possible frequency of the generated signal.

The effect of sample delay timing truncation is a increase in the output noise similar to quantization noise.

4 PicoBlaze Emulator and Extensions for Solution Tuning ahead of Synthesis

The PicoBlaze microcontroller was designed aimimg the objectives of simplicity and low deployment cost.

Typical implementations in a FPGA together with a block RAM that stores the instructions can be simulated in the performant Xilinx ISE environment and its states easily tracked.

The PicoBlaze is supported by development tools including an assembler, an integrated development environment (ISE) and a third party graphical instruction set simulator software tool. Furthermore, the PicoBlaze microcontroller is provided as a free, source-level VHDL file with royalty-free re-use within Xilinx FPGAs thus avoiding proprietary issues.

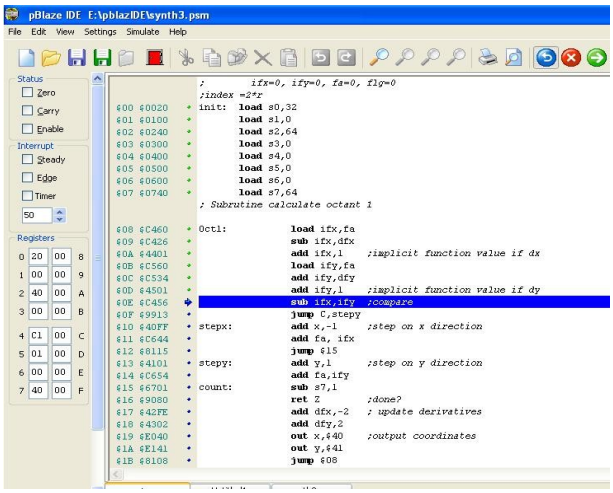

Fig. 5. Outline of the PicoBlaze code development environment for direct digital synthesis module.

For the purpose of this project the Mediatronix pBlaze IDE assembler and graphical instruction set simulator was used.

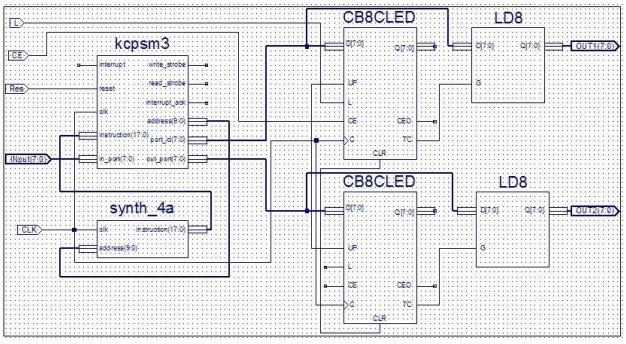

Fig. 6. Example of a complete module in a multiple frequency synthesis application.

The DDFS module was implemented in assembly code using byte-wide arithmetic. The 16 byte-wide general-purpose data registers are just sufficient to accommodate the variables for two frequency synthesizer module simultaneously.

The basic amplitude generation module was implemented in PicoBlaze assembly code in both original eight bit wide world length and a extended double byte version.

The timing function was implemented in a hardware module as add on to the core PicoBlaze emulated module [12].

Table 1

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	76	3,840	1%
Number of 4 input LUTs	116	3,840	3%
Logic Distribution			
Number of occupied Slices	100	1,920	5%
Number of Slices containing only related logic	100	100	100%
Number of Slices containing unrelated logic	0	100	0%
Total Number of 4 input LUTs	186	3,840	4%

The results of the ICE synthesis of the emulated module and its timing circuit are presented in Table 1 Gate count is very low and nearly equal to the gate count synthesis result for an amplitude based DDFS architecture of the manually instantiated reference.

5 Sample DDFS Design Project Results

Every synthesized frequency application has its specific needs that are difficult to define in the early stages of the design. The project in this example is an ongoing project in the field of Electrical Bio-Impedance hardware development.

The objective of the project is to design a flexible and 'tunable' three frequency generators for use in the MIT tomography [9].

The amplitude based DDFS architecture as proposed was found as well suited for compact generator implementation placed next to each magnetic field generator coil.

The design target device for the final implementation is the Xilinx Spartan 3 series. The master timing can be implemented by division of master clock frequency using the DCM (Digital Clock Manager) module [10].

Direct implementation in VHDL of a flexible clock scheme using the capabilities the Xilinx DCM (Digital Clock Manager) would be difficult to accomplish.

The PicoBlaze Digital Synthesizer Emulation

Environment was used to explore the solutions to generate simultaneously three frequencies using for each a direct frequency synthesizer module and clock obtained from a associated DCM resource.

One simple solution identified was to generate the three frequencies scaled in amplitude using the same clock frequency and stabilized for jitter by the DCM.

The leveling of amplitudes is done by truncating the two least significant bits.

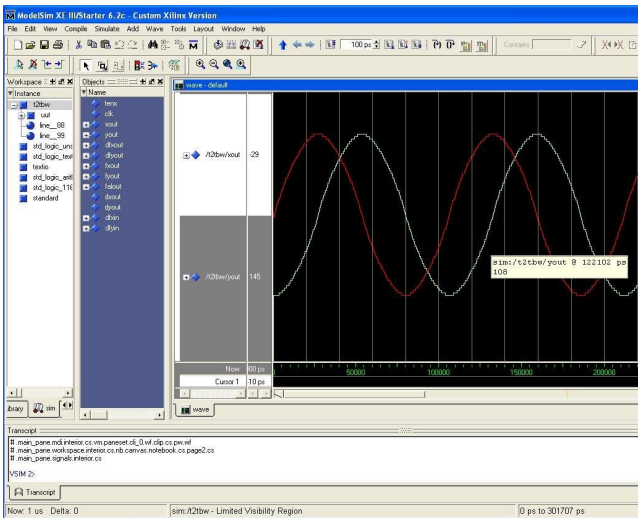

Fig.7 PicoBlaze simulation of multi frequency signal generated using the amplitude based DDFS architecture.

Further work is necessary using the same environment to determine the noise level introduced by sample delay word truncation for applications with frequencies higher then the 1Mhz range.

6 Conclusions

The paper presents a design framework for frequency synthesis using the amplitude based DDFS architecture targeting FPGA implementation. In depth analysis of the algorithm outlines the timing method and the output frequency spectrum of the generated signal. This was found as on eof the main qualities of the proposed architecture with great practical importance.

A development framework is exemplified for design insight and internal variable visibility using the Xilinx ISE environment and a PicoBlaze software emulation for the amplitude generating module.

Emulation in assembly code of the amplitude generator module and the synthesis results for Xilinx Spartan 3 family of devices proved the major advantage of the amplitude based architecture - the flexibility to implement multi frequency signal generation with a very low gate count.

A practical application sample design space exploration and solution proofing is also presented.

Further work is necessary to determine the highest signal frequency by timing delay truncation.

References

[1] I. Jivet, B. Dragoi Direct Digital Synthesizer Architecture based on Amplitude Sequencing, Proceedings of the 9th Intrenational WSEAS Conference on Circuits, Crete, July 07, p. 421-425

[2] B.W. Jordan, W.J. Lennon, and B.D Holm. An Improved Algorithm for the Generation of Nonparametric Curves. *IEEE Transactions on Computers*, Vol.C-22, No. 12, 73, pp. 1052-1060.

[3] T. C. Huang, H. T. Ho, Digital sine/cosine wave generator,*US Patent 6892213,* Issued May, 2005.

[4] D. Nowrouzezahrai, B. Decker and W. Bishop High-Performance Double-Precision Cosine Generation, *Proceedings of the 2005 International Conference on Computer Design*, Las Vegas, Nevada, USA, June 27-30, 2005 pp.42 – 48

[5] Dengwei Fu, and A. N. Willson, Jr.A Two-Stage Angle-Rotation Architecture and Its Error Analysis for Efficient Digital Mixer Implementation, *IEEE Tran. on Circuits & Systems*,Vol.53,No. 3, 03/06.

[6] T. Vladimirova and H. Tiggeler, FPGA Implementation of Sine and Cosine Generators Using the CORDIC Algorithm, *Proceedings of 2006 MAPLD International Conference*, Washington, D.C.,September 26-28, 2006.

[7] Madisetti, A.; Kwentus, A.; Willson, A.N A Sine/Cosine Direct Digital Frequency Synthesizer using an Angle Rotation Algorithm, *1995 IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, Feb 95 pp:262 – 263.

[8] Numerically Controlled Oscillators, Altera Corp. www.altera.com /literature/ug/ *ug_nco.pdf*, *MegaCore Function Users Guide,* Altera, May 07.

[9] H. Sharfetter, A Kostinger, S Issa, Spectroscopic 16 channel magnetic induction tomograph: the new Graz MIT system, *Proc. of the 13th Int. Conference on Electical Bioimpedance,* Graz, Austria, 07

[10] Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs, *Xilinx, XAPP 462,* Jan 5, 2006.