A Low Noise and Reliable CMOS I/O Buffer for Mixed Low Voltage Applications

HWANG-CHERNG CHOW and YOU-GANG CHEN
Department and Graduate Institute of Electronics Engineering, Chang Gung University
259 Wen-Hwa 1st Road, Kwei-Shan, Tao-Yuan 333
TAIWAN, REPUBLIC OF CHINA
http://www.elec.cgu.edu.tw

Abstract: - In this paper the design of a high voltage tolerant and reliable CMOS I/O buffer is proposed without using thick-oxide devices. In this presented design for mixed low voltage interface applications, it uses a simpler structure and therefore the circuit has good gate-oxide reliability. In addition, it is free of dc leakage current. No additional pad for dual power supplies is required in the proposed circuit. The pull-up operation including both the rise-time and power-delay product is reduced about 20%. The simple structure leads to 50% area saving as compared to the existing prior art.

Key-Words: - I/O buffer, Mixed low voltage, Interface, Single pad, DC leakage

1 Introduction

With the advancement of the process technology, the device dimension scales down and the standard power supply voltage also reduces to a lower level. However, for system design, it is hard to convert all high voltage (for example 5V, 3.3V or 2.5V) components into low voltage (1.8V) integrated circuits due to the cost consideration. Because of these facts, there are usually different supply voltages used so that the transmission of signals between high and low voltage circuits has some problems. This causes the desire for the mixed low voltage interface applications.

2 Prior Art

As shown in Fig. 1, it is a conventional CMOS input/output (I/O) buffer. When the OEN signal is ”0”, it is an output buffer and when the OEN signal is “1”, it is an input buffer (in tri-state mode). When the buffer operates as an input buffer and the signal in PAD is VDDH, many big problems arise. For example, the first, reliability problems in gate-oxide of strong PMOS MP1 and NMOS MN1 are suffered due to the high electric field resulting from high voltage difference of the gate-drain and gate-source terminals. Because transistors are generally fabricated with thin gate-oxide, they cannot tolerate the high voltage difference and the oxide can only tolerate 20%~30% higher than the nominal supply voltage [1]. Therefore, thin gate-oxide will break down due to overstress [1]. The second problem is that the voltage in nodes “b” and “c” should be VDD and 0V to turn the strong PMOS MP1 and NMOS MN1 off and therefore there is no static power consumption. However, under the high voltage input signal condition, the parasitic diode of PMOS MP1 to well will conduct current due to forward bias. The other leakage path is from pad to VDD via the pull-up PMOS channel since the high voltage causes the V_{DG} (voltage difference between drain and gate of PMOS) is larger than its threshold voltage |Vtp|. These two-leakage paths will lead to extra power consumption and wrong operations.

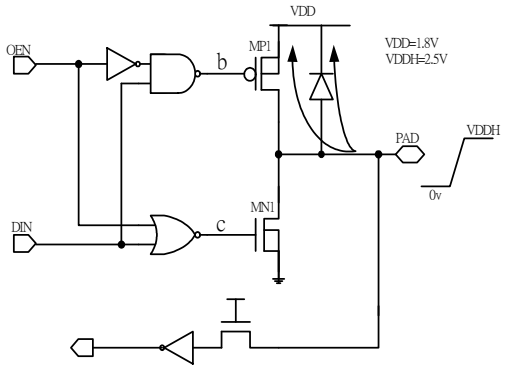


Fig. 1 A conventional 1.8V I/O buffer driven by a 2.5V input signal

There are some prior art circuits proposed to solve these problems [2]-[8]. The use of thick- oxide device and the stack NMOS can overcome the gate-oxide overstress problems [2]. And the second power supply (VDDH PAD) connected to the pull-up PMOS N-well can solve the leakage current

problems [3]. However, these solutions also have a few drawbacks. The first one is that the use of thick-oxide devices needs a dual-oxide process. The second drawback is that the second power needs an additional bonding pad. Therefore, a prior art circuit that can eliminate the problems described above is proposed [4], as shown in Fig. 2. In this circuit, it uses a technique called "floating N-well". Although it overcomes the problems but the use of many additional transistors makes the circuit complicated. As shown in Fig. 3, in this prior art circuit [5], it uses only 4 additional transistors to realize the function. It reduces the complexity of the circuit design but the transistor MN3 needs a thick-oxide device and the series structure of the two large PMOS transistors needs more area to achieve the circuit layout and degrades the rise-time.

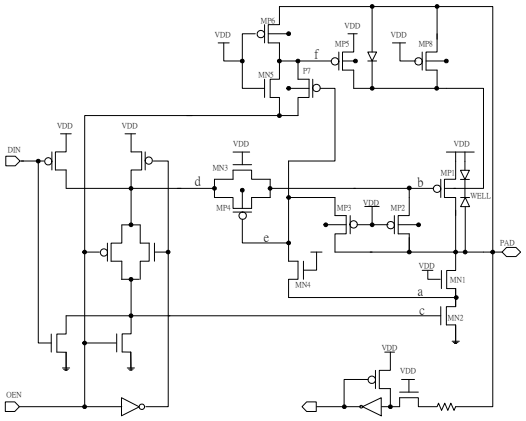


Fig. 2 The prior art 1 mixed-voltage input/output buffer

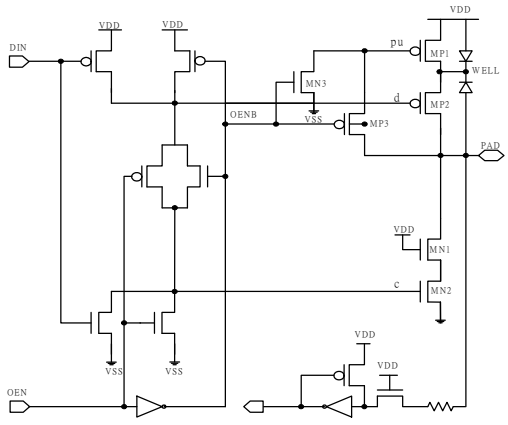


Fig. 3 The prior art 2 mixed-voltage input/output buffer

3 Proposed Circuit

The proposed CMOS I/O buffer is shown in Fig. 4. The left part is a pre-driver circuit and the other part is the main circuit. The proposed circuit uses the technique of "floating N-well." The circuit operation is described in the following.

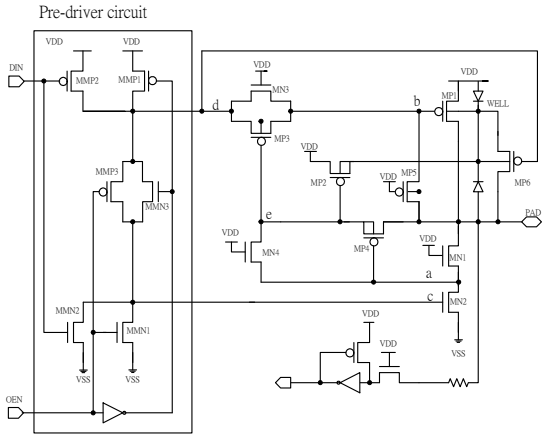


Fig. 4 The proposed mixed-voltage input/output buffer

When OEN= "0", it is for output buffer use. As shown in Fig. 5, when the input signal DIN is "1", the node "b" is discharged to 0V and the node "c" is also discharged to 0V. Therefore the PAD voltage is pulled up to VDD by MP1 and MN2 is turned off. Because the node "d" voltage is discharged to 0V, the WELL voltage can be pulled up to VDD by MP6 via PAD.

As shown in Fig. 6, when the input signal DIN is "0", the node "b" is initially pulled up to VDD-Vtn(mn3) and the node "c" is pulled up to VDD. Therefore, MN2 is turned on and the node "e" voltage is discharged to 0V. So the node "b" voltage can be pulled up to VDD to turn MP1 completely off. Because the node "d" voltage is VDD, the WELL voltage can be pulled up to VDD by MP2.

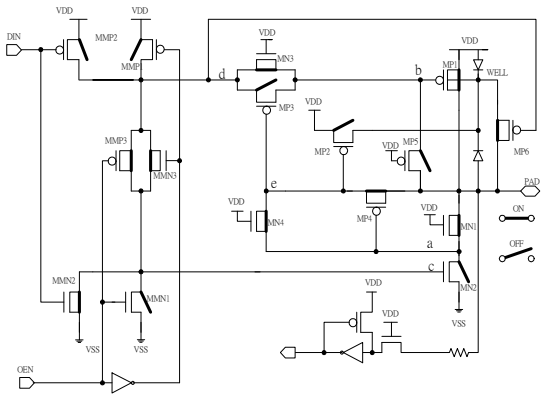


Fig. 5 The proposed circuit for output buffer use. (DIN="1")

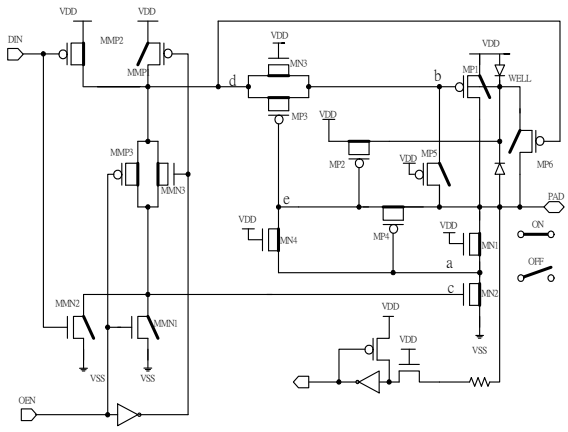


Fig. 6 The proposed circuit for output buffer use.(DIN=”0”)

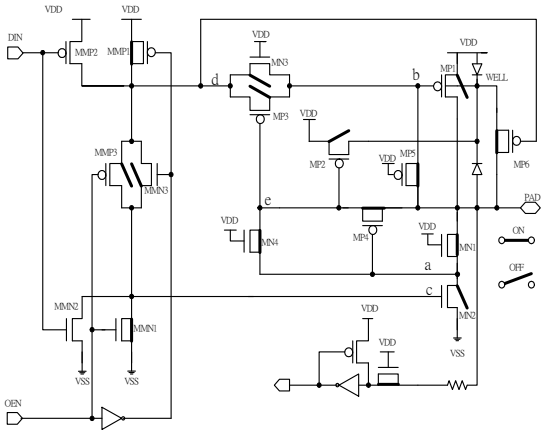
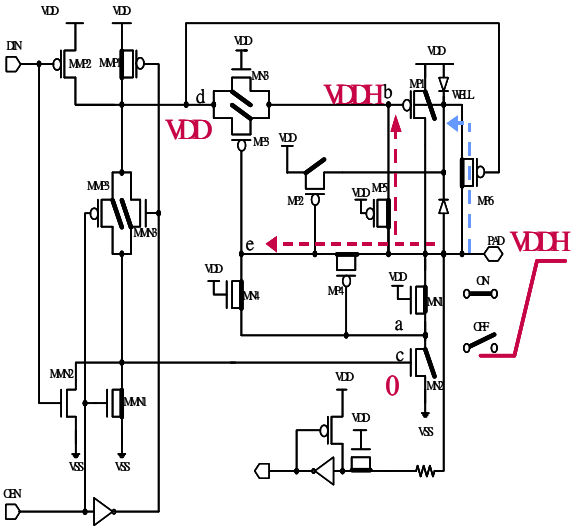


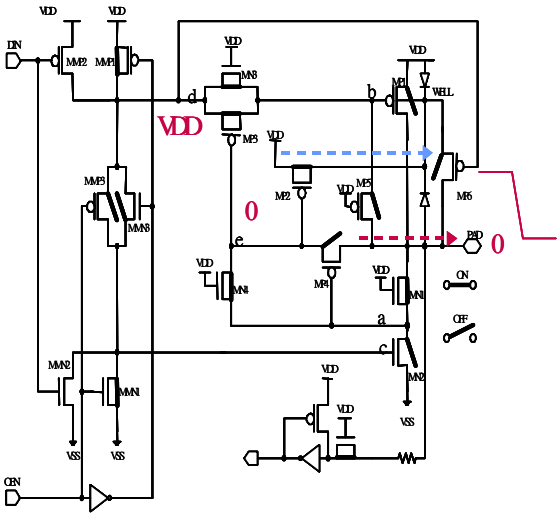
Fig. 7 The proposed circuit for input buffer use

When OEN= “1”, it is for input buffer use, as shown in Fig. 7. It means that both MP1 and MN2 are in off state. As shown in Fig. 8(a), when the input high signal via the PAD is VDDH, the node “b” voltage can be pulled up to VDDH by MP5 and the node “a” voltage is pulled to VDD-Vtn(MN1). Therefore, MP1 is turned off and MP4 is turned on to pull the node “e” voltage to VDDH to keep MP3 off. The WELL voltage is pulled to VDDH by MP6 because the gate voltage of MP6 is VDD. As for the case that the input high signal via the PAD is VSS (0V), the details are shown in Fig. 8(b). Therefore, there are no leakage current paths and no gate-oxide overstress condition in the devices in the proposed circuit for all input conditions.

Because the proposed circuit uses the technique of “floating N-well”, the latch-up problem may arise. Therefore, the double guard ring structure should be applied to avoid the latch-up problem.



(a)



(b)

Fig. 8 input buffer (a) PAD=VDDH (b) PAD=0V

4 Results and Discussions

The simulation results are performed based on TSMC 0.18μm CMOS process by Hspice. In Fig. 9, it is the comparison of rise-time between the proposed circuit and prior art 2 circuit [5] (Fig. 4) under 50MHz with 150pF load in output buffer mode. It is obvious that the pull-up speed in the

proposed circuit is faster than that of the prior art 2 circuit.

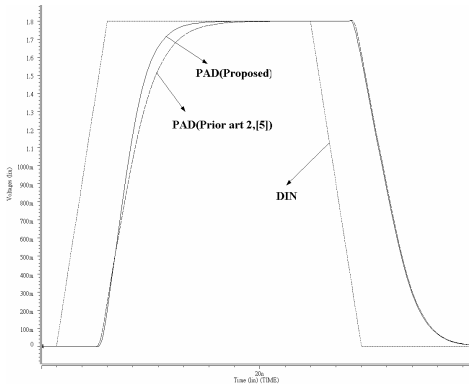


Fig. 9 The comparison of rise-time between the proposed circuit and prior art 2 circuit

In Fig. 10, it is the comparison of the WELL voltage among the proposed circuit, prior art circuit [4] and prior art circuit [5] operating as an output buffer at 50 MHz with 150pF load. From the waveform, the WELL voltage in prior art circuit [5] is lower. It may cause the parasitic diode forward bias and results in latch-up.

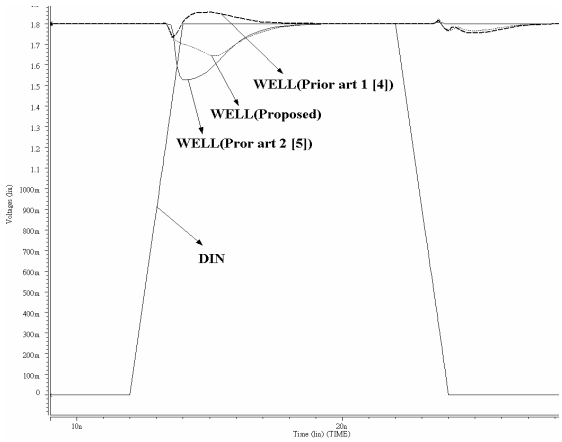


Fig. 10 The comparison of the WELL voltage among the proposed circuit, prior art circuit [4] and prior art circuit [5] as an output buffer at 50MHz

In Fig. 11, it is the comparison of the WELL voltage among the proposed circuit, prior art circuit [4] and prior art circuit [7] operating as an input buffer at 100 MHz in 3.3V. From the waveform, when the input signal is VDDH, the WELL voltage can change to VDDH with the PAD voltage. Therefore, it can get good gate-oxide reliability and has no leakage path. However, the WELL voltage of the prior art circuit keeps floating and cannot change to VDDH. This condition may cause latch-up. As for the complete mixed-voltage I/O simulations, the results are given in Fig. 12.

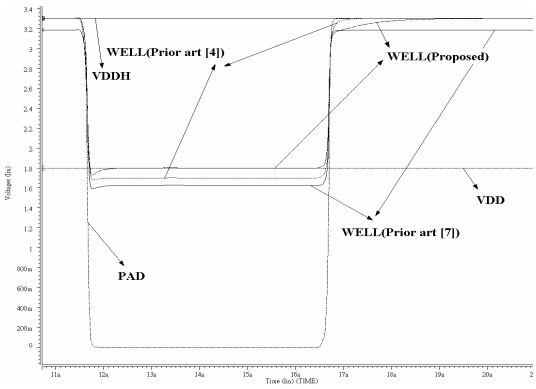


Fig. 11 The comparison of the WELL voltage among the proposed circuit, prior art circuit [4] and prior art circuit [7] as an input buffer at 100 MHz in 3.3V

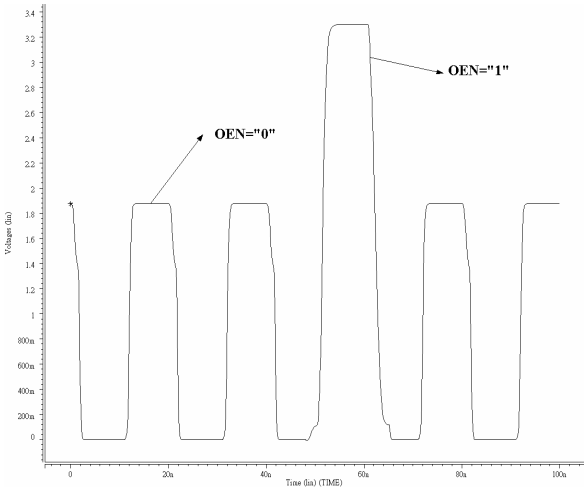


Fig. 12 Complete mixed-voltage I/O simulation results

As shown in Table 1, it is the performance comparison among the prior art 1 [4], prior art 2 [5], and proposed circuits. In this table, where Trpad and Tfpad: rise-time and fall-time in PAD, respectively; Tdr and Tdf: rising and falling propagation delay between input signal (DIN) and output signal (PAD), respectively; PDP-r and PDP-f: power-delay (Tdr or Tdf) product; additional transistors: devices added except the large MP1 and MN2. The transistor count of additional devices in the proposed circuit is 8 as compared to 11 in prior art 1. Therefore, the circuit complexity is effectively reduced 27% while it also

demonstrates about 10% pull-up speed enhancement. As compared to prior art 2, the pull-up speed including both the rise-time and PDP is about 20% improvement while the area is reduced to only half. Therefore, the proposed circuit has higher speed performance, better latch-up immunity, lower circuit complexity, and very smaller area.

5 Conclusion

In this paper, the design of a high voltage tolerant and reliable CMOS I/O buffer has been proposed without using thick-oxide devices. In this presented design for mixed low voltage interface applications, it uses a simpler structure and therefore the circuit has good gate-oxide reliability. In addition, it is free of dc leakage current. No additional pad for dual power supplies is required in the proposed circuit. The pull-up operation including both the rise-time and power-delay product is reduced about 20%. The simple structure leads to 50% area saving as compared to the existing prior art. Therefore, the proposed I/O buffer is very suitable for mixed low voltage interface applications.

References:

[1] A. -J. Annema, G.J.G.M. Geelen, and P.C. de Jong, 5.5-V I/O in a 2.5-V 0.25-µm CMOS technology, *IEEE Journal of Solid-State Circuits*, Vol. 36, 2001, pp. 538-538.

[2] K. Bult, Analog broadband communication circuits in pure digital deep sub-nicron CMOS, in Dig. Tech. Papers *Int. Solid-State Circuits Conf.* , 1999, pp 76-77.

[3] M. Assar et al., CMOS low power mixed voltage bidirectional I/O buffer, *US Patent #5,300,835*, April 1994.

[4] M. Pelgrom and E. Dijkmans, A 3/5 V Compatible I/O Buffer, *IEEE J. Solid-State Circuits,* Vol. 30, 1995, pp. 823-825.

[5] H. -C. Chow, Bidirectional buffer for mixed voltage applications, *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems,* Vol. 1, 1999, pp. 270-273.

[6] D. -Y. Chen, Design of a mixed 3.3 V and 5 V PCI I/O buffer, 2nd International Conference on ASIC, 1996, pp. 336-339.

[7] M. -D. Ker and C. -S. Tsai, Design of 2.5 V/5 V mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic N-well bias circuit, *Proceedings of the 2003 International Symposium on Circuits and Systems*, Vol. 5, 2002, pp. 97-100.

[8] G. P. Singh and A. B. Salem, High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process, *IEEE J. Solid-State Circuits,* Vol. 34, 1999, pp. 1512-1525.

*The software support from the Chip Implementation Center of Taiwan is acknowledged.

Table 1 Performance comparison

50MHz/150pf	prior art 1	prior art [6]	prior art 2	prior art [7]	proposed
Power(mW)	25.315	27.022	25.389	27.88	25.465
improvement	-0.59%	5.70%	-0.29%	8.60%	
Trpad(ns)	2.096	2.092	2.420	2.23	1.948
improvement	7.00%	10.27%	19.50%	12.60%	---
Tfpad(ns)	2.390	2.547	2.382	2.590	2.390
improvement	0%	6.10%	-0.33%	7.700%	---
Tdr(ns)	2.355	2.326	2.663	2.86	2.194
improvement	6.80%	8.25%	17.60%	23.20%	---
Tdf(ns)	1.738	1.745	1.789	1.740	1.740
PDP-r(W*s)	5.980E-11	6.29E-11	6.742E-11	7.99E-11	5.893E-11
improvement	1.50%	13.35%	12.60%	26.20%	---
PDP-f(W*s)	4.412E-11	4.72E-11	4.528E-11	4.85E-11	4.432E-11
improvement	-0.45%	6.10%	1.90%	8.60%	---
Additional transistors	11	6	4	11	8
improvement	27.20%	-25%	-50%	27.20%	---
Area(um)	1300	1270	2580	1297	1280
improvement	1.60%	---	50.30%	1.30%	---