Reliability of Single-Electron Logic Gates

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Abstract: - This paper investigates the relationship between a single-electron gate probability of failure and the random variations affecting its elements. The study focuses on digital logic gates and circuits. Two major implementations are considered: static complementary logic gates and threshold logic gates (TLG). In addition to implementation, the effect of the gate fan-in on the reliability is investigated. The results show that the type of implementation strongly affects the gate's intrinsic robustness to variations. A static SET gate has a higher probability of failure than a SET TLG implementing the same function. Regarding fan-in, the results show that the probability of failure of TLGs increases with increasing fan-in. The results of this study indicate that the neural inspired threshold logic gates are more suitable for the emerging SET technology than the static complementary gates used in current technology.

Key-Words: - Reliability, Single-Electron, Threshold Gates, Static Gates, Statistical Model.

1 Introduction

The continuous miniaturization of electronic devices, and the discovery of novel nano-devices are facing many challenges, including the reliability of these devices [1]. The small size, and consequently the small amount of energy required and allowed in switching these devices, make them susceptible to fabrication defects (hard errors) and transient failures (soft errors). Single-Electron-Technology (SET) is an emerging technology that is distinguished by very small device sizes, and ultra-low power dissipation, but faces serious reliability issues.

A large number of articles have reported advances in analytical models of reliability, and in the simulation/analysis of practical design strategies. The bulk of the analytical research focuses on bounding the complexity of reliable circuit designs [2]. Broadly speaking, these studies seek to construct a reliable architecture for a particular logic function, given the failure probability of gates and/or wires. On the design side, the reliability has been tackled at all levels: device, gate, module, and system level. The application of reliable design strategies to nanoelectronic module design has been considered in [3],[4]. To the author's knowledge, the first device-level reliability study for SET gates was performed in [5], where a statistical module was used to estimate the tolerance of different gates. In this study, this module has been improved to calculate the probability of failure of different SET gates rather than the tolerance limit.

The remainder of this paper is organized as follows. Section 2 describes the different designs of SET gates and circuits. The modeling and simulation procedure is described in Section 3. Section 4 presents the results of this reliability investigation, followed by concluding remarks.

2 Single-Electron Technology Gates

Two different implementations of SET gates were considered in this study: threshold logic gates (TLG) and static complementary logic gates. A TLG is the simplest artificial neuron which computes the sign of the weighted sum of its inputs. The TLG compares the weighted sum with a threshold value. If the weighted sum is larger than the threshold, the TLG outputs a one, otherwise the output becomes a zero. In the remainder of this paper, a TLG will be represented by the series of its weights $(w_1,\ldots,w_n)$. Static complementary gates are similar to the well-known static CMOS gates. NAND and NOR static SET gates are shown in Fig. 1(a) and Fig. 2(a).

The TLG design is based on the SET inverter which contains bias capacitors connected to the two complementary SET transistors (similar to the NMOS and PMOS transistors) [6]. Considering the SET NAND gate, it can be implemented as follows. To start with, design parameters are determined based on the AND logic function (not the NAND)
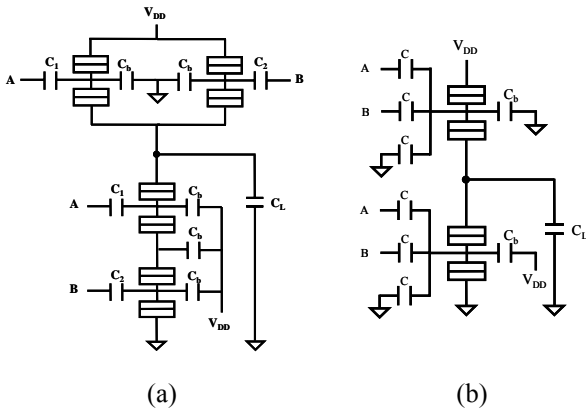
Fig. 1: Single-Electron-Technology NAND gate implementations (a) Static (b) Threshold.

Fig. 2: Single-Electron-Technology NOR gate implementations (a) Static (b) Threshold.

because SET gates have an inversion property. The AND function can be described by the threshold equation: $F = sign(A + B - 1.5)$. The function has two equally weighted inputs and a threshold of 1.5. The sum of all input capacitors should be equal to the input capacitance of the SET inverter (3 aF for the particular inverter considered in this design). We define C as the unit capacitance corresponding to a weight of 1. Since the threshold is 1.5, the sum of two capacitor units should be larger than 1.5 aF and one capacitor unit less than this value. Mathematically: $2C > 1.5$ aF and $C < 1.5$ aF, hence 0.75 aF $< C < 1.5$ aF. Using $C_1 = C_2 = 1$ aF gives a total of 2 aF. Hence, this TLG requires a bias capacitor C_b of 1 aF to complete the sum of input capacitors to 3 aF. The bias capacitor should be connected to ground for proper operation of the TLG (Fig. 1(b)). The design of the NOR gate is similar to the NAND except that the bias capacitor is connected to V_{DD} for proper operation of the TLG (Fig. 2(b)).
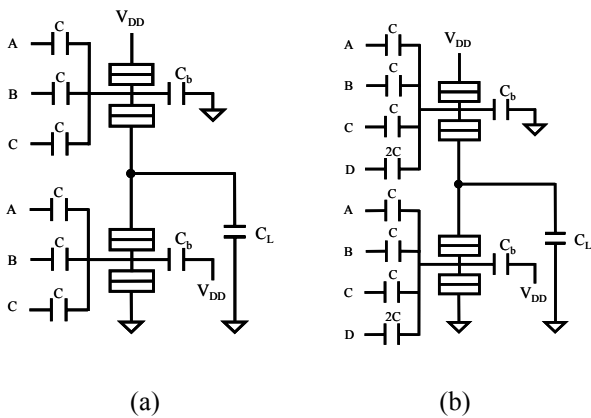
In addition to the NAND and NOR, other SET gates with different fan-in were considered. Figure 3 shows the Majority gate (MAJ) and the TLG(1,1,1,2). These two gates are the major components of SET adders [7], which are the major elements in computing systems. The majority gate has a simple design consisting of three equal input capacitors. The TLG(1,1,1,2) comprises four capacitors corresponding to the weight series (1,1,1,2).

At the circuit level, two SET full adders were considered. The first one is the Majority full adder, which consists of three MAJ gates and two inverters (Fig. 4(a)). One MAJ and an inverter produce the carry C_o, while the combination of all the gates produces the sum S. The second one is the TLG full adder, which uses general TLGs instead of MAJs. By using TLGs, the circuit is reduced from three MAJs and two inverters (Fig. 4(a)), to only two TLGs (Fig. 4(b)). The sum function is implemented by a TLG(1,1,1,2) and the carry by a MAJ [7].
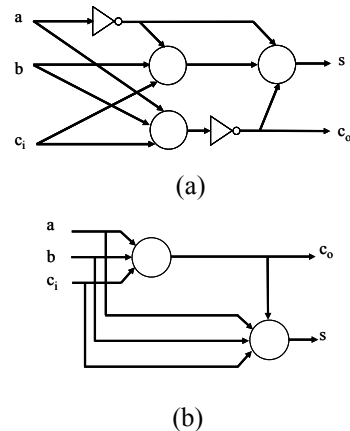

Fig. 3: Single-Electron-Technology threshold gates (a) Majority (b) TLG(1,1,1,2).

Fig. 4: SET full adders (a) Majority (b) TLG.

3 Modeling and Simulation

SET circuits are simulated by SIMON [8] using a MonteCarlo method, rather than a SPICE model-based program. MATLAB modules were developed and used in conjunction with SIMON for simulating SET gates and circuits. The necessity to use MATLAB modules stems from a number of limitations in SIMON including its inability to generate statistical data sets. Statistical analysis is an important requirement for fully exploring the sensitivity to process variations of SET gates and circuits. The statistical analysis module allows the selective injection of random or controlled errors into the capacitors and tunneling junctions. These modules prepare the input data, call SIMON repeatedly to simulate the SET device, record output, and finally process and present the results graphically.

The statistical analysis module works as follows. Random errors are injected into SET elements (capacitors and tunneling junctions). A modified capacitor value is computed as $C' = C + v*U(-1,1)$, where C is the original value, v is the maximum allowed variation, and $U(-1,1)$ is a random number uniformly distributed between -1 and 1. The new circuit (with modified capacitors) is then simulated with SIMON. The process of varying the values, and performing simulations, is repeated 10000 times in a loop in MATLAB, while data is collected. This data includes the number of errors at the outputs of individual gates. The number of errors of individual gates are averaged and used to calculate the probability of failure of that particular gate.
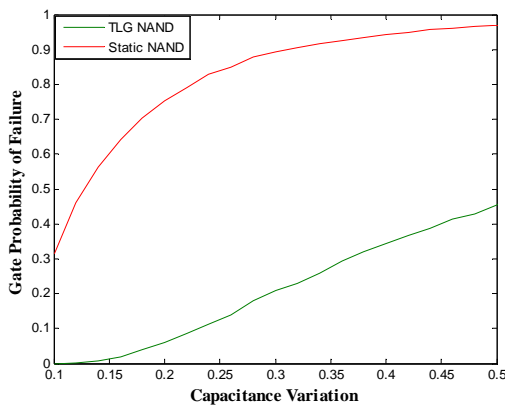
4 Results

The probability of failure of different SET gates and circuits were obtained for different capacitance variations. Figures 5 and 6 show the results for the NAND and NOR gates. These results show that the probability of failure of a TLG SET gates is significantly smaller than that of the static complementary gates implementing the same function. This can be explained by the fact that complementary gates use more tunneling junctions than TLG gates (Fig. 1). These junctions are more sensitive to variations than simple capacitors, and hence increasing their number reduces reliability. Since the NAND and NOR gates are the simplest complementary gates, these results can be generalized to all complementary gates. These results indicate that the neural inspired TLG gates are better candidates than the static complementary gates for the SET.

Figure 7 shows the probability of failure for SET gates with different fan-in. The gates are the TLG NAND with a fan-in of two (Fig. 1(b)), the MAJ with a fan-in of three (Fig. 2(a)), and the TLG(1,1,1,2) with a fan-in of four (Fig. 2(b)). Note that NAND and MAJ gates have the same number of capacitors connected to each tunneling junction However, one of the NAND capacitors is connected to GND which makes it a bias capacitor, while the MAJ capacitor is connected to a variable input which makes it an input capacitor. The results show that the probability of failure increases with increasing fan-in, i.e. smaller simpler gates are more reliable than complex gates.
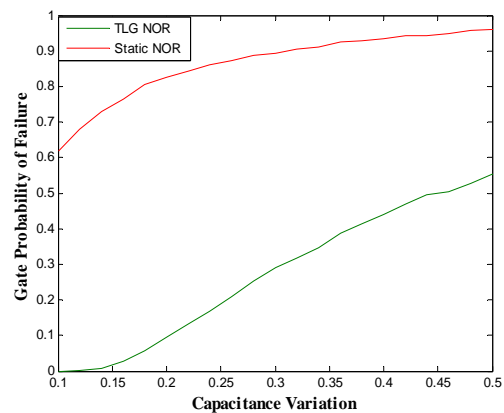

Fig. 5: Effect of implementation on the NAND gate's probability-of-failure.
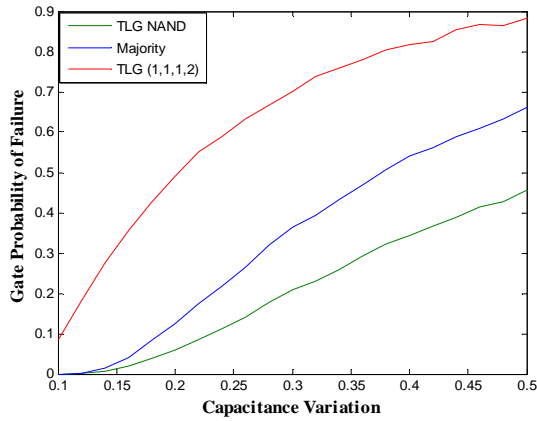

Fig. 6: Effect of implementation on the NOR gate's probability-of-failure.

Fig. 7: Effect of fan-in on the gate's probability-of - failure

Fig. 8: Probability-of-failure of SET Adders

Figure 8 shows the probability of failure for two SET adders: MAJ adder and TLG adder (shown in Fig. 4). The results show that the MAJ adder is more reliable than the TLG adder up to a variation of 0.07, while the two are similar for higher values of capacitance variations. This is a typical example of a reliability area trade-off, where the MAJ adder consists of five gates and the TLG adder of only two gates. Since TLG(1,1,1,2) has only one more capacitor than the MAJ, the MAJ adder with five gates will consume a larger area than the TLG adder. On the other hand, the MAJ gate and the inverter in the MAJ adder are simpler and more reliable than the TLG(1,1,1,2) in the TLG adder, and hence the MAJ adder proved to be more reliable than the TLG adder.

5   Conclusion

The reliability of SET gates and circuits has been investigated. The study focused on the relationship between the gate's probability of failure and the random variations affecting the elementary components (capacitors and junctions). The results show that the type of implementation strongly affects the gate's intrinsic robustness to variations. SET TLGs proved to be more reliable than static complementary SET gates implementing the same function. Regarding fan-in, the results show that the probability of failure of TLGs increases with increasing fan-in. The results of this study indicate that the neural inspired threshold logic gates are more suitable for the emerging SET technology than the static complementary gates used in current technology. At the circuit level, the larger adder with more reliable gates showed a lower probability of failure than a smaller one with less reliable gates.
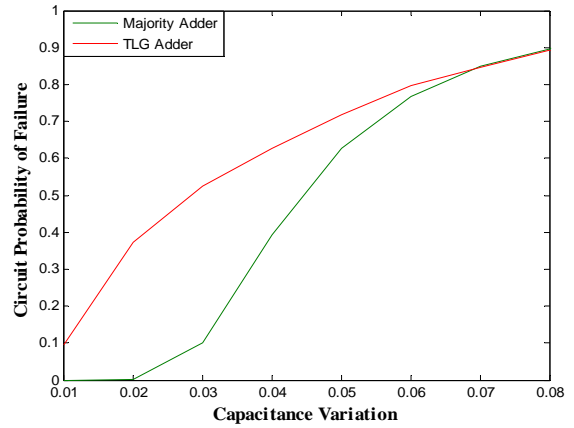
References:
[1] C. Constantinescu, "Trends and challenges in VLSI circuit reliability," *IEEE Micro*, vol. 23, pp. 14–19, 2003.
[2] W. S. Evans, and L. J. Schulman, "On the maximum tolerable noise of k-input gates for reliable computations by formulas," *IEEE Trans. Inform. Theory*, vol. 49, pp. 3094−3098, 2003.
[3] A.S. Sadek, K. Nikolić, and M. Forshaw, "Parallel information and computation with restitution for noise-tolerant nanoscale logic networks," *Nanotechnology*, vol. 15, pp. 192−210, 2004.
[4] S. Roy, and V. Beiu, "Majority multiplexing—Economical redundant fault-tolerant designs for nanoarchitectures,"*IEEETrans. Nanotechnology*, vol. 4, no. 4, pp. 441−451, 2005.
[5] M. Sulieman, and V. Beiu, "Design and Analysis of SET Circuits: Using MATLAB modules and SIMON," *IEEE-NANO conference*, Munich, Germany, pp. 317−320, Aug. 2004.
[6] J. R. Tucker, "Complementary digital logic based on the Coulomb blockade," *J. Appl. Phys.*, vol. 72, pp. 4399−4413, 1992.
[7] M. Sulieman, and V. Beiu, "On Single Electron Technology Full Adders," *IEEE Trans. Nanotechnology*, vol. 4, no. 6, pp. 669−, 2005.
[8] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON: A simulator for single-electron tunnel devices and circuits," *IEEE Trans. Comp. Aided Design*, vol. 16, pp.937, 1997.