Fabrication of Pt/$Sr_2(Ta_{1-x},Nb_x)_2O_7/SiO_2$/Si Field-Effect Transistor for One-Transistor-Type Ferroelectric Random Access Memory

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Abstract: - $Sr_2(Ta_{1-x},Nb_x)_2O_7$ (STN; x=0.3) is one of the most practical candidates for one-transistor-type ferroelectric random access memory devices. One of the most typical structures for the devices is metal-ferroelectric-insulator-semiconductor (MFIS) structure. However, the fabrication of STN on an amorphous SiO_2 (insulator) is difficult. In particular, in the case of STN, because its crystallization annealing temperature is 950˚C, the metal elements of STN and Si react with each other during crystallization annealing. As a result, perovskite STN cannot be fabricated. We have already developed STN film formation technologies on SiO_2 by ion-bombardment-assisted sputtering and introducing a thin STN seed layer treated by oxygen radicals using a microwave-excited plasma system. The IrO_2/perovskite STN (140 nm)/STN seed layer (10 nm)/SiO_2 (10 nm)/Si device shows square hysteresis curves and a memory window of 1.7 V under an 8 V writing operation. Furthermore, we have fabricated and operated the Pt/STN (140 nm)/STN seed layer (10 nm)/SiO_2/Si field-effect transistor for the first time. The drain current (I_d)-gate voltage (V_d) [I_d-V_g] characteristics show counterclockwise hysteresis curves due to ferroelectric polarization switching.

Key-Words: - ferroelectric random access memory (FeRAM), one-transistor-type ferroelectric memory, non volatile memory, metal-ferroelectric-insulator-semiconductor (MFIS) structure, MFIS field-effect transistor, ferroelectric film, perovskite $Sr_2(Ta_{1-x},Nbx)_2O_7$ (perovskite STN)

1 Introduction

Recently, nonvolatile memory devices having ferroelectric gate structure have attracted much attention from the viewpoints of high speed, nondestructive readout, and high-density memory LSIs. Metal-ferroelectric-insulator-Si (MFIS) and metal-ferroelectric-metal-insulator-Si (MFMIS) FETs are widely researched, as shown in Fig. 1. In this structure, since a ferroelectric capacitor and an insulator capacitor are connected in series, the voltage applied to the ferroelectric film becomes small when the ferroelectric film has a high dielectric constant [1], as shown in Fig. 2. Thus, a ferroelectric film with a low dielectric constant is advantageous for low voltage operation of the devices. Furthermore, hydrogen atmosphere processes such as the passivation process degrade the properties of ferroelectric films. Such degradation is also enhanced by the catalytic effect of Pt for hydrogen reaction [2].

$Sr_2(Ta_{1-x},Nb_x)_2O_7$ (perovskite STN; x=0.3) is one of the most practical candidates for MF(M)IS structure devices. STN has attracted considerable attention as a bismuth-and lead-free ferroelectric material having a low dielectric constant and a small remanent polarization [3], [4], [5]. STN is the $Sr_2Nb_2O_7$ (SNO) family ferroelectric material, which are $A_2B_2O_7$ type oxide compounds with a perovskite slab structure. The crystal structure of SNO is shown in Fig. 3. A spontaneous polarization occurs along the c-axis. The characteristics of STN film formed on Pt/IrO_2 substrate have been reported for MFMIS structure devices [1]. The values of the remanent polarization and the coercive field are 0.5 μC/cm^2 and 44 kV/cm, respectively. The film has a low dielectric constant of 53. Furthermore, we have already

obtained a remanent polarization of 0.6 μC/cm^2 and a coercive field of 59 kV/cm by controlling the crystal orientation of a STN flm by introducing an IrO_2 substrate [6]. The film has a very low dielectric constant of 35.

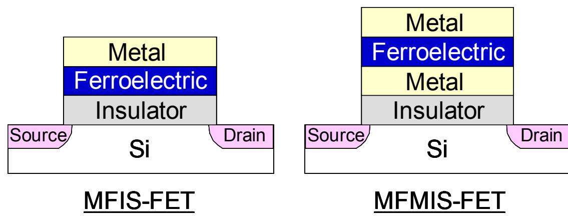
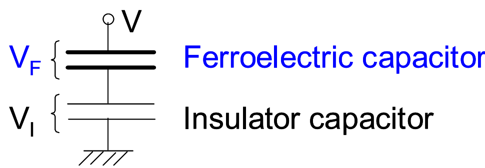


Fig. 1 Schematic cross sections of MFIS-FET and MFMIS-FET.



V: applied gate voltage
(V is split into the ferroelectric and insulator capacitor)
V_F: voltage applied to the ferroelectric capacitor
V_I: voltage applied to the insulator capacitor

Fig. 2 Equivalent circuit of MF(M)IS structure devices.

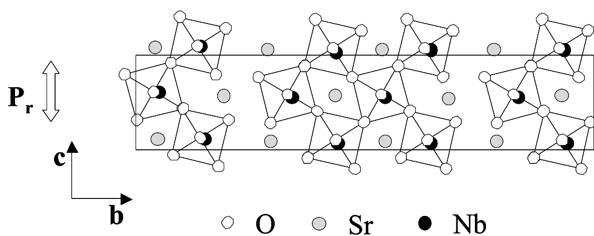


Fig. 3 Crystal structure of SNO family ferroelectric.

For applications using MFIS FETs, crystallization of ferroelectric film on insulator is necessary. However, it is difficult to fabricate STN on an amorphous insulator such as SiO_2, because STN has a high crystallization annealing temperature of 950˚C. When SiO_2 is introduced as an insulator, the $Sr_3(Ta_{1-x},Nb_x)_6Si_4O_{26}$ phase was formed by crystallization annealing at 950˚C and perovskite STN was not obtained [7]. For overcoming this problem, it is effective to oxidize STN film with oxygen radicals using a microwave-excited plasma system (oxygen radical treatment). We have already reported STN formation technology on amorphous SiO_2, and perovskite STN has been successfully obtained by ferroelectric-multilayer-scack (FMLS) deposition, that is, alternating steps of rf-sputtering deposition and oxygen radical treatment (O* treatment) [8]. This result shows that it is very important to reduce oxygen vacancy in the STN films by the use of oxygen radicals to obtain the perovskite STN phase. We have also successfully formed perovskite STN on an O*-treated STN seed layer/SiO_2/Si by ion-bombardment-assisted sputtering, that is, a large Kr ion bombardment energy of 38 eV can be provided to the film surface during the rf-sputtering deposition [9]. IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/Si device whose STN was formed by ion-bombardment-assisted sputtering showed square hysteresis curves of capacitance-voltage (C-V) characteristics due to ferroelectricity and a memory window of 1.7 V under an 8 V writing operation.

For developing ferroelectric gate FET memory devices with MFIS structure, formation of MFIS FET with STN is desirable. However, fabrication of the MFIS FET with STN was not achieved. Thus, in this paper we report the formation and the operation of Pt/STN/O*-treated STN seed layer/SiO_2/p-type Si FET.

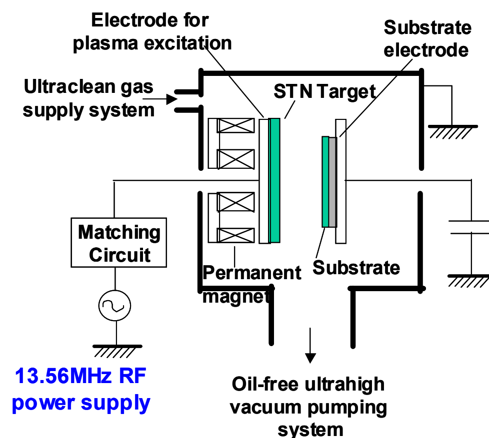


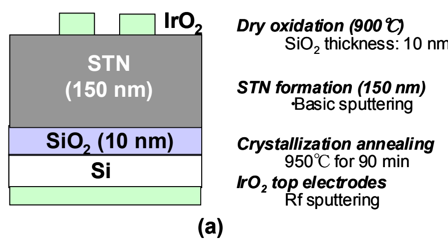
Fig. 4 Rf-sputtering system for STN film deposition.

2 Formation of perovskite STN on SiO_2

Figure 4 illustrates the rf-sputtering system used for STN film deposition. Details of the rf-sputtering conditions are shown in Table I. For applications using metal-ferroelectric-insulator-semiconductor (MFIS) FETs, crystallization of ferroelectric film on insulator is necessary. However, it is difficult to fabricate STN on an amorphous insulator such as SiO_2, because STN has a high crystallization annealing temperature of 950˚C. When SiO_2 is introduced as an insulator, the $Sr_3(Ta_{1-x},Nb_x)_6Si_4O_{26}$ phase is formed by crystallization annealing at 950˚C, that is, perovskite STN cannot be obtained [7].

Table I. RF-sputtering conditions of STN films.

	basic condition	**Ion-bombardment-assisted condition**
Gas	Kr/O_2	Kr/O_2
Rf frequency (MHz)	13.56	13.56
Rf power (W): R_I Working pressure (Pa): P_W (R_I, P_W)	(14, 4)	**(18, 20)**
Ratio of O_2 partial pressure to total working pressure (%)	6	6
Substrate voltage	Floating	Floating
Substrate temperature	RT	RT



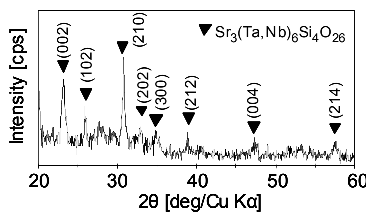


Fig. 5 Device structure image and process flow of IrO_2/STN/SiO_2/Si device (a) and XRD patterns of STN formed on SiO_2 (b).

Figure 5 shows the X-ray diffraction (XRD) measurement results [7] of STN formed on SiO_2. 150 nm STN was deposited on SiO_2 under the basic condition (as shown in Table I) and it was crystallized by annealing in oxygen molecular ambient at 950˚C for 90 min. The pattern indicates the growth of a $Sr_3(Ta_{1-x},Nb_x)_6Si_4O_{26}$ phase. This result indicates that, for forming STN by conventional rf sputtering (basic condition), the metal elements of the STN film diffuse into the substrate, or Si diffuses into the STN film. They react with each other because of the high crystallization annealing temperature of 950˚C.

2.1 STN formation by newly developed plasma process

For ion-bombardment-assisted condition, both rf power (R_I) and working pressure (P_W) during STN sputtering deposition were increased so that the deposition rate should not be different from that of the basic sputtering condition. The deposition rate was 11 Å/min. The reason for employing a constant deposition rate was to make the migration rate of the ferroelectric elements constant. The mixing ratios of $O_2/(Kr+O_2)$ during STN sputtering were fixed at 6%.

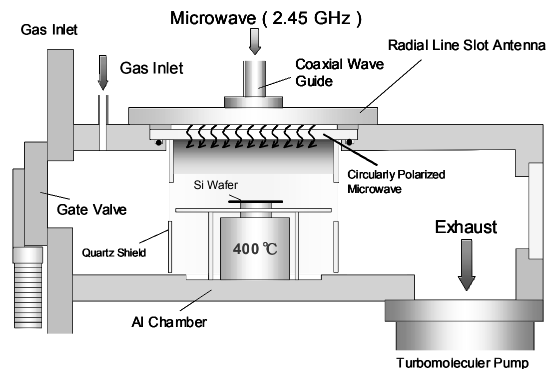


Fig. 6 Microwave-excited high-density plasma system.

Figure 6 shows the microwave-excited (2.45 GHz) high-density ($>10^{12}$ cm^{-3}) low-electron-temperature (< 1 eV) Kr/O_2 plasma system for ferroelectric film improvement. This system is characterized by a low ion bombardment energy (ε_i) of less than 7 eV, a high plasma density above 10^{12} cm^{-3}, a low electron

temperature below 1 eV, and an excellent uniformity of less than 1% on a 300-mm-diameter wafer. This system can effectively oxidize STN from a surface to a depth of 17 nm or more at 400˚C (O* treatment). During microwave-excited plasma treatment (O* treatment), the mixing ratios of O_2/(Kr+O_2) and working pressure were 1% and 133 Pa (1 Torr), respectively. The substrate temperature was 400˚C.

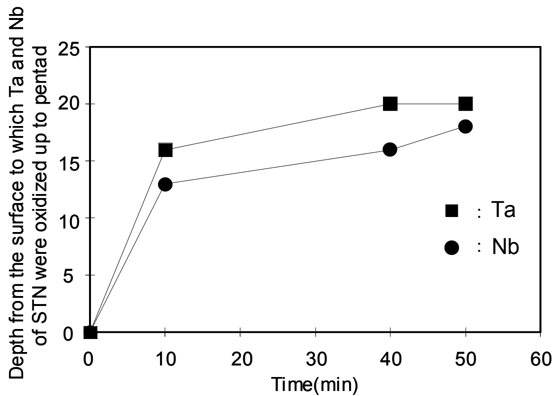


Fig. 7 Depth from the surface to which Ta and Nb of STN were oxidized up to pentad as function of O* treatment time.

Figure 7 shows the depth from the surface to which Ta and Nb of STN were oxidized up to pentad (Ta_2O_5, Nb_2O_5) as a function of O* treatment time [10]. This result shows that O* treatment for 10 min can oxidize Ta and Nb of STN to a depth of 16 and 13 nm from the surface of the film, respectively. This means that we have developed a technology that can oxidize ferroelectric STN film at very low temperature of 400˚C. On the other hand, we have reported that annealing in the oxygen molecular ambient at 950˚C could not oxidize STN films at all [10]. It is effective to oxidize ferroelectric film by use of oxygen radicals whose atomic radius is smaller than those of molecular oxygen. The results also show that oxidation of Nb is more difficult than that of Ta. This reason is that the ionization energy of Nb is larger than that of Ta. This result also indicates that it is effective to use oxygen radicals that are very active to oxidize STN film.

2.2 IrO_2/STN/STN seed layer/SiO_2/Si device whose STN was formed by ion-bombardment-assisted sputtering and O* treatment

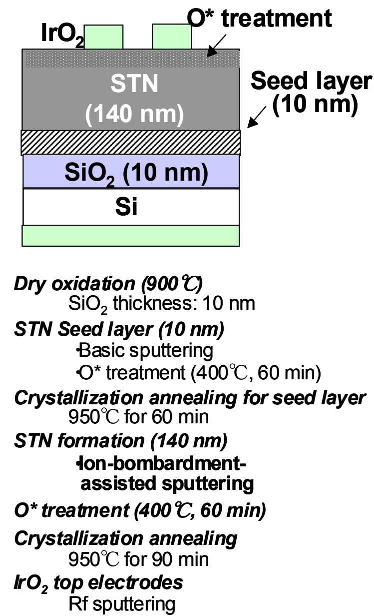


Fig. 8 Device structure image and process flow of IrO_2/STN/O*-treated STN seed layer/ SiO_2/Si device.

Figure 8 (a) shows the device structure images and process flows of the IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/Si device whose STN was formed by ion-bombardment-assisted sputtering. The sputtering conditions of the seed layer were the basic condition with (R_I, P_W) of (14 W, 4 Pa), and it was treated by oxygen radicals using a microwave-excited high-density plasma system. For 140 nm STN deposition, the conditions of (R_I, P_W) were (18 W, 20 Pa), naming it ion-bombardment-assisted conditions. This film was crystallized by annealing in molecular oxygen gas ambient at 950˚C for 90 min.

The XRD patterns in Fig. 9 (a) show that the peaks of perovskite STN such as (111), (151) and (172) appear, and that the peaks of $Sr_3(Ta_{1-x},Nb_x)_6Si_4O_{26}$ disappear [9]. This means that only perovskite STN is fabricated, and introducing STN seed layer treated by oxygen radicals and STN deposition by ion-

bombardment-assisted sputtering is effective for obtaining the perovskite STN phase. Figure 9 (b) shows the C-V characteristics of the IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/Si device [9]. The device shows square hysteresis curves and a memory window of 1.7 V under an 8 V writing operation. This value corresponds to a coercive field of 55 kV/cm. This means that we have successfully developed a technology of perovskite STN formation on amorphous SiO_2 with the same large coercive field as that of STN formed on an IrO_2 film [6].

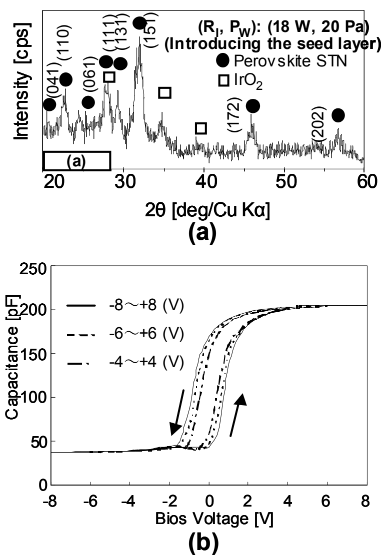


Fig. 9 XRD patterns of STN (140 nm)/O*-treated STN seed layer (10 nm) on SiO_2 at (R_I, P_W) of (18 W, 20 Pa) (a) and C-V characteristics of IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2/Si device whose STN was formed at (R_I, P_W) of (18 W, 20 Pa) (b) .

3 MFIS FET

3.1 Fabrication of the IrO_2/STN/STN seed layer/SiO_2/Si FET

Figure 10 shows a schematic cross section of the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2/p-type Si FET. On a p-type Si substrate, n^+ regions for the source and drain (S/D) were fabricated. For ion implantation, As^+ with its energy of 25 keV was implanted to the source and drain regions at the dose of 2.5×10^{15} cm^{-2}. Activation annealing for S/D was performed by furnace in Ar gas ambient at a temperature of 950˚C for 30 min, and the protection oxide film was formed on the Si surface with the switch of the gas from Ar to O_2, as it was. Non-silicated glass (NSG) for etching-stop in the gate etching process was formed by normal pressure CVD. After lithography and wet etching of NSG, SiO_2 of 10 nm thicknesses was formed by dry oxidation at a temperature of 900˚C. STN of 10 nm thickness for the seed layer was formed by ion-bombardment-assisted sputtering at an (R_I, P_W) of (18 W, 20 Pa) and then it was treated by oxygen radicals for 60 min at a substrate temperature of 400˚C. Annealing for crystallization of the seed layer was performed in O_2 gas ambient at 950˚C for 60 min. STN of 140 nm thickness was formed by ion-bombardment-assisted sputtering at the same conditions. Pt of 80 nm thickness was formed on the STN by rf sputtering. NSG for the hard mask in the gate etching process was formed on Pt by normal pressure CVD. After lithography and dry etching for gate patterning, NSG was deposited again. After contact etching for S/D region and gate electrodes, Al was deposited by vacuum evaporation.

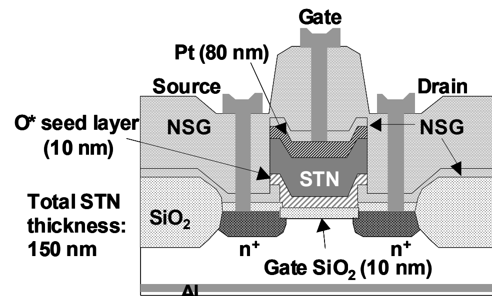


Fig. 10 Schematic cross section of the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/p-type Si FET.

3.2 Characteristics of the IrO_2/STN/STN seed layer/SiO_2/Si FET

Figure 11 shows the drain current (I_d)-gate voltage (V_g) [I_d-V_g] characteristics for the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2/p-type Si FET with 100 μm-long and 200 μm-wide gate. The gate voltage was scanned from a negative

voltage to a positive voltage and back to the negative starting voltage. Concretely, V_g was scanned from 0 ± 3 V to 0 ± 7 V, where the center of V_g was fixed at 0 V. The drain voltage was kept at 0.05 V. The source voltage (V_s) and substrate voltage (V_{sub}) were 0 V. The I_d-V_g curves of the FET show that on-state and off-state of I_d was controlled by V_g, indicating that the operation of a FET was successfully achieved. The I_d-V_g curves also show counterclockwise hysteresis curves due to ferroelectricity.

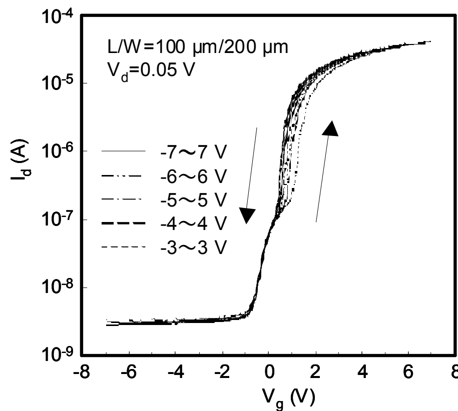


Fig. 11 Drain current (I_d)-gate voltage (V_g) [I_d-V_g] characteristics for the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/p-type Si FET.

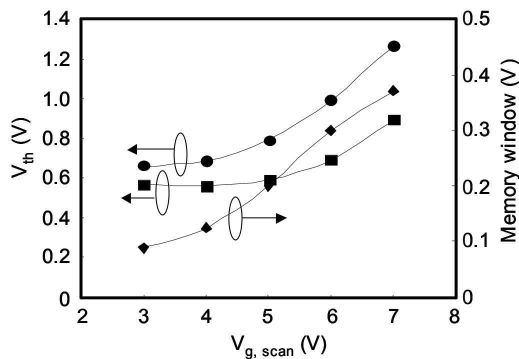


Fig. 12 Threshold voltages (V_{th}) and memory windows as function of writing operation gate voltage ($V_{g,scan}$) for I_d-V_g characteristics of the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/ p-type Si FET.

Figure 12 shows threshold voltages (V_{th}) and memory windows as function of writing operation gate voltage ($V_{g,\ scan}$) for I_d-V_g characteristics of the fabricated Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/p-type Si FET. The maximum memory window is 0.4 V under 7 V writing operation. The memory windows of I_d-V_g curves are smaller than those of C-V hysteresis curves of Fig. 9 (b). In fig. 12, the V_{th} that is obtained by writing operation from positive to negative voltage increases with amplitude of $V_{g,\ scan}$. This is a reason why the expected values of the memory windows are not obtained. The detailed mechanism of increase of the V_{th} is not understood at the present stage. However, we have fabricated and operated the Pt/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/p-type Si FET (MFIS-FET with STN) for the first time.

4 Conclusion

We have successfully oxidized ferroelectric STN film by oxygen radical treatment using our developed microwave-excited plasma system. Ta and Nb of STN can be oxidized up to pentad (Ta_2O_5, Nb_2O_5) at very low temperature of 400°C. O* treatment for 10 min can oxidize Ta and Nb of STN to a depth of 16 and 13 nm from the surface of the film. We have successfully formed perovskite STN films on amorphous SiO_2 by introducing the O*-treated STN seed layer and using ion-bombardment-assisted sputtering. The IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/Si device whose STN was formed by ion-bombardment-assisted sputtering showed square hysteresis curves and a memory window of 1.7 V under 8 V writing operation. On the basis of these experimental results and our developed technologies, we have fabricated IrO_2/STN (140 nm)/O*-treated STN seed layer (10 nm)/SiO_2 (10 nm)/p-type Si FET whose STN was formed by ion-bombardment-assisted sputtering. The I_d-V_g characteristics of the FET show that on-state and off-state for I_d was controlled by V_g, indicating that the operation of a FET was successfully achieved. The I_d-V_g curves also show counterclockwise hysteresis curves due to ferroelectricity. This means that we have successfully fabricated and operated the MFIS FET with STN for the first time [11], [12].

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