# A Programmable Voltage Reference Design

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*Abstract* – **The paper emphasizes the circuit innovations of a key analog function realized on the IAD GmbH DLC _2 family chip, a precision programmable voltage reference with superior performance capabilities dedicated for an integrated 10 bits D/A converter. The chip developed in co-operation of IAD and MAZ Brandenburg has been produced with 0.35μm CMOS switched capacitor technology from AMS, it can be used on the one hand within typical power-line applications, such us controlling and management, and the other hand for data communication, such as telephony or internet access.**
**The programmable voltage reference is based on a new design that provides fast programmability between voltages and stable voltage operation from 0.25Vdda to 0.75Vdda. The main objective is to select a design that meets as close as possible criteria related to the chip specification requirements such as reliability, flexibility, and integration area. Consequently, an adequate programmable voltage reference is proposed which is 4 bits decoder-based converter architecture.**

## I. INTRODUCTION

Networks can easily be built with help of the existing power-line network management system [1], which is based on a master-slave concept using repeaters to increase the range of the network, where every slave can also be a repeater. Therefore, using power-line telecommunication exploits power-line infrastructure and avoid synergy with home power-line networking. A power-line modem allows devices to communicate using ordinary power-lines as the transmission media. Its main functional blocs are a transmitter and a receiver. Typically, an A/D and D/A converters are integrated to interface respectively the receiver to an analog signal and the transmitter to the digital one. They are the main links between the analog signals and the digital worlds of signal processing.

A wide variety of DAC architectures exist, from very simple to complexes ones, each of them have its own merits and limits. Perhaps the most straightforward approach for realizing N-bit D/A converters is to create $2^N$ reference signals and pass the appropriate signal to the output, depending on the digital word. It is referred to such D/A converters as decoder-based converters. They are based on selecting one tap of a segmented resistor string by a switch network [2]. The output signal quality of such converters is one to one related with the reference voltage. Consequently, the important analog building bloc in data acquisition systems is a voltage reference. Ideally this bloc will supply a fixed dc voltage of known amplitude that does not change with temperature. There have been a number of approaches that have been taken to realize voltage references in integrated circuits [3].

Specific programmable voltage reference cell based on the decoder-based converter architecture have been designed and integrated on the chip. It is required to set two reference voltages for the sampled inputs of the DAC to be compared to. The on-chip D/A converter is developed on basis of the circuit concept of the standard cell DAC 10 of AMS. The DAC changes 10 bits into an analog value with each clock (7MHz) within a gain range from –7 dB to 0 dB in 1 dB step. The accuracy of the reference voltage needs to be as linear as the converter itself. The developed voltage reference is built with standard 0.35 μm AMS CMOS switched capacitor technology. This technique uses charge storage on rationed capacitors and allows the design high speed and low power circuits.

In this paper, the enhanced programmable voltage reference architecture based on miniaturized digital to analog converter (DAC) dedicated for a high resolution D/A converter will be described.

At first, the principal of the suggested voltage reference will be explained and the final implementation will be presented. Then, the simulation results will be given to verify circuit performance. Finally, the layout consideration and implementation will be discussed.

## II. CIRCUIT DESCRIPTION

In our project, it is important that the design is both precise and accurate as possible. Because of the accuracy required, it is important for reference to exhibit long-term stability and insensitivity to temperature variations. There are many different techniques to generate highly accurate output voltages from a voltage reference [4], [5], [6]. The circuit principle for developing the programmable voltage reference is illustrated in figure 1. It consists of a resistor chain and a binary switch array whose inputs are a binary word. The analog output is the voltage division of the resistors following via pass switches.

The voltage reference uses the three bit input (B0, B1, B2) to control the transmission gate network that selects two of the reference voltages, which are transferred to the outputs Vout1 and Vout2. The delay through the switch network is the major limitation on speed. To achieve a higher speed implementation in our design, logic is used for the decoder, and a MUX is connected to a single resistor string node.

The integrated programmable voltage reference "Vref_DAC" generates $2^4$ unequal reference voltages distributed between 0.75 Vdda and 0.25 Vdda for each gain values. The proposed concept for the programmable voltage reference schematic is shown in figure 2. The new design consists of a resistor chain with unequal 16

resistors, two symmetrical MUX, 4 bits decoder and two buffers. The code loaded to the "Vref_DAC" decoder determines at which node on the string the voltages are tapped off to be fed into the output amplifiers. The voltage is tapped off by closing one of the switches of each MUX connecting the string to the amplifiers. Because it is a string of resistors, it is guaranteed monotonic. Notice that there will be two low impedance paths between the resistor string and the input of the buffers, and those paths is determined by the digital input word.

"Vref_DAC" has two symmetrical reference outputs: positive reference voltage "vrefp" and negative reference voltage "vrefn", which define the dynamic range of the DAC output signals.

The design with not matching resistors is used to keep the minimum gain error below 0.25 dB.

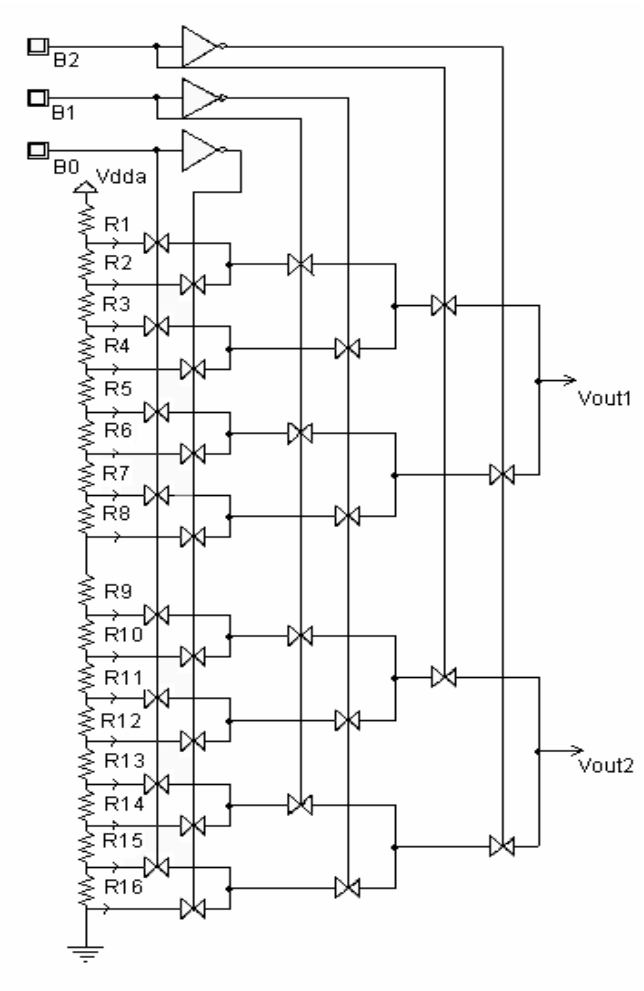


Fig. 1. Programmable reference voltage Principle Design

## *Buffers*

The output buffers are high quality CMOS amplifier for high capacitive load (1.6 to 2.2μF). They are need for buffering the reference voltages of the ADC and the *DAC*.

The first one "buffer_vrefp" is developed for the buffering of the positive voltages. The open loop characteristics of the opamp can be found in figure 3. A gain of 87 dB with a unity gain bandwidth of 535KHz and a phase margin of 61 degrees are confirmed through simulations for a capacitive load of 1.6μF.

The second high gain and high bandwidth amplifier "buffer_vrefn" is needed for the buffering of the negative voltage. It is developed to determine the goal. Both amplifiers provide low offset voltage and low noise.

## *Ana_mux8cell*

To transmit the reference voltage from the resistor chain into the buffer, two Ana_mux cells are used. This analog multiplexer cell has 8 inputs; it is built using 8 transmission gates. This cell is used to select one of the positive/negative reference voltages. It uses a decoder to select which input line gets sent to the output.

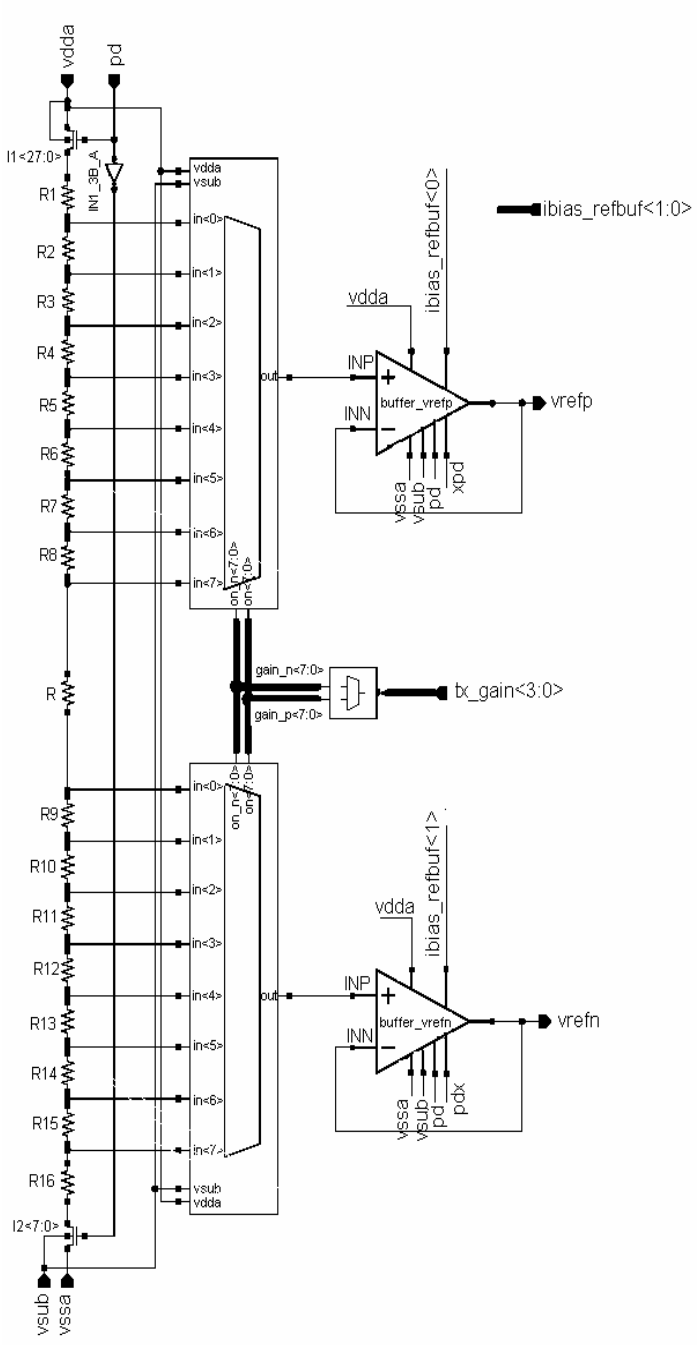


Fig. 2. Programmable reference voltage circuit diagram

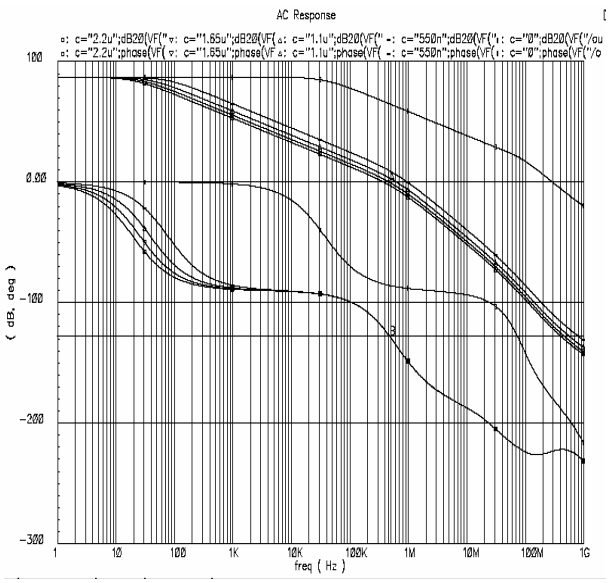


Fig. 3. Magnitude and phase Bode plot

*TX_gain_decoder*

The tx_gain_decoder cell is a 4-to-16 decoder. It uses an input address to select two of many possible outputs. All of the outputs are used to select which positive reference voltages gets sent to the first buffer and which negative reference voltages gets sent to the second one.

## III. SIMULATION RESULTS

The new high performance programmable voltage reference based upon switched capacitor technology has been designed and simulated with the Cadence Analog Artist tool using the CMOS 0.35 μm technology from AMS. It must be able to generate several reference voltages indicated by the binary encoded equivalent.
Simulation of the programmable voltage reference shown in figure 4 shows a regular decrease of the positive output voltage vrefp and a regular increase of the negative output voltage vrefn with the output combinations from 000 (vrefp=2.475V and vrefn= 0.825V) to 111 (vrefp=2.019V and vrefn= 1.281V).

From the simulation results, it appears clearly that an integral non-linearity exists which corresponds to the difference between the ideal and actual value of the output, for some values of the digital word. The origin of this non_linearity is the resistor chain design, which does not create perfectly regular resistor values; the $R_{ON}$ of the transmission gates, which has a not negligible value; and the buffer offset voltages. Also, process fluctuation may affect the value of the resistor, which is one other source of non-linearity. Still, further improvements in accuracy are expected with taken into account all those non-ideal effects. The conclusion is that the deviation from the ideal voltages is tolerable.

The different available reference levels are shown in table1, table2 and table3. Table 1 gives the value of vrefp and vrefn versus the input code with vdda=3.3V and T=27°C. In table 2, the simulated results of the programmable voltage reference design with vdda=3.6V and T=-40°C can be found. Furthermore, Table 3 represent the different reference voltages values with vdda=3V and T=105°C.

To reduce the power consumption of the programmable voltage reference cell, it is necessary to be able to turn off the cell when it is not needed.

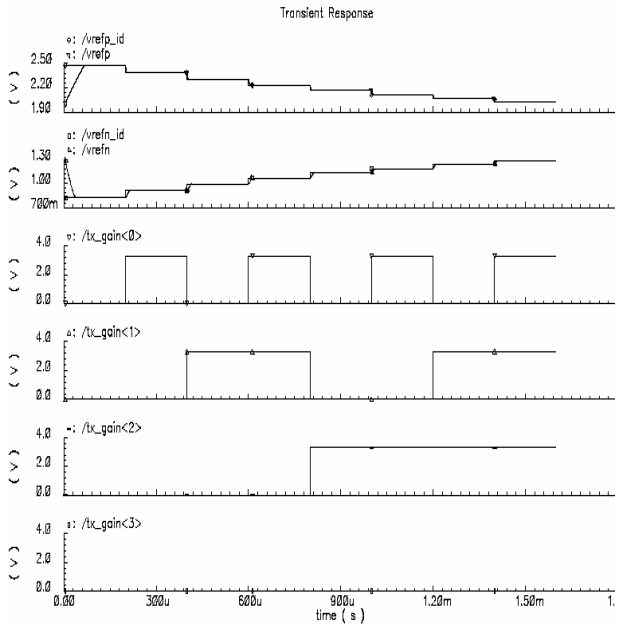


Fig. 4. Simulation of the programmable voltage reference

TABLE 1
( vdda=3.3V, T=27°C, $C_L$ = 1.6 pF)

| Gain[dB] | db_sel[ ] | vrefp[V] | vrefn[V] | Vout_diff[V] |
|---|---|---|---|---|
| 0 | 000 | 2.475 | 825m | 1.649 |
| -1 | 001 | 2.386 | 915m | 1.470 |
| -2 | 010 | 2.306 | 995m | 1.310 |
| -3 | 011 | 2.234 | 1.066 | 1.168 |
| -4 | 100 | 2.171 | 1.129 | 1.041 |
| -5 | 101 | 2.114 | 1.186 | 0.928 |
| -6 | 110 | 2.064 | 1.236 | 0.827 |
| -7 | 111 | 2.019 | 1.281 | 0.738 |

TABLE 2
( vdda=3.6V, T=-40°C, $C_L$ = 1.6 pF)

| Gain[dB] | db_sel[ ] | vrefp[V] | vrefn[V] | Vout_diff[V] |
|---|---|---|---|---|
| 0 | 000 | 2.701 | 899m | 1.801 |
| -1 | 001 | 2.603 | 997m | 1.605 |
| -2 | 010 | 2.516 | 1.085 | 1.431 |
| -3 | 011 | 2.438 | 1.163 | 1.275 |
| -4 | 100 | 2.369 | 1.232 | 1.137 |
| -5 | 101 | 2.307 | 1.294 | 1.013 |
| -6 | 110 | 2.252 | 1.349 | 0.903 |
| -7 | 111 | 2.203 | 1.397 | 0.806 |

TABLE 3.
( vdda=3V, T=105°C, $C_L$ = 1.6 pF )

| Gain[dB] | db_sel[ ] | vrefp[V] | vrefn[V] | Vout_diff[V] |
|---|---|---|---|---|
| 0 | 000 | 2.250 | 751m | 1.498 |
| -1 | 001 | 2.169 | 833m | 1.336 |
| -2 | 010 | 2.096 | 905m | 1.190 |
| -3 | 011 | 2.031 | 970m | 1.061 |
| -4 | 100 | 1.974 | 1.028 | 0.946 |
| -5 | 101 | 1.922 | 1.079 | 0.843 |
| -6 | 110 | 1.877 | 1.125 | 0.752 |
| -7 | 111 | 1.836 | 1.166 | 0.670 |

## IV. LAYOUT DESCRIPTION

This paper is attempted to present and analyse the new design architecture based on decoder-based converter principle. The integrated programmable voltage reference circuit structure has been simulated, verified and successfully implemented with a double poly 0.35µm AMS CMOS process that ensures high functionality with low power dissipation.

The layout realisation of the programmable voltage reference discussed in this paper is illustrated in figure 6. The physical layout is occupied 0.099mm$^2$. The resistor string circuit takes up the center portion of the layout. It consists of four long strip of polysilicon with equal widths. The use of polysilicon resistors that have a resistivity of around 20-30 (ohms per square) can improve accuracy. The resistor string layout is composed of 21 elements of unequal lengths connected in series as illustrated in figure 5. However, the use of not matching resistors eliminates the problem of mismatch between resistors.

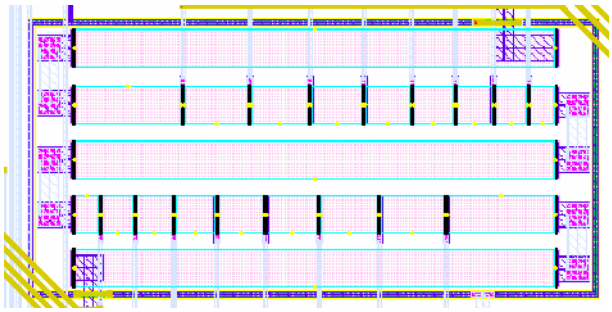

Fig. 5. Resistor string Layout

The positive buffer and the first MUX take up the right half of the circuit layout. Furthermore, the negative buffer and the second MUX take up the left-hand side of the layout. The decoder is located in the center-lower half. Moreover, in order to realize a high quality circuit, appropriate layout techniques are used and special care has been taken [7], [8], [9].

The performance characteristics of the complete programmable voltage reference are broadly summarized bellow:

TABLE 4.
CIRCUIT SPECIFICATIONS

| Parameter design | Values |
|---|---|
| Pos. Analog power supply range Vdda | 3.3V(+3V - 3.6V) |
| Neg. Analog power supply Vssa | 0 Volts |
| Vsub | 0 Volts |
| Reference voltages range | 0.25vdda to 0.75vdda |
| Temperature range | -40 to 105°C |
| Bias current ($I_{BIAS}$<1:0>) | <10.5,10.5>µA |
| Programmable Voltage Reference size | 230µm*432µm |
| Technology | 0.35µ double-poly CMOS AMS |

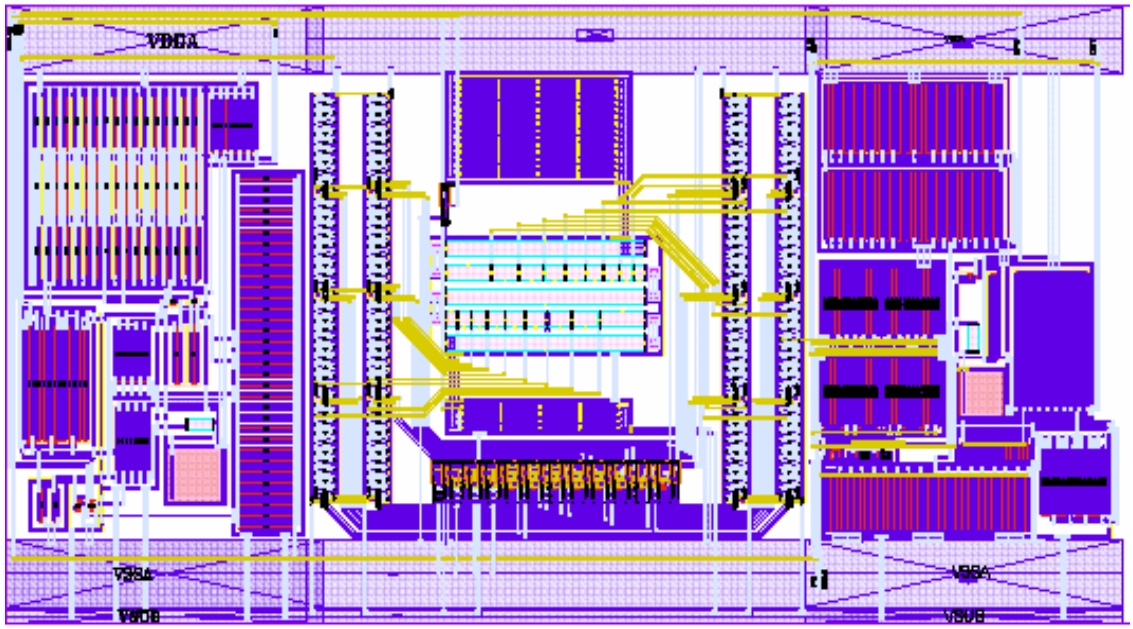


Fig. 6. Programmable voltage reference circuit Layout

## V. CONCULSION

Since reliability, speed, accuracy and power consumption were important parameters to overcome; the proposed programmable voltage reference "Vref_DAC" is the most appropriate choice for our application. It has been selected between different possibilities to closely satisfy the criteria.

The "Vref_DAC" cell is designed for single supply operation from 3 V to 3.6 V. It is characterized for operation from -40°C to 105°C. The level of the reference voltages can be set in a range from 0.75Vdda to 0.25Vdda. The "Vref_DAC" combines low drift and noise with excellent long-term stability and high output accuracy.

## VI. REFERENCES

[1] Markus Sebeck and Gerd Bumiller; "A Network Management System for Power-line Communications and its Verification by Simulation"; IAD GmbH, Germany, ISPLC 2000

[2] Adib R. Hamadé, "A Single Chip All-MOS 8-Bit A/D Converter", 786 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-13, NO. 6, DECEMBER 1978

[3] David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons Inc, first edition, 1997.

[4] Yannis P. Tsividis and Richard W. Ulmer, "A CMOS Voltage Reference", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-13, N. 6, December 1978

[5] Jim McCreary, "Precision Floating-Gate Voltage Reference»; IIC-China/ESC-China 2004, Conference Proceedings 97

[6] *Alan Rich;* "Voltage Reference Application and Design Note»; Application Note

[7] Kadaba R. Lakshmikumar Robert, A. Hadaway and Miles A. Copeland; "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design»; IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, NO. 6, DECEMBER 1986

[8] Marcel L J. M. Pelgrom, and C. J. Duinmaijer Andanton P. G. Welbers; "Matching Properties of MOS Transistors»; IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989

[9] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2000

[10] Gerd Bumiller and Manfred Deinzer. "Narrow Band Power-line Chipset for telecommunication and Internet Application", *IAD* GmbH, Unterschlauersbacher-hauptstr. 10, D-90613 Großhabersdorf, Germany