An Averaged Switch Model Including Conduction Losses for Boundary Conduction Mode Dc-to-Dc Converters

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Abstract − In this paper, following the averaged switch approach, an averaged model, including conduction losses for the switch network of the pulse width modulated (PWM) dc-to-dc converters operating at the boundary between continuous conduction mode (CCM) and discontinuous inductor current mode (DICM) is developed. The model is verified through PSpice and CASPOC simulation for the boost converter. The averaged model is general, and can be applied to different dc-to-dc converters, without deriving a different averaged switch network model for each converter configuration.

1 Introduction

Averaged switch models are powerful tools for studying the behaviour of PWM dc-dc converters.

In [1] an averaged model for CCM dc-dc converters, including switch conduction losses and an averaged model for lossless DICM dc-dc converters are described.

An averaged switch model for lossless dc-to-dc converters operating at the boundary between CCM and DICM is described in [2].

In this paper an averaged model for dc-to-dc converters operating at the boundary between CCM and DICM, including conduction losses is developed.

The real diode is modeled, using the classical approach, as an ideal diode in series with a constant voltage source V_D and a linear resistor R_D. The transistor is modeled as an ideal switch in series with a resistor R_{on}. The real inductor is modeled as an ideal inductor in series with a resistor R_L.

The averaged switch model for boundary conduction mode (BCM) dc-to-dc converters, including conduction losses is derived in Section 2. The PSpice and CASPOC implementation of the model is presented in Section 3. In Section 4 the model is verified through PSpice and CASPOC simulation. Some conclusions are presented in Section 5. The PSpice netlists of the averaged model and of the circuit used for simulation are presented in the Appendix.

2 Averaged Switch Model for BCM Dc-to-Dc Converters, Including Conduction Losses

The system under study consists of a boost converter, controlled such as the transistor is turned on when the diode current equals zero, and turned off when the peak transistor current reaches a

desired value [2]. The switching period in this operating mode is variable.

As it is known, for the capacitor voltage v_C the negligible ripple assumption is still valid in BCM and therefore it can be admitted constant during one switching cycle, T_s.

Let us examine the BCM operation of the boost converter. In the first subinterval, while the transistor conducts, the inductor current increases from zero until it reaches the peak value equal to the control input, i_c, when the transistor is turned off and the diode starts to conduct. In the second subinterval the inductor current decreases form the peak value until it reaches zero, when the transistor is turned on again.

The terminal variables i_1, i_2, v_1 and v_2 of the switch network are defined in Fig. 1.
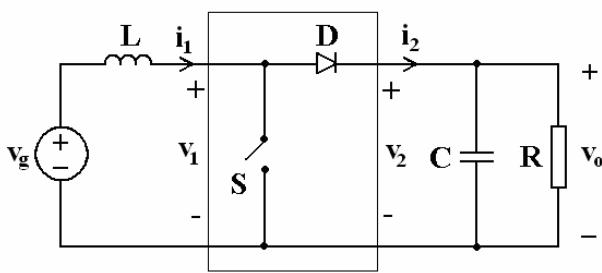

Fig. 1. The boost converter, with the switch network identified.

The equivalent circuits of the boost converter in the two topological states when BCM operated are shown in Fig. 2.
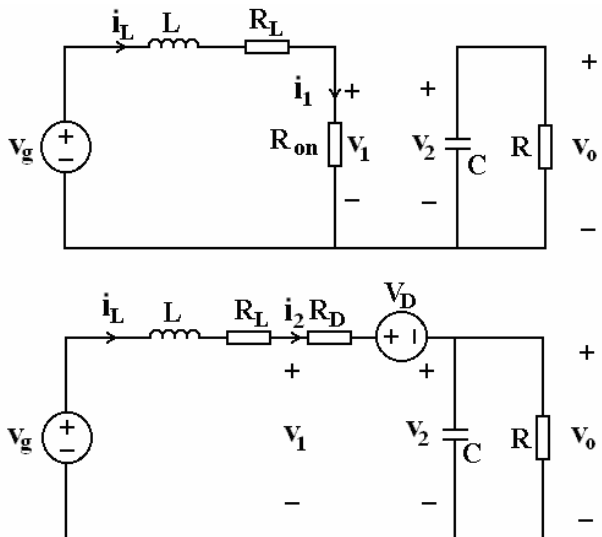

Fig. 2. The topological states of BCM boost converter.

Due to the non-ideal components, the inductor current waveform is not triangular, as in case the

components were ideal. In fact, the inductor current rises and falls exponentially, as shown in Fig. 3, and its peak value, i_c, is smaller compared to the lossless situation.
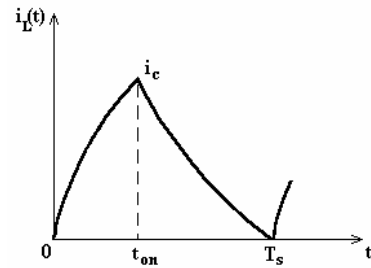

Fig. 3. The inductor current waveform.

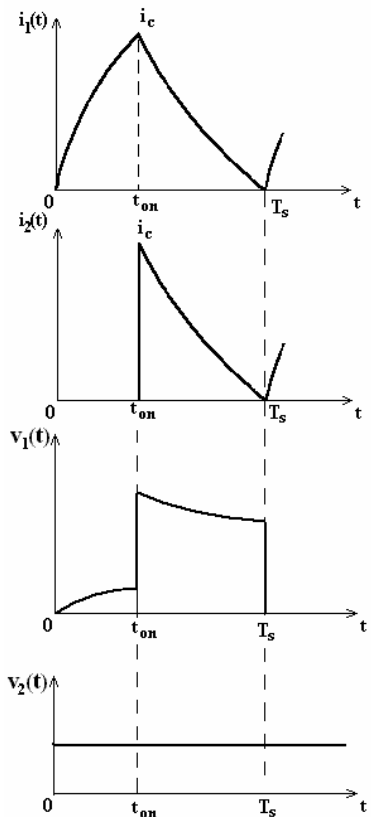The switch network voltage and current waveforms are presented in Fig. 4.

Fig. 4. The waveforms for the switch network variables.

During the transistor on-time $(0 - t_{on})$ the switch network input current, i_1 is equal to the inductor current, i_L. The switch network variables are given by:

$$i_1(t) = i_L(t) = \frac{v_g}{R_{on} + R_L}\left(1 - e^{-\frac{R_{on}+R_L}{L}t}\right) \quad (1)$$

$$i_2(t) = 0 \quad (2)$$

$$v_1(t) = R_{on}i_1(t) \quad (3)$$

$$v_2(t) = v_o \qquad (4)$$

When $t = t_{on}$ the inductor current equals i_c and, therefore, from Eqn. (1) the peak value of the inductor current, i_c, can be obtained as:

$$i_c = i_L(t_{on}) = \frac{v_g}{R_{on} + R_L}\left(1 - e^{-\frac{R_{on}+R_L}{L}t_{on}}\right) \qquad (5)$$

From Eqn. (5) the transistor on-time, t_{on} can be obtained as:

$$t_{on} = -\frac{L}{R_{on} + R_L}\ln\left[1 - \frac{i_c(R_{on} + R_L)}{v_g}\right] \qquad (6)$$

The denominator in the logarithm, v_g, is the inductor voltage in the first subinterval. It can be shown that the same applies to the buck and buck-boost converters.

During the second subinterval, $(t_{on} - T_s)$ the switch network variables are given by:

$$i_1(t) = i_L(t) = \frac{v_g - v_o - V_D}{R_D + R_L} + \\ + \left(i_c - \frac{v_g - v_o - V_D}{R_D + R_L}\right)e^{-\frac{R_D+R_L}{L}(t-t_{on})} \qquad (7)$$

$$i_2(t) = i_L(t) = \frac{v_g - v_o - V_D}{R_D + R_L} + \\ + \left(i_c - \frac{v_g - v_o - V_D}{R_D + R_L}\right)e^{-\frac{R_D+R_L}{L}(t-t_{on})} \qquad (8)$$

$$v_1(t) = v_o + V_D + R_D i_2(t) \qquad (9)$$

$$v_2(t) = v_o \qquad (10)$$

The transistor off-time can be determined from the condition $i_L = 0$ at the end of the second subinterval:

$$t_{off} = \frac{L}{R_D + R_L}\ln\left[1 - \frac{i_c(R_D + R_L)}{v_g - v_o - V_D}\right] \qquad (11)$$

The expression $v_g - v_o - V_D$ is the inductor voltage in the second subinterval, considering only V_D and neglecting resistive losses. The same applies to the buck and buck-boost converters. With this observation, the expressions of t_{on} and t_{off}, obtained for the boost converter, can be generalized for buck and buck-boost converters operating in BCM:

- for the buck converter:

$$t_{on} = -\frac{L}{R_{on} + R_L}\ln\left[1 - \frac{i_c(R_{on} + R_L)}{v_g - v_o}\right] \qquad (12)$$

$$t_{off} = \frac{L}{R_D + R_L}\ln\left[1 - \frac{i_c(R_D + R_L)}{-v_o - V_D}\right] \qquad (13)$$

- for the buck-boost converter:

$$t_{on} = -\frac{L}{R_{on} + R_L}\ln\left[1 - \frac{i_c(R_{on} + R_L)}{v_g}\right] \qquad (14)$$

$$t_{off} = \frac{L}{R_D + R_L}\ln\left[1 - \frac{i_c(R_D + R_L)}{-v_o - V_D}\right] \qquad (15)$$

The switching period can be computed as:

$$T_s = t_{on} + t_{off} \qquad (16)$$

The derivation of the averaged model can be simplified, by making some approximations. Of course, the precision of the model is decreased. One approximation that can be made is to consider that the waveform of i_L is linear, while using the exact values of t_{on} and t_{off}. Using this approximation, by averaging the waveforms in Fig. 4 over one switching cycle the averaged switch network variables are found as:

$$\begin{cases} <i_1(t)> = \dfrac{<i_c(t)>}{2} \\[2mm] <i_2(t)> = \dfrac{t_{off}}{T_s}\dfrac{<i_c(t)>}{2} \\[2mm] <v_1(t)> = <i_1(t)>\left(\dfrac{t_{on}}{T_s}R_{on} + \dfrac{t_{off}}{T_s}R_D\right) + \\[2mm] \qquad\qquad + \dfrac{t_{off}}{T_s}(V_D + <v_2(t)>) \\[2mm] <v_2(t)> = <v_o(t)> \end{cases} \qquad (17)$$

Based on the Eqns. (17), the averaged circuit model of the switch network can be constructed, as shown in Fig. 5:
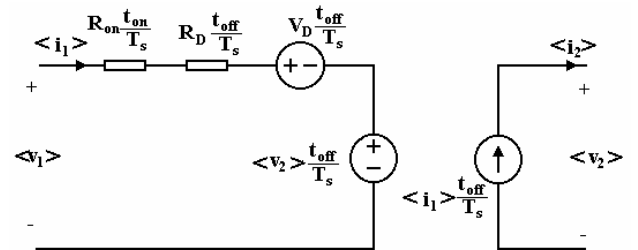

Fig. 5. The large signal averaged switch model for BCM with conduction losses.

The averaged model is general, and can be applied to different converters, without deriving a different averaged switch network model for each converter configuration, which is a very useful feature for simulation. The only model parameter

that depends on the converter configuration is the ratio t_{on}/T_s.

3 Implementation of the BCM Averaged Switch Model Including Conduction Losses in Circuit Simulators

A PSpice subcircuit implementation of the model given by Eqns. (6), (11), and (17) is given in the Appendix.

The first subcircuit is used to compute t_{on}/T_s. The inputs of this subcircuit are: the control input v(ctr), and inductor voltages v(1) and v(2) for the two subintervals, considering zero voltages dropson loss resistors. The output of the subcircuit is v(5), which is used in the second subcircuit as t_{on}/T_s. The second subcircuit has six nodes: the control input v(ctr), the node 5 which represents t_{on}/T_s, the nodes 1 and 2 representing the input port of the switch network, and the nodes 3 and 4 representing the output port.

The averaged model can be also implemented in CASPOC. The library block is shown in Fig. 6.
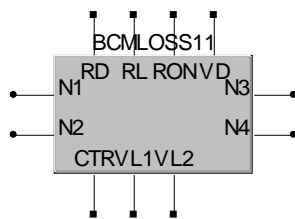

Fig. 6. CASPOC library block implementing the BCM averaged switch model.

The terminals N1 and N2 are the input terminals of the switch network. N3 and N4 are the output terminals. CTR is the control input, VL1 and VL2 are the inductor voltages (neglecting the losses). RD, RL, RON and VD are the losses.

In Fig. 7 is shown one possible implementation for the library block. The EXPRESSION blocks are used to compute: the values of the two controlled sources, $<i_2>$, and $<v_1>$, the arguments of the logarithm in Eqns. (6) and (11), and the ratio t_{on}/T_s. The LIM block limits the value of t_{on}/T_s to (0.01, 0.99).
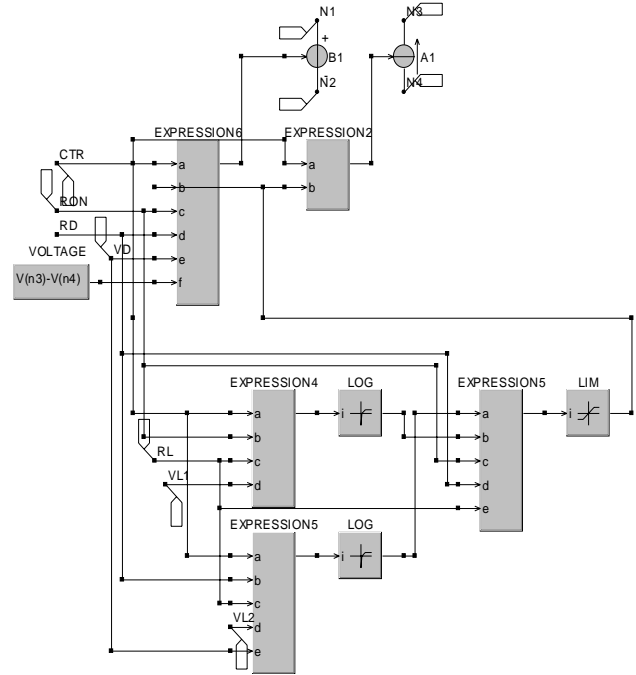

Fig. 7. One possible realization of the library block implementing the BCM averaged model.

To construct the averaged circuit model of a converter, the switch network has to be simply replaced by the library block.

4 Simulation Results

The investigated boost converter has the following circuit parameters: V_g=20V, L=250μH, C=15μF, R=70Ω, i_c=1.68A.

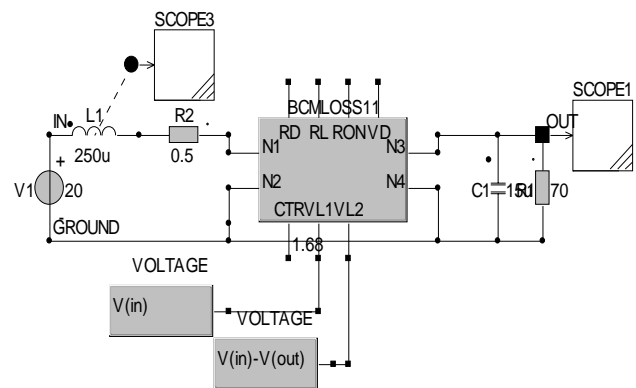In Fig. 8 the averaged circuit model used in CASPOC simulation is shown.

Fig. 8. The BCM averaged boost converter used in CASPOC simulation.

First, the averaged model, given by Eqn. (17) is applied to the converter to study the steady state performances compared to the switching circuit. The

PSpice simulated waveforms of the output voltage, considering conduction losses (R_{on} = 0.2Ω, R_D = 0.11Ω, R_L = 0.1Ω, V_D=0.8V) are shown in Fig. 9.
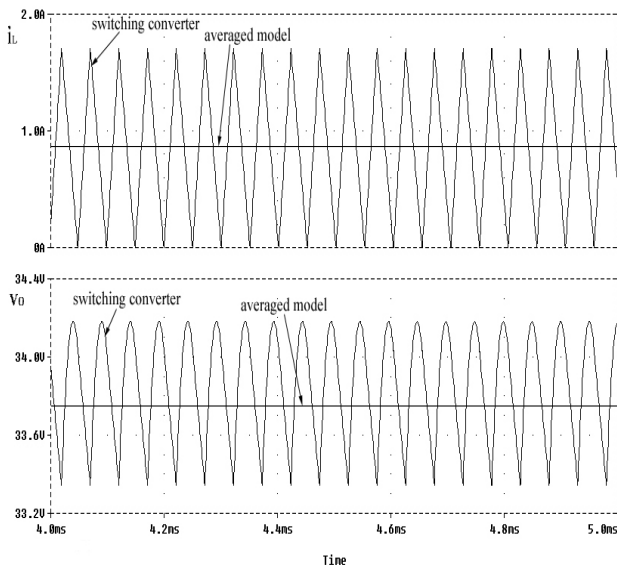

Fig. 9. Steady state inductor current and output voltage waveforms obtained by PSpice simulation of the switching converter and by simulating using the proposed averaged circuit model.

Then the model is applied to the boost converter, considering large conduction losses (R_{on} = 0.5Ω, R_D = 0.61Ω, R_L = 0.5Ω). The results for the output voltage V_o and efficiency η, are compared to those obtained by simulating the switching circuit and compared also to the values obtained using the lossless model described in [2]. The results are presented in Table 1. The errors introduced by the averaged model are also determined. The same results were obtained using PSpice and CASPOC simulation.

Table 1. The output voltage and the efficiency for the boost converter.

		V_o	error	η
Small losses	Switching circuit	33.716V	-	96.5%
	Averaged model	33.72V	0.01%	96.6%
	Lossless averaged model [2]	33.67V	0.14%	100%
Large losses	Switching circuit	32.93V	-	91.8%
	Averaged model	33.13V	0.6%	92.5%
	Lossless averaged model [2]	33.67V	2.2%	100%

The results confirm the accuracy of the model.

The model can also be used in transient simulation. The output voltage and inductor current waveforms during start-up transient are shown in Fig. 10. For comparison, the waveforms obtained by CASPOC simulation of the switching circuit and by simulating the averaged circuit are shown. It can be observed that the low-frequency component of the waveforms obtained by simulating the averaged circuit matches very closely with the waveforms obtained by simulating the switching circuit.
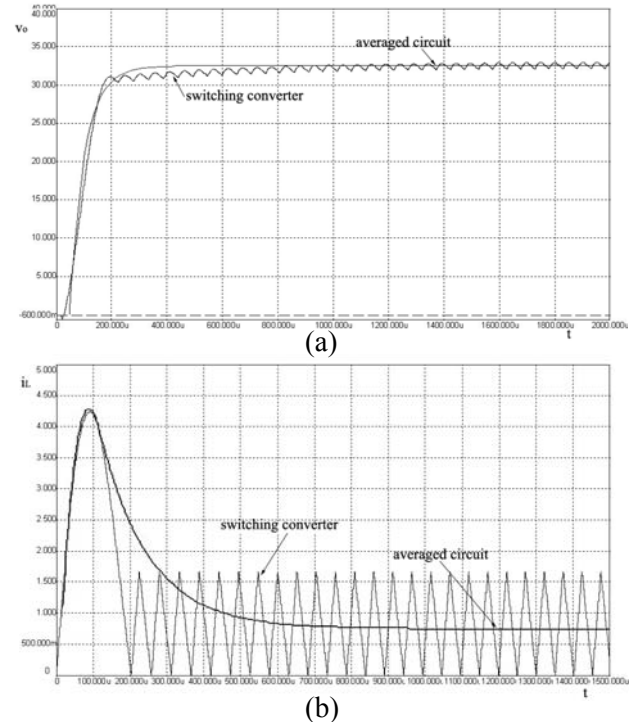

(a)

(b)

Fig. 10. (a) Output voltage waveform and (b) inductor current waveform obtained by transient simulation of the switching converter and by simulation of the proposed averaged circuit model.

5 Conclusions

In this paper a PWM switch model including conduction losses, for Boundary Conduction Mode (BCM) dc-dc converters is developed.

The averaged model can be easily absorbed in a PSpice subcircuit or a CASPOC library. Because of its generality it can be used in many different converters, without deriving a different averaged switch network model for each converter configuration. This is a very useful feature for constructing averaged circuit models for simulation and in calculating efficiency and different averaged values. Compared to the switching circuits simulation, the averaged circuits simulation can be completed much faster.

The averaged model was verified on a boost converter for steady state analysis. The model was also verified in a transient simulation.

The simulation results confirmed the accuracy of the model.

6 Appendix

Netlist of the PSpice subcircuit implementation of the model given by Eqns. (6), (11), and (17):

```
*****************************************
.subckt BCMLOSS1 ctr 1 2 d
+params: RL=1 Ron=1 RD=1 VD=1
*
*generate d
*
Eduty d 0 table
+{1/(1-(Ron+RL)*log(1-v(ctr)*(RD+RL)/
+v(2))/(RD+RL)/log(1-v(ctr)*(Ron+RL)/
+v(1)))} (0.01 0.01) (0.99 0.99)
*
.ends
*****************************************


*****************************************
.subckt BCM2 1 2 3 4  ctr 5
+params:Ron=0 VD=0 RD=0
Er 1 2 value={v(ctr)/2*(Ron*v(5)+(1-v(5))*
+RD)+(1-v(5))*(v(3,4)+VD)}
Gd 4 3 value={(1-v(5))*v(ctr)/2}
.ends
*****************************************


Netlist of the PSpice circuit used for simulation:

BOOST bcm with conduction losses
.param fs=50kHz
.param L=250uH
.param VD=0.8
.tran 1u 1m 0m 1u
.lib bcm2.lib
```

```
.lib bcmloss.lib
Vg 1 0 dc 20V
L  1 2x {L}
RL 2x 2 0.5
Xswitch 2 0 3 0 6 5 bcm2
+PARAMS: Ron=0.5 VD={VD} RD=0.61
Rload 3 0 70
C1 3 0 15uF
Xswitch1 6 7 8 5 bcmloss1
+params: RL=0.5 Ron=0.5 RD=0.61 VD={VD}
V1 6 0 1.68
E1 7 0 value={v(1)}
E2 8 0 value={v(1)-v(3)-VD}
.probe
.end
```

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[6] CASPOC - *Reference Manual*, Simulation Research, 1999.