Charge Loss Measurement under illumination in Single-Poly One-Time-Programming Floating Gate Non-Volatile-Memories

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Abstract : -Charge loss in single poly OTP FG-NVM embedded in a smart power circuit is studied under illumination. It is found that the leakage current is due to photo-field emission for both intrinsic and extrinsic cells. The two types of cells can be discriminated from aging experiment at near room temperature. The acceleration factor is much higher than during bake at high temperature.

Key-Words : - non volatile memories, photo-field emission, reliability, charge loss, screening test

1 Introduction

Charge loss in floating gate non volatile memories (FG-NVM) is one of the main issues affecting reliability [1]. For some applications requiring highly secure systems a near-zero-defect reliability level is needed which implies extensive reliability testing and screening to remove all defective or potentially defective units. In addition during the development of a new product wafer level reliability testing with fast feedback is useful. In both cases very fast reliability testing is needed and this is a real challenge as far as data retention is concerned.

In order to reduce the test time the most widely used method is to perform temperature accelerated life-tests for charge retention capability [1]. According to this method for a given charge loss criterion, failure rates at high temperature (200°C – 300°C) are extrapolated to the operating conditions using the well known Arrhenius law. However the method is questionable regarding the validity of the extrapolation law [2] and possible defects annealing can lead to data retention overestimation [3]. Furthermore the test is always very long, typically several hundred hours even at the highest temperature.

Charge loss in non volatile semiconductor memories may have various origins: degradation of the parameters of the intrinsic conduction mechanism (barrier lowering, local insulator thinning, interface roughness), carrier detrapping, trap-assisted leakage current (SILC) and/or contamination.

As OTP-NVM are cycled a few times only during preliminary testing, carrier detrapping and SILC are not of primary concern. Consequently charge loss is mainly due to degraded intrinsic conduction mechanisms and acceleration may be obtained by heating carriers in the floating gate to higher energies. This may be obtained either by an increase of the test temperature or by illumination with photons of energy less than the polysilicon-insulator barrier height.

In this paper we propose a new method for accelerated charge loss characterization which can be applied at the wafer level and at the operating temperature (near room temperature). Acceleration is obtained by illumination of the polysilicon floating gate with visible light (λ > 400nm). Of course the floating gate must be free of metallic overlayer and the method applies particularly to embedded memories of moderate density. This acceleration method for charge loss in memories has already been proposed [4] but not for floating gate memories and for different loss mechanisms. So it is necessary to check the validity of the method in the case of a FG-NVM.

Light absorption in the floating gate of a single-poly One-Time-Programming FG-NVM has been studied and it is shown that the penetration depth of incident photons in the degenerate polysilicon is large enough to interact with carriers at the polysilicon-tunnel oxide interface. Charge loss under illumination in both intrinsic and extrinsic cells has been studied and equivalence of the acceleration method with the thermal one has been obtained.

2 Experimental Procedure

The studied memory cell was a single-poly NVM cell with a classical architecture embedded in a smart power

circuit with a 35 nm thick gate oxide and no metal line above both the NMOS transistors and the coupling capacitors.
Large area capacitors have also been obtained with the same process. Program and erase operations were by the Fowler-Nordheim tunneling effect. Samples with 10^4 memory cells from an engineering lot were first cycled 10 times, programmed and measured for the cells threshold voltage V_T. Then each sample has been submitted to a bake at a temperature of 25°C, 125°C, 150°C, 200°C, 250°C and 300°C during up to 7000h. The bake was sequentially stopped after given periods for V_T measurement. Some cells have been individually identified as intrinsic or extrinsic following their place in the cumulative distribution. These cells have been illuminated (λ_1= 514 nm, P_1= 30 mW/cm^2 and λ_2= 488 nm, P_2= 5 mW/cm^2). In all the experiments the leakage current has been determined from the variations of the threshold voltage V_T.

3 Results and discussion

3.1 Charge loss during bake in intrinsic cells

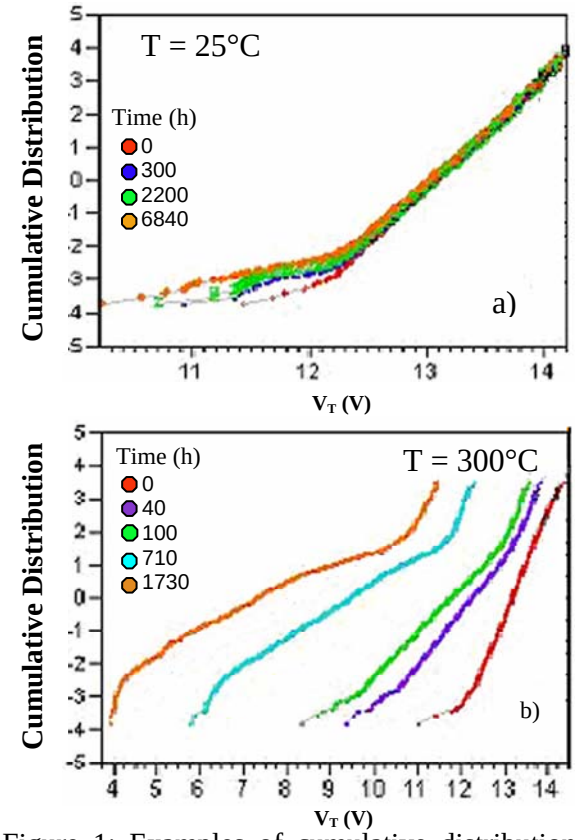

Figure 1: Examples of cumulative distribution after various bake times.

Cumulative distribution of V_T for the two extreme temperatures are illustrated in Fig.1.
The distributions do not show any particular feature. The large spread of more than 2V of the initial distribution is due to the large thickness of the gate oxide. As usually the curves show two parts: one with the highest slope is attributed to non defective cells, the second one with a shape depending upon the temperature is due to defective cells.

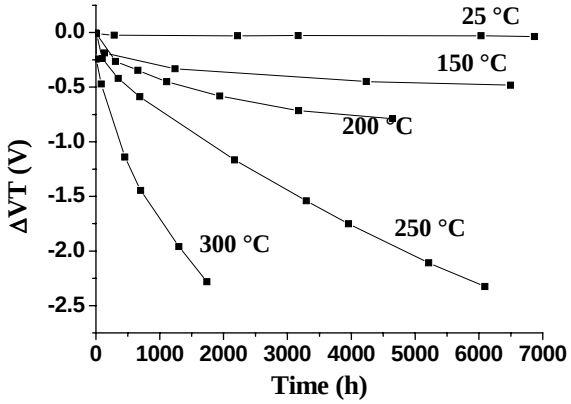

Figure 2: Variation ΔV_T of cells threshold voltage with bake time and temperature.

We have followed the evolution with time of several cells in the first part of the distribution and Fig. 2 shows an example at each temperature.
Then the data have been fitted by the least square fit technique and the leakage current I_l versus the floating gate voltage V_{FG} has been extracted by the formulae:

$$I_l = -C_C \, dV_T/dt \qquad (1)$$
$$V_{FG} = \alpha_C \, V_T \qquad (2)$$

Where C_C and α_C are the control gate-floating gate capacitor and the coupling factor of the cell respectively.

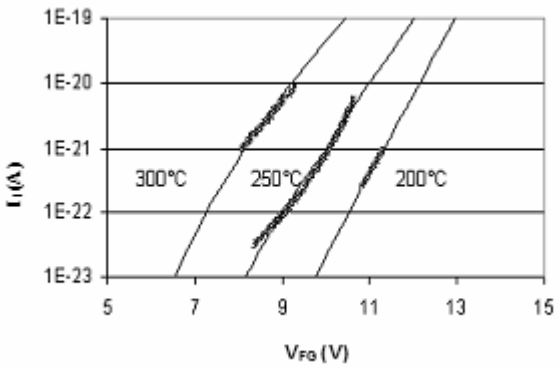

Figure 3: Leakage current versus floating gate voltage. Experimental (symbols) and theoretical (curves) results.

For a temperature less than 200°C the V_T variation was too small to extract the current. For a higher temperature the current-voltage curves are shown in Fig. 3 together with theoretical results considering a charge loss due to the Fowler-Nordheim (FN) conduction through the tunnel insulator.

The influence of the temperature T on the FN conduction has been studied in [5]. The conduction is well described by the following relation:

$$J_{FN} = AT \int_0^{\phi} D(F,E) Ln\left(1+\exp\left(\frac{E_f(T)-E}{kT}\right)\right) dE \quad (3)$$

$$D(F,E) = \exp\left(B\frac{(\Phi-E)^{3/2}}{F}\right) \quad (4)$$

Using a barrier height Φ linearly dependent upon the temperature [3,6,]

$$\Phi = \Phi_0 - \beta T \quad (5)$$

where A and B are constants independent of the temperature, E_f the Fermi level, F is the electric field in the insulator, E is the carriers energy, k the Boltzman constant, D(E) the transmission coefficient of the floating gate-tunnel oxide barrier and Φ_0 the value of Φ at 0 °K. The FN current and its temperature dependence have been studied with the large area capacitors. Φ_0 and β have been found equal to 3.23 eV and 0.55 mV/°K respectively.

Considering the results in Fig. 3 and the method used to obtain the leakage current the agreement between experimental and simulated results are satisfactory. Consequently the loss mechanism in intrinsic cells is Fowler-Nordheim tunnelling through the transistor and coupling capacitor oxides as expected.

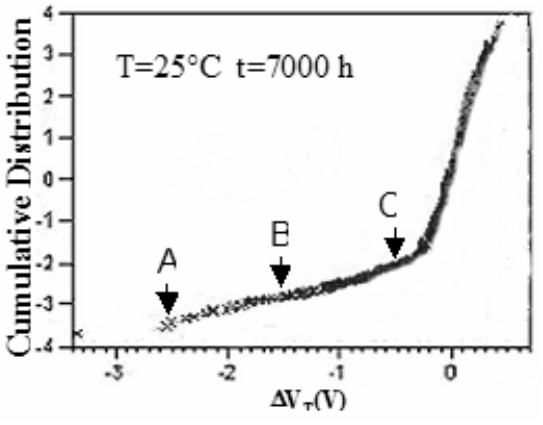

Figure 4: Cumulative distribution of the threshold voltage variation after aging at room temperature during 7000 h.

3.2 Charge loss during bake in extrinsic cells

In the case of extrinsic cells the same procedure has been applied. For bake temperatures of 250°C and 300°C the leakage current plotted in a Fowler-Nordheim graph did not show any linear part, thus eliminating charge loss due to Fowler-Nordheim tunnelling as previously, but showed linear variations in both a Poole-Frenkel and a Poole graphs. This situation has been encountered and studied in [7] where it was shown however that the squared theoretical to experimental Poole-Frenkel ratio was between one and two in contrast to a value between 1 and 5 found in this work depending upon temperature and cell. So during a bake at a temperature higher than 200°C the charge loss mechanism is not clearly identified.

However at a lower temperature the leakage current of extrinsic cells is large enough to be measured by the same procedure and in particular at room temperature which is the most interesting case for the purpose of the paper. Fig. 4 shows the threshold voltage shift distribution after aging at room temperature and the position of three selected cells in the extrinsic part of the curve referenced as A, B and C. The leakage currents associated with these cells are shown in Fig. 5 together with calculation of the Fowler-Nordheim current using adjusted values of the barrier height Φ to obtain the best fit to the experimental results. The values of Φ are given in Table 1.

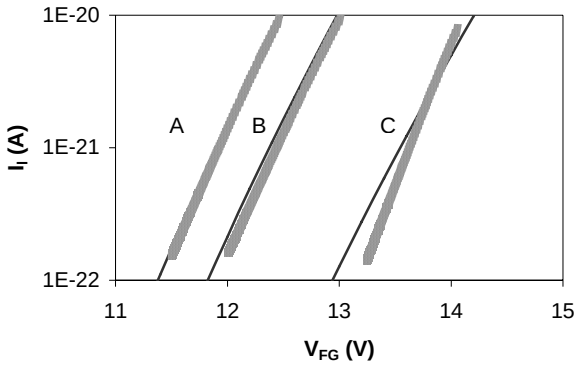

Figure 5: Leakage current versus floating gate voltage of selected extrinsic cells during aging at room temperature. Experimental (symbols) and theoretical (curves) results.

Cell	Φ (eV)
A	2.77
B	2.8
C	2.85

Table 1: Room temperature barrier height values for extrinsic cells

As previously, the agreement is satisfactory indicating that at room temperature charge loss is due to Fowler-Nordheim tunnelling through the tunnel oxide with distributed values for the associated barrier height.
The same results have been obtained during bake at 200 °C with room temperature barrier height values ranging from 2.7 eV to 3 eV.

3.3 Charge loss under illumination

3.3.1 Light transmission through the floating gate

In order to accelerate charge loss, photons must excite carriers in the floating gate close to the floating gate-tunnel insulator interface. We have studied the transmission spectrum through the floating gate using a structure as shown in Fig. 6 where the substrate has been etched so that visible light is absorbed in the floating gate polysilicon layer only. The spectrum of

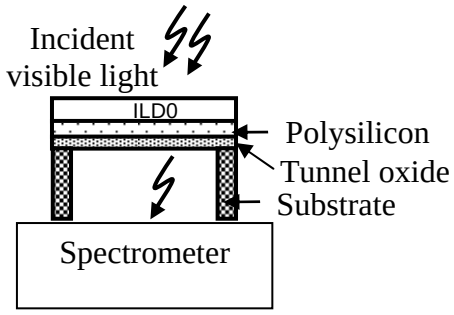

Figure 6: Structure used to study light transmission through the polysilicon layer.

the transmitted light normalised to the incident one is shown on Fig. 7 which indicates that in the wavelength range used in this study [480nm-520nm] more than 10% of the incident flux reaches the polysilicon-tunnel oxide interface.

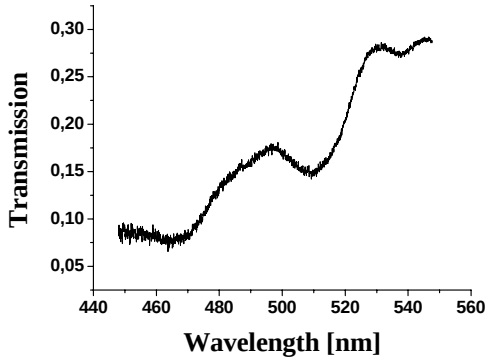

Figure 7: Transmission spectrum through the floating gate layer.

This is in agreement with results obtained in [8] where the absorption coefficient in degenerate polysilicon is 3-5 10^4 cm^{-1} in the same wavelength range so that 15-20 % of the incident light can reach the tunnel oxide.

3.3.2 Photo-field emission

Conduction under illumination through an interfacial semiconductor-insulator barrier has been studied in [9]. The mechanism responsible of the conduction is photo-field emission (PFE). A simplified model has been developed in which electrons are first excited by photons, then they migrate towards the interface within a diffusion length and finally they cross the interfacial barrier as depicted in Fig. 8

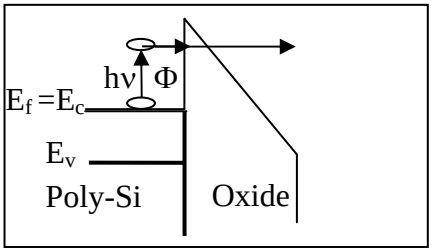

Figure 8: Photo-field emission mechanism

The photo-field emission current is similar to the FN current with a barrier height reduced by the photon energy. It can be written:

$$J_{PFE}(\Phi, h\nu) = N\nu\Gamma J_{FN}(\Phi - h\nu) \qquad (5)$$

Where hν is the photon energy and Nνγ a constant dependent upon the incident photons flux and the electron-photon interaction probability.

3.3.3 Conduction in intrinsic cells during illumination

Cells detected as intrinsic during bake have been erased then reprogrammed and illuminated. During illumination V_T has been sequentially recorded and Fig 9 a) shows its variation with time. The time scale compared with that in Fig. 2 put into evidence a drastic acceleration.
The leakage current associated with this variation is represented in Fig. 9 b) together with the result of equation (5). The fit has been obtained by adjustment of the effective barrier height $\Phi_{eff} = (\Phi - h\nu)$ and of the prefactor Nνγ. Values of Φ_{eff} were 0.77 eV and 0.64 eV for 514 nm and 488 nm respectively, corresponding in both cases to a barrier height of 3.18 eV or to a value Φ_0 of 3.34 eV considering a mean temperature of the cell of 35 °C measured with an infrared camera during illumination. This value is close to that found during the thermal measurement (3.23 eV). So as a summary, under illumination the leakage current in intrinsic cells is due to photo-field emission i.e. to a Fowler-Nordheim type conduction as in the case of a bake but with a barrier height reduced by the photons energy.

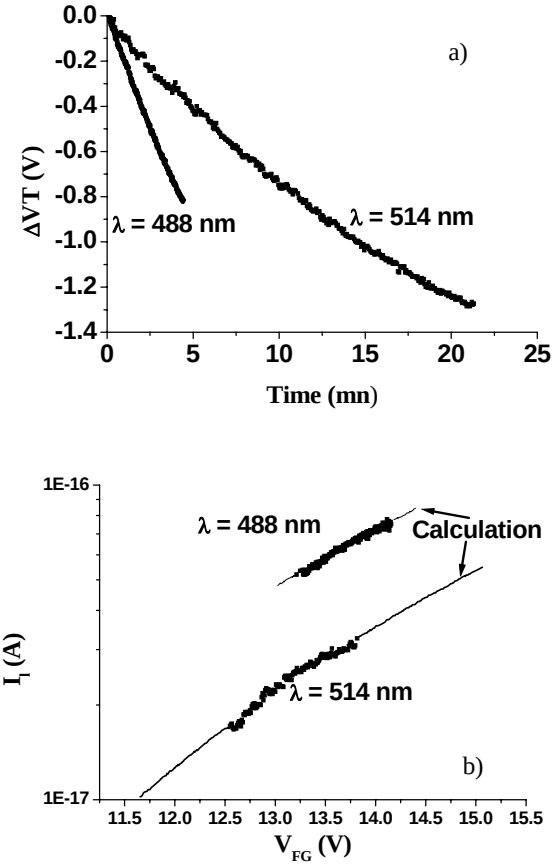

Figure 9: Threshold voltage variation during illumination (a) and leakage current (b) in an intrinsic cell. Calculation is the result of equation (5).

3.3.4 Conduction in extrinsic cells during illumination

Cells in the tail shown in Fig. 4 have been erased then reprogrammed and illuminated (λ = 514 nm). All cells had the same behaviour and we only give the example of cell "A" in Fig. 4.

The procedure as in § 3.2 has been applied and the leakage current obtained is represented in Fig.10 in a FN plot. Although the electric field range is not very large the curve is quasi-linear and the slope gives an effective barrier height of 0.4 eV. After correction for the temperature during illumination and photon energy (λ = 514 nm) the room temperature barrier height is equal to 2.81 eV in good agreement with the value found from burn-in experiment (2.77 eV).

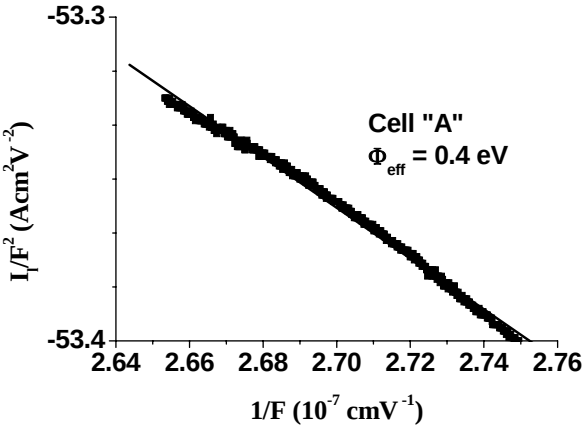

Figure 10 : FN plot of the leakage current in an extrinsic cell versus the reciprocal of the electric field F in the tunnel oxide.

So it is found that aging under illumination keep the same charge loss mechanism as a bake in intrinsic and in extrinsic cells at least when FN conduction only is involved which is the case in this work at low temperature. Extrinsic cells are characterized by a degradation of the tunnel barrier as expected and discussed in the introduction. This allows us to conclude that aging under illumination can be a fast method at room temperature to discriminate between intrinsic and extrinsic cells as illustrated in the following.

A population of cells has been erased, programmed and illuminated (λ = 514 nm, 30 mW/cm^2) during 3 mn. The distribution of the threshold voltage shift during illumination is shown in Fig. 11. Two parts can be easily discriminated: one corresponding to a normal distribution and a tail indicating a leakage current in excess typical of defective cells.

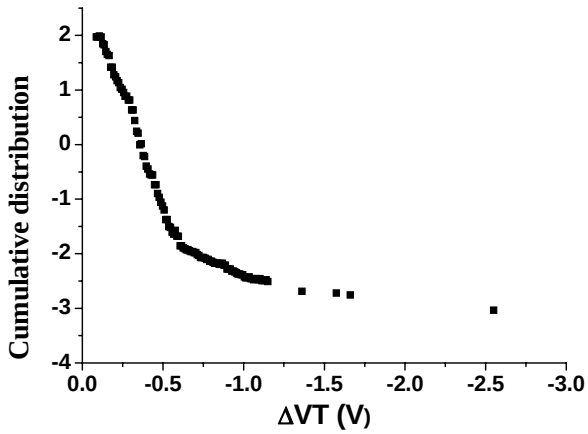

Figure 11 : Cumulative distribution of the threshold voltage shift after a 3 mn illumination.

4 Summary and conclusion

In this work we have studied charge loss under illumination in single-poly OTP-NVM embedded in a smart power circuit. It has been shown that the leakage mechanism was photo-field emission with a non degraded barrier in the case of the intrinsic cells and a degraded one for extrinsic cells.
All the results were in good agreement with those obtained from bake experiment at high temperature.
Analysis of the cumulative distribution of cells after illumination shows that aging under illumination is able to detect extrinsic cells in a population and can be used as a screening test.
The advantage of the test is that it is performed at a near-ambient temperature and with a very high acceleration factor since the illumination time lies in the minute range compared to hundred hours for burn-in experiment.
The main limitation is related with the absence of metal above the floating gate. So the method is limited to memories with a moderate density.

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