A 60-GHz Low Noise Amplifier in 0.13-μm CMOS

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Abstract: - The low noise amplifier (LNA) serves as the first component of the radio frequency receiver system. The performance of LNA determines the sensitivity and selectivity of the receiver. In order to maximize performance the gain, noise figure and input matching of LNA needs to be optmized. This paper presents a 60GHz low noise amplifier on 0.13-μm standard CMOS technology designed using classical noise matching techniques. The simulation results show a power gain of 18dB and a noise figure of 5.5dB at 60GHz.

Key-Words: - Low noise amplifier, Classical noise matching, Gain, Noise figure

1 Introduction

Recently 7GHz of frequency around 60GHz has become available in the US (57-64GHz), Europe (59GHz-63GHz and 65GHz-66GHz) and Japan (59GHz-66GHz) for unlicensed operation. The release of this frequency band allows for high data rate (up to 10Gb/s) low cost wireless data communication systems. Moreover, as the size of the antenna is inversely proportional to the propagation frequency of the signal, operation in the millimetre wavelength permits the integration of multiple antennas on one single chip. This makes it possible to have the entire transceiver system built on a single chip and significantly decrease the size and cost of the system.

To date 60GHz wireless communication solutions are predominantly built using GaAs and to a lesser extent SiGe technologies. CMOS provides a low cost alternative solution. Compared to GaAs and SiGe CMOS technologies have the advantages of lower cost and permit integration with low power digital components.

One of the first component in the receiver system is the Low Noise Amplifier (LNA). It needs to achieve a low noise figure and a sufficiently high power gain to ensure an appropriate receiver noise figure, good matching with the antenna and the mixer to maximize receiver sensitivity.

In this paper, a 60 GHz low noise amplifier using classical noise matching technique is presented. The proposed design exhibits a power gain of 18dB and a noise figure of 5.5dB at 60GHz using 130nm CMOS.

This paper is organized as follow: Section 2 reviews the design method for low noise amplifier. Section 3 and section 4 examines the transistor geometry and the transmission line used in this design. Section 5 presents the design and analysis of a 60GHz LNA using classical noise matching technique. Section 6 summarises the simulation results and conclusions are presented in Section 7.

2 Design Methods of Low Noise Amplifier

Three design methods for low noise amplifier are commonly used: the classical noise matching (CNM), the simultaneous noise and input matching (SNIM) and the common gate LNA.

As reported in [1] and [2], for a given amplifier the minimum noise figure can be achieved by bringing the source impedance to the optimum noise impedance by building a matching network between the signal source and the input port of the amplification 2-port. It is

possible to achieve the minimum noise figure of the amplification 2-port by properly selecting the impedance presented to the 2-port. The problem with the CNM technique is that typically the conjugate input matching and the optimal noise matching do not occur with the same source impedance [3]，[4]. Therefore, there is a trade-off between the maximum available gain and the noise figure of the LNA.

As described in [4] [5] [6] and [12], the source degenerative inductor shifts the optimum noise impedance to the desired value. Therefore, simultaneous noise and input matching is possible with the application of inductive source degeneration to the common source or the cascode topology. In addition, this inductor increases the real part of the input impedance of the amplifier and can be used to match the input.

In contrast to the narrow band matching given by the cascode amplifier with source degeneration, the common gate low noise amplifier provides a relatively wideband input match [8] [9]. Compared to the cascode topology, the common gate structure also requires a lower biasing voltage and hence consumes less power.

In this paper we utilize the traditional classical matching technique to design the LNA because it allows to obtain optimal power gain and noise figure over the frequency band of interest.

3 TRANSISTOR GEOMETRY

The maximum oscillation frequency $f_{\max}$ of transistor gives a good indication of power gain of transistor. Another crucial figure of merit of a transistor for LNA design is the minimum noise figure $NF_{\min}$, which represents the minimum achievable noise figure for the transistor. Both of these two figures of merit are strongly dependant on the size of transistor, the number of transistor fingers and the biasing current.

In order to determine the appropriate transistor geometry and biasing current, the maximum oscillation frequency $f_{\max}$ and the minimum noise figure $NF_{\min}$ are investigated for different transistor sizes, numbers of fingers and biasing currents. Figure 1, 2, 3 and 4 show $f_{\max}$ and $NF_{\min}$ for transistors of total width equal to $45\mu m$, $60\mu m$, $75\mu m$ and $90\mu m$, respectively. As a result of trading off maximum oscillation frequency and the minimum noise figure, a transistor of total width $75\mu m$ and width per finger $3.75\mu m$ is selected for the LNA design. The biasing current is selected to be $200\mu A/\mu m$. This is because it achieves the best transistor gain and minimum noise power.

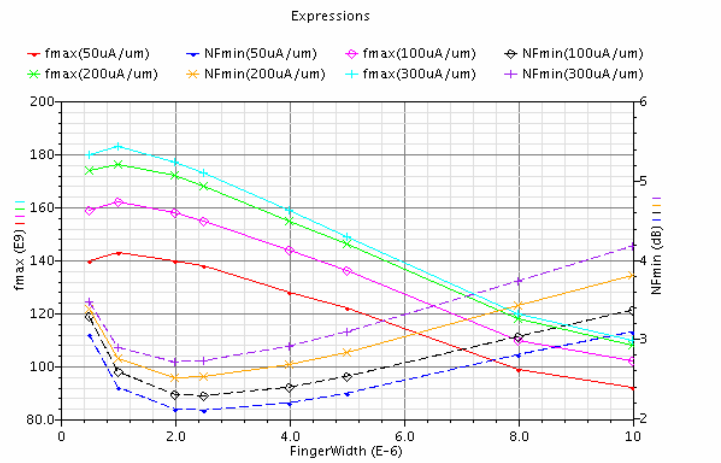

Figure 1 $f_{\max}$ and $NF_{\min}$ for total transistor width of $45\mu m$

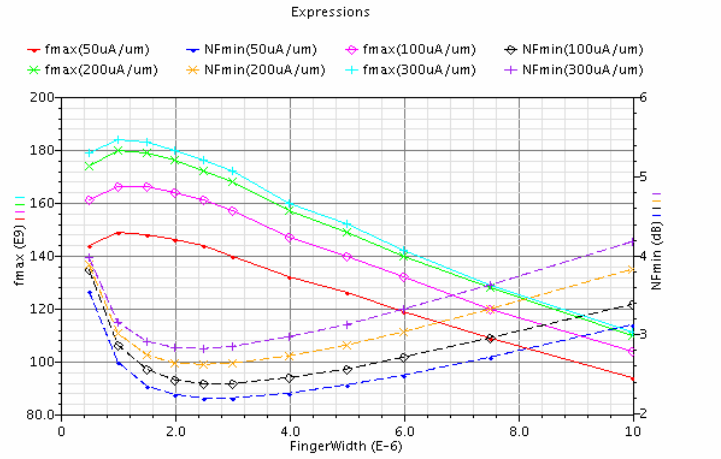

Figure 2 $f_{\max}$ and $NF_{\min}$ for total transistor width of $60\mu m$

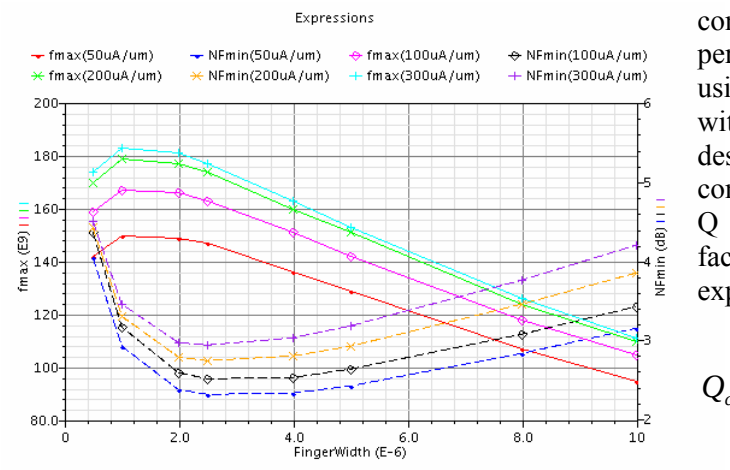

Figure 3 $f_{\max}$ and $NF_{\min}$ for total transistor width of $75\mu m$

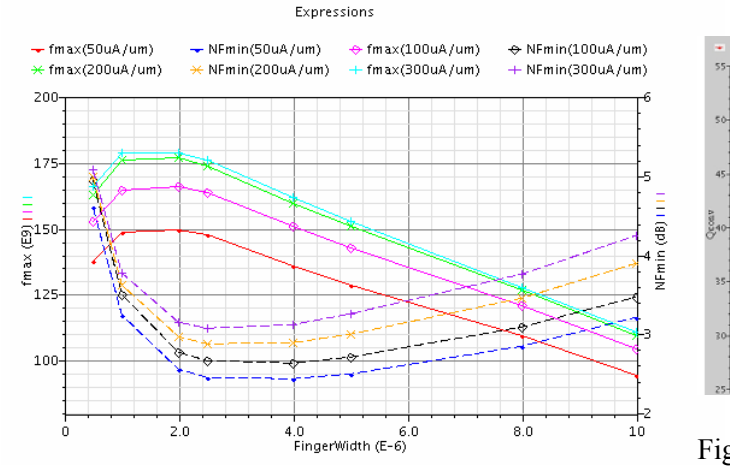

Figure 4 $f_{\max}$ and $NF_{\min}$ for total transistor width of $90\mu m$

4 TRANSMISSION LINE

At 60GHz, the inductance elements in the matching networks become very small (tens of pH). In this case, the inductive transmission lines, which are scalable in size are preferred in the matching networks.

For the LNA design, the inductive elements with high Q value are the key to low noise figure and high power gain [10] [11]. This is because the loss leads to drop in gain and rise in noise figure. Performance is limited by the Q values of the inductive elements.

In this design, microstrip transmission lines are selected as the inductive elements in the matching network considering their relatively higher effective inductance per unit length and their relatively high Q values. By using microstrip transmission lines, inductive elements with high Q value can be kept compact and make the design layout easier leading to a smaller overall size. A conventional Q factor is used to estimate the inductive Q factor of the microstrip transmission lines. This Q factor and the inductance of the transmission line can be expressed as:

$$Q_{conv} = \frac{\mathrm{Im}[Y_{11}]}{\mathrm{Re}[Y_{11}]}$$

$$ind = \frac{\mathrm{Im}[Y_{21}]}{\omega\left(\mathrm{Re}[Y_{21}]^2 + \mathrm{Im}[Y_{21}]^2\right)}$$

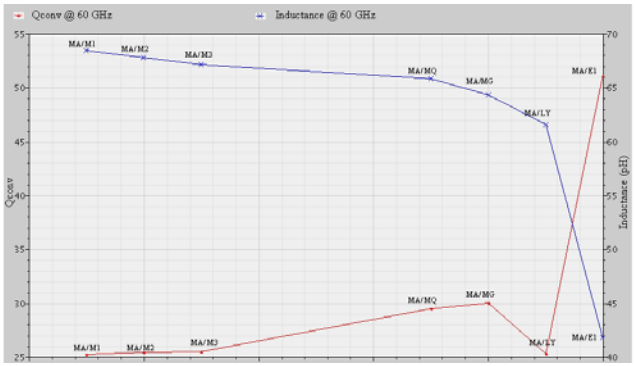

Figure 5 Inductance and conventional Q value for a 140um microstrip line

The CMOS technology used in this design utilizes eight metal layers indicated as M1, M2, M3, MQ, MG, LY, E1 and MA, with MA as the top layer. It is determined by simulation that the Q value and the inductance per length of the microstrip line are affected by layout arrangements such as the selection of top layer material and bottom layer material. Figure 5 shows the simulation results for a 140um microstrip line with MA as the top layer and several different layers as the bottom layer. The conventional Q values and inductances for different bottom layer options are simulated and plotted. MA/MQ configuration for the top/bottom layer is adopted in this design because it achieves a high Q value and a relative high inductance at the same time.

5 CIRCUIT DESIGN

The 60GHz low noise amplifier is designed using classical noise matching techniques [1] [10] [11]. The amplifier consists of three cascode amplification stages, input matching network and output matching network. Inter-stage matching networks are built in order to match the output of previous stage to the input of subsequent one. The schematic of the LNA is shown in Figure 6.

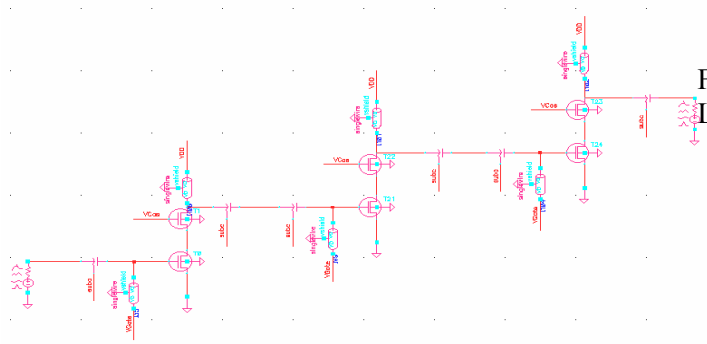

Figure 6 Simplified schematic of 60GHz low noise amplifier

Cascode transistors are used in this design to decrease the Miller capacitance and to achieve higher isolation compared to the common source transistor [11] [12]. The cascode transistor pair are biased at $200\mu A/\mu m$ and achieve a maximum power gain of 7dB and minimum noise figure of 4dB at 60GHz.

6 SIMULATION RESULTS

The performance of the LNA is simulated and its performance is shown in Figure 7, Figure 8 and Figure 9. As shown in these figures, S11 and S22 both reach a low at around 61GHz, while a maximum gain about 18dB is achieved. The 3dB bandwidth covers the entire 57-64GHz range. The noise figure is also lowest at around 61GHz with a minimum of around 5.5dB. The difference between the minimum noise figure of the cascode stage and the actual realized noise figure is due to the finite Q values of the microstrip transmission lines which induce loss into the circuit.

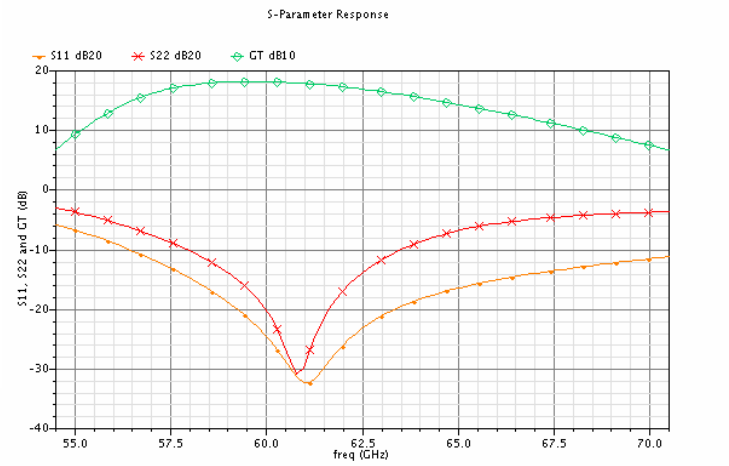

Figure 7 S11, S22 and transducer gain GT of the 3-stage LNA

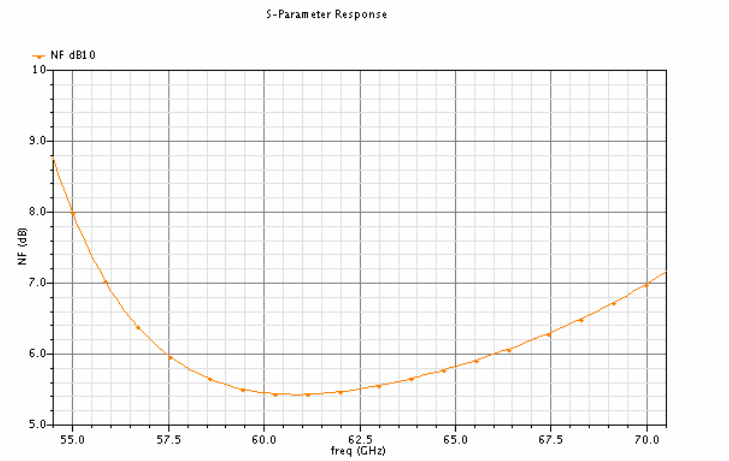

Figure 8 Noise figure of the 3-stage LNA

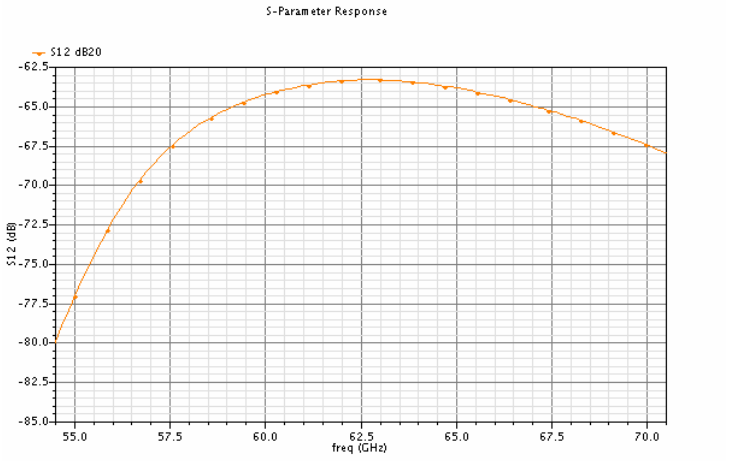

Figure 9 S12 of the 3-stage LNA

The simulation results at 60GHz are listed in Table 1.

Gain	NF	S11	S22	S12
18dB	5.5dB	-32dB	-30dB	-64dB

Table 1 LNA simulation results at 60GHz

7 CONCLUSION

A 60GHz low noise amplifier is designed in $0.13\mu m$ standard CMOS technology using classical noise matching technique. The transistor geometry and inductance transmission lines are optimized. The simulation results show a power gain of 18dB and noise figure of 5.5dB at 60GHz.

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