A 60 GHz 130 nm CMOS VCO with Ultra Wide Tuning Range

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Abstract: - A 60 GHz cross-coupled differential voltage controlled oscillator is designed in 130 nm CMOS technology. The tuning range is from 57GHz to 66GHz, with an estimated phase noise of -93 dBc/Hz at 1 MHz offset. The oscillator employs fundamental 30 GHz VCO followed by doublers and buffers.

Key-Words: - CMOS, 60GHz, VCO, wide tuning range, phase noise

1 Introduction

In recent years, 7 GHz of contiguous bandwidth has been allocated for unlicensed use at frequencies around 60 GHz in U.S.(57-64GHz), Japan (59-66GHz). In order to develop a product for the global market an ultra wide band VCO (57-66GHz) is required.

In order to facilitate cost effective solutions researchers have been investigating the applicability of designs based on CMOS type technologies [1]. The particular application pursued by the authors requires oscillators with low phase noise. In many cases the phase noise of LC-tank oscillators is limited by the ability to build high-Q factor inductors [2]. In this project, IBM 130nm CMOS technology is employed. This cmrf8sf_DM technology has 3 thin, 2 thick, 3 RF metal layers. The three thick RF-top metals are suitable for high-Q inductors.

In this paper, a voltage controlled oscillator with 9GHz tuning range is presented. The fundamental oscillator utilizes a differential cross-coupled topology which operates around 30GHz. It then followed by a frequency doubler and an output buffer. The output amplitude is between 300mV to 400mV across the frequency band of interest. The phase noise is -93 dBc/Hz at 1MHz offset.

This paper is organized as follows: section 2 describes VCO core structure; section 3 presents the overall structure; section 4 shows varactor topology and phase noise considerations; section 5 presents post-layout simulation results; section 6 concludes the paper.

2 VCO core structure

An oscillator is characterized by its oscillation frequency, amplitude, stability, phase noise and tuning range. In our case, to meet the specification of the transceiver, the tuning range of 9 GHz is required along with phase noise less than -90 dBc/Hz. The output amplitude needs to be more than 300mV to provide sufficient voltage to maximize the conversion gain of the mixer.

The performance of the oscillator is mostly determined by the quality factor (Q value) of the LC resonator. At low frequencies, the inductor can be made off-chip to reduce phase noise. In this process a high Q transmission line is used on-chip along with two MOS varactors to form a LC tank. The circuit of the differential cross-coupled LC oscillator [3] is shown in figure 1. Each arm has a LC tank circuit that determines the frequency of oscillation. Frequency dependent signals at the drain are then cross-coupled to the other transistor's gate which creates a negative impedance -1/gm. This negative impedance has to exceed the losses of the resonator to ensure sustained oscillation.

An important consideration in oscillator design is to determine the transistor size in order to achieve optimum performance. Transistors M1, M2 are 130 nm nfet transistors with 20 um width. L1 and L2 are 100um long, 25 um wide transmission lines with equivalent inductance value of 50 pH. C1 and C2 are MOS varactors. In this design the supply voltage Vdd is set to 1.5 V and the varactor tuning voltage Vtune varies from 0 to 1.5 V.

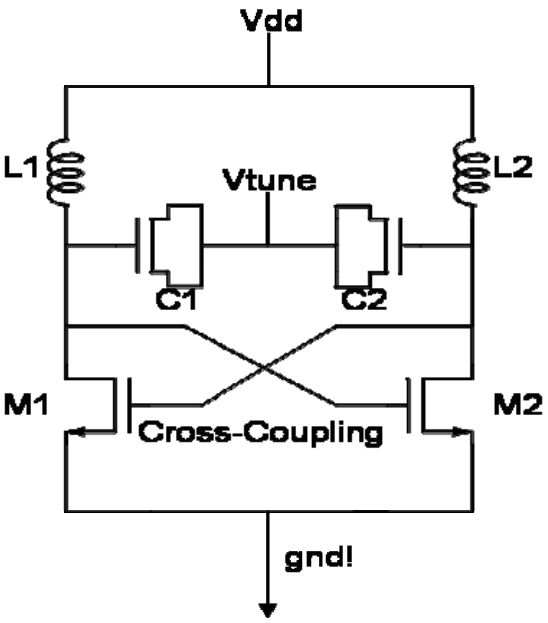

Fig.1 VCO core structure

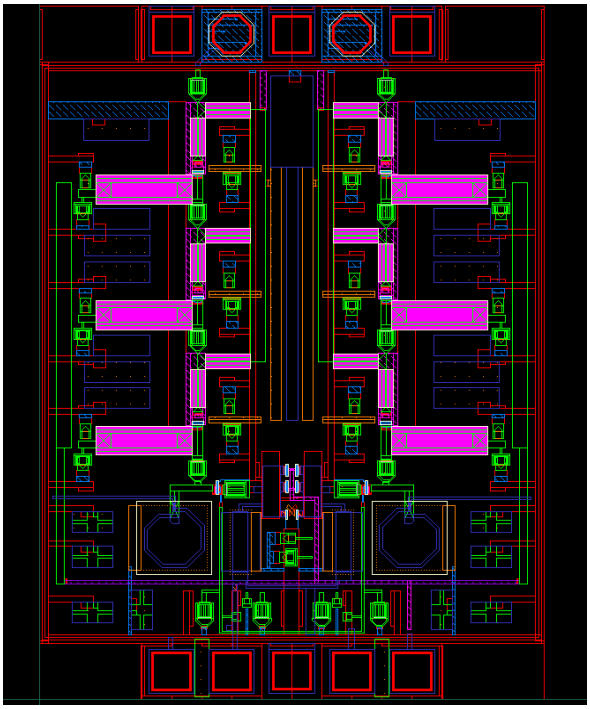

Fig.2 VCO overall layout

3 Overall structure

Figure 2 shows the entire layout structure of VCO. A VCO operating at 30 GHz followed by a frequency doubler is employed in this design. The differential outputs then connect to the mixer.

4 Varactor structure

The minimum and the maximum value of the varactor's capacitance determine the oscillation frequency range. Although we can determine the input capacitance for certain operating point, we can not use this value to determine the exact value of oscillation frequency. The capacitance seen by the tank deviates as a function of the large signal swing during the oscillation [4]. Therefore the effective average capacitance of the varactor determines the frequency of oscillation. This non linear capacitance causes higher order harmonics that increase phase noise.

Figure 3 shows an nfet with drain and source connected together. Apply different voltages at this node results in a different effective capacitance values. A very wide tuning range of 15% is achieved with a control voltage tuned from 0 to 1.5V. The default length of NMOS transistor is 130 nm. Increasing this length to 260 nm provides a higher Cmax to Cmin ratio.

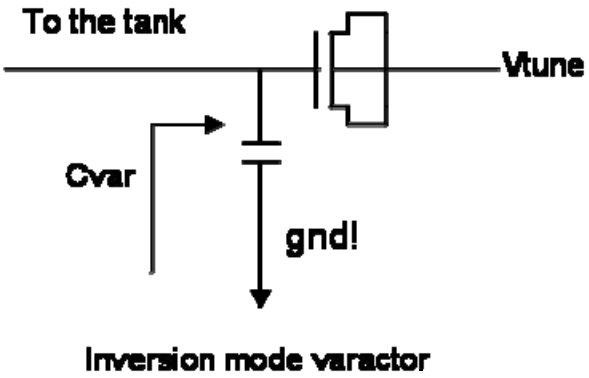

Fig.3 NMOS transistor with source and drain connected together to act as an inversion mode capacitance.

There is a trade off between tuning range and phase noise. In our case, tuning ranging is the primary issue along with minimum phase noise requirement -90 dBc/Hz. Most of the traditional designs include current source to set the bias current and provide high impedance. Due to the oscillator transistor's mixing effect caused by nonlinearity, the low frequency noise of the current source is up converted to high frequency around the even harmonics and then down converted to the fundamental frequencies [5]. In our design, the current source is omitted to suppress this phase noise contribution.

5 Results

The simulations were performed with SpectreRF tools. Electromagnetic simulations were also needed to determine interconnect parasitics. The extraction tools were Cadence Assura RLCK which extracts not only resistors, capacitors, but also self and

mutual-inductance of interconnections. All simulation results in this section are based on post-layout including parasitics extractions.

Figure 4 shows the spectrum of a single run, the tuning range is from 57.2 GHz to 66.1 GHz.

Figure 5 and 6 show Monte Carol simulations of 50 runs with the inclusion of process variations. The monte-carlo simulations show the range of oscillation frequencies around the nominal frequency of 57GHz. The frequencies vary from 56 GHz to 58.4 GHz.

Figure 6 shows oscillator performance centered around 65.7 GHz. The frequencies vary from 64.2 GHz to 66.8 GHz.

Figure 7 shows the estimated phase noise is -93 dBc/Hz at 1MHz offset at 60 GHz centre frequency.

Table 1 summarize the key results of this design.

The design has been submitted to MOSIS for fabrication.

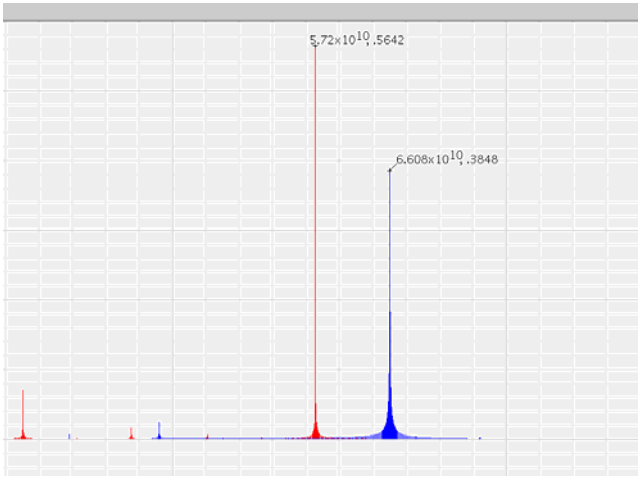

Fig.4 Spectrum simulation of a single run

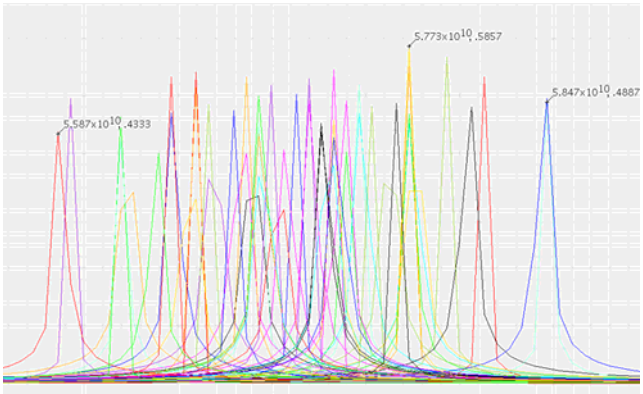

Fig.5 Monte Carlo simulation at 57 GHz

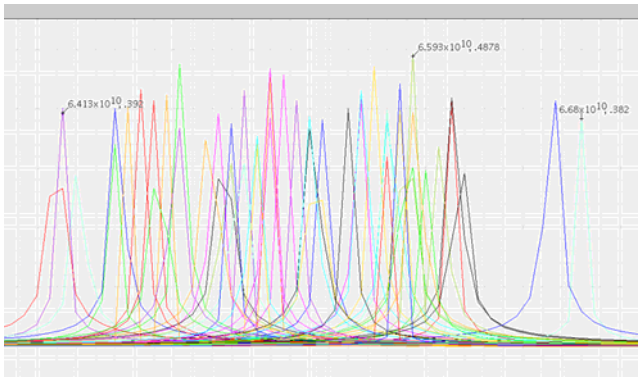

Fig.6 Monte Carlo simulation at 66 GHz

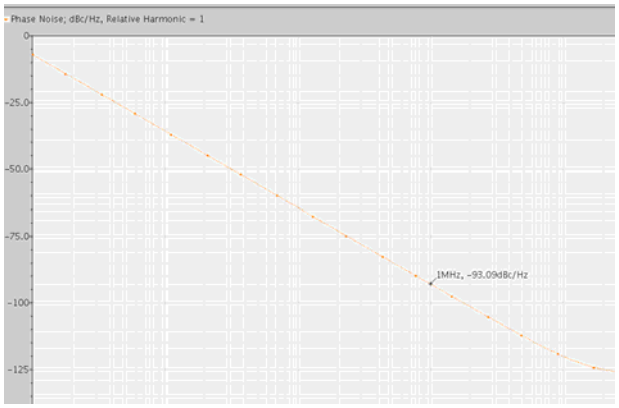

Fig.7 Estimated phase noise

fo [GHz]	Vdd [V]	L(1MHz) [dBc/Hz]	Tuning Range [GHz]	Technology
60	1.5	-93	9 (15%)	130nm CMOS

Table 1: VCO performance summary

6 Conclusion

An ultra wide band VCO is implemented in 130nm CMOS technology. The designed oscillator has a tuning range from 57 GHz to 66 GHz with a simulated phase noise of -93 dBc/Hz at 1MHz offset. It also provides 0 to 2 dBm output power.

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