A 60-GHz Broad-Band Frequency Divider in 0.13-µm CMOS

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Abstract: - A frequency divider based on injection-locked tunable ring oscillator is designed on 0.13-µm standard CMOS. The proposed design can achieve divide-by-4 in the frequency range of 58.75-66.3 GHz. The divider dissipates 49.5 to 54.5 mW power from a 1.5-V voltage supply.

Key-Words: - High-speed frequency dividers, Injection-locked tunable ring oscillator, Division range

1 Introduction

The frequencies from 54-66 GHz have currently been set aside for unlicensed operations in the US, Europe and Japan [5]. In order to build low cost transceivers, frequency dividers are required in phase-locked loops (PLL) that are used to stabilize the voltage-controlled oscillator's (VCO) output using a low cost external low phase noise, temperature coefficient and frequency drift crystal oscillator.

In the past DHBT [1], HEMT [2] and SiGe bipolar [3] technologies have been used for high-speed frequency dividers implementation. These technologies are more expensive compared to standard CMOS technologies. CMOS allows for low cost and high integration with low power digital circuits. The fastest frequency divider based on CMOS reported in the literature operates at 50 GHz [10]. This divider has been designed narrow band operation and is not applicable for operation in the 54-66 GHz band.

In this paper, a 60-GHz wide-band frequency divider is presented. The proposed divider implemented in IBM 130nm CMOS process uses an injection-locked tunable ring oscillator and exhibits a divide-by-4 function for input frequencies from 58.75-66.3 GHz.

In Section 2 of this paper a review of the design methods of frequency dividers is presented. In section 3 and 4 the details of the proposed circuit design and division range analysis are presented. Sections 5 and 6 summarize the simulation results and conclusions are presented.

2 Design Methods of High-speed Frequency Dividers

Conventional low frequency dividers are implemented digitally by connecting two D-flip flops with a feedback loop [7]. This design method can be extended to gigahertz frequency range with a differential current-switching structure, called current mode logic (CML) [7]. The CML frequency dividers have a high division bandwidth [8], but low operational frequency and large power consumption when compared to other divider structures.

Regenerative frequency dividers show the characteristics of high-speed operation frequency [4] and low power dissipation. This type of frequency divider circuit is based on a mixer structure which combines the output through a *LC* tank feedback loop to one of the input ports of the mixer. The *LC* tank functions as a band-pass filter to select the half frequency signal of the signal produced by the mixer. This band-pass property limits the frequency division range.

Injection-locked frequency dividers are widely utilized in the gigahertz frequency domain [9]. An input signal is injected to oscillator input which is oscillating at half the input signal's frequency. Because of nonlinearity, the input signal drives the oscillator which achieves the division. For the high-speed, low phase noise and low power, the *Q* factor of the *LC* oscillator needs to be high which limits the division range.

3 Circuit Design

Regenerative and Injection locked dividers generally have the problem of narrow division range at high frequency. This is caused by the high *Q* of the *LC*

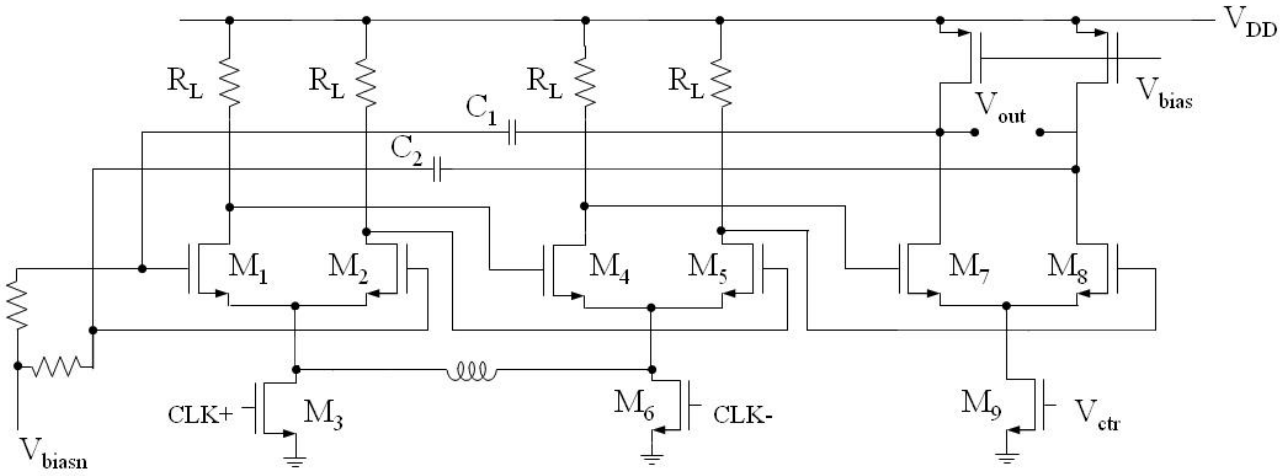

Fig. 1. Schematic of proposed injection-locked ring oscillator

tank component. To build a high frequency large division bandwidth divider with low phase noise, a tuneable ring oscillator topology can be utilized. The ring oscillator topology has wide frequency tuning range and small integrated size. This structure has attracted recent interest and in [6] a divide-by-4 injection-locked ring oscillator built on 0.18-μm standard CMOS technology operating in the 41.2-46.9 GHz is reported.

Fig. 1 shows the schematic of the proposed 60-GHz injection-locked tunable ring oscillator with a division ratio of 4. In order to achieve the high self-oscillation frequency, three delay stages are used (ring oscillator consisting of 2 stages has been reported in [11]). The extra stage is required to achieve sufficient gain at high frequency to ensure sustained self-oscillation.

In this design, the first and second delay stages are identical whilst the last stage uses PMOS loads. The free running frequency of entire ring oscillator is dominated by the last stage. In [7] the transfer function of the 3-stage ring oscillator is determined and shown to be equal to

$$H(j\omega) = -\frac{(G_m R)^3}{(1+j\frac{\omega}{\omega_o})^3}. \quad (1)$$

In this analysis all three stages are the same and G_m, R and ω_o are the transconductance, load and 3-dB bandwidth of each stage, respectively. Due to the Barkhausen conditions for an oscillator, each stage contributes $\pi/3$ phase shift when oscillating at steady state. Then the phase shift required per stage is equal to

$$\tan^{-1}\left(\frac{\omega_{osc}}{\omega_o}\right) = \frac{\pi}{3}, \quad (2)$$

where ω_{osc} is the oscillating frequency. In our design, the first and second delay stages differ from the third stage. Therefore, the phase condition equation of the proposed ring oscillator is given by

$$\sum_{i=1}^{2} \tan^{-1}\frac{\omega_{osc}}{\omega_i} + \tan^{-1}\frac{\omega_{osc}}{\omega_3} = \pi, \quad i = 1,2 \quad (3)$$

where ω_i and ω_3 represent the 3-dB bandwidth of the first second and third stage respectively. The solution of (3) is simulated for different $\omega_{1,2}$ and ω_3 and is shown in Fig. 2. The solution region around 15 GHz (60 GHz divided by 4) is the region of interest. Furthermore the overall ω_{osc} is sensitive to ω_3 and varies significantly as it is varied which implies a large tuneable frequency range. Utilizing equation (3) in conjunction with the gain condition for the ring oscillator the optimal values are established as follows: $\omega_{1,2}$ equal to 19 GHz, and ω_3 varying between 3-5 GHz.

Fig. 1 shows the change of the free running frequency of ring oscillator by adjusting the load of the last stage. This is achieved by controlling the tail current of M_9 so that transconductance value of the PMOS loads is appropriately adjusted. V_{ctr} is the control for the tail current source and V_{bias} are adjusted to ensure that the PMOS loads remain in the triode region. CLK+ and CLK- represent input signals with 180° phase difference, which are injected into the tail current sources of the first and second stages. To reduce the loss of the input signal power during the injection procedure, a shunt inductance is introduced across the transistors M_3 and M_6. The shunt inductor is chosen such that it resonates with the parasitic capacitances of M_3 and M_6 at approximately the desired input frequency. The introduction of this inductor helps improve injection efficiency as well as increasing the divider locking range.

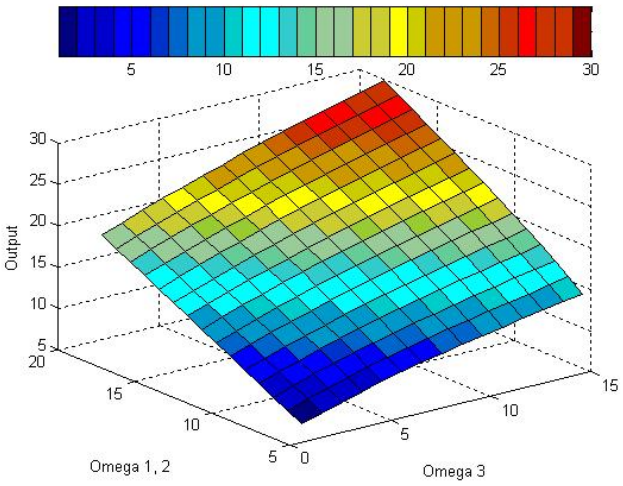

Fig.2. Simulation results of phase condition equation

4 Division Range Analysis

Many researches have investigated the locking range of injection-locked phenomena: [9], [12], [13] [14]. In [9] and [13], it is assumed that the *LC* tanks provide additional phase shift and this is used to derive the division frequency range. The analysis in [14] gives an analytical expression for division range of an injection-locked ring oscillator frequency divider. In this paper, a new expression for division range is introduced combining the work in [13] and [14]. A simple model from [14] to investigate injection-locked mechanism of ring oscillators is illustrated in Fig. 3. In this model, the differential pair of the delay stage is considered as a mixer and the cascading of these stages has a low-pass filter characteristic. The input signal is injected at the *RF* port of the mixer and *LO* port receives the signal from the oscillator's loop which is simplified as a square wave. Due to the nonlinearity of the mixer, only odd harmonics are present at the *LO* port. These signals are multiplied with the injected frequency. Denoting the injected frequency as ω_{inj} and ω_{osc} as the free running oscillator frequency, we have

$$\left|\omega_{inj} - (2k-1)\omega_{osc}\right| = \omega_{osc}. \quad k = 1,2,\ldots \tag{4}$$

The high frequency components produced by mixer are filtered out because of the low-pass property of the ring oscillator. Equation (4) implies that the division ratio for injection-locked dividers can only be an even number.

In order to determine the division range, we use the vector addition [13] shown in Fig. 4. I_{osc} represents the free running frequency of the oscillator and βI_{inj} is the signal produced by the mixer (β denotes the mixer conversion factor). In [13] the relationship

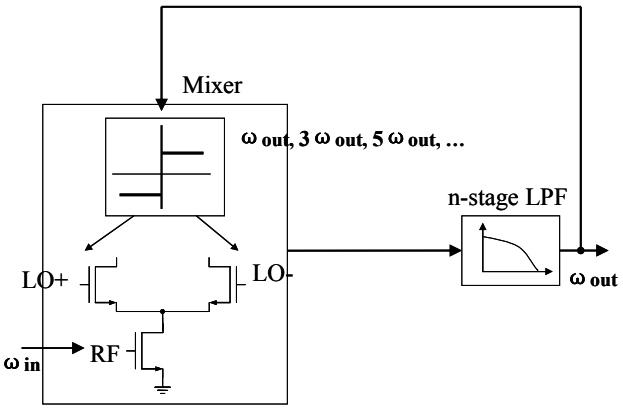

Fig.3. Mode of injection-locked ring oscillator

$$\sin\phi_o \approx \frac{\beta I_{inj}}{I_{osc}}\sin\theta, \tag{5}$$

is derived. The angle ϕ_o is the deviation from 360° which corresponds to the required oscillation phase condition. This deviation in angle must be eliminated. The low-pass filter is formed by 3-stage cascading delay stages and also provides the requisite phase compensation. In reference [14] the linearized phase response expression of the filter in the vicinity of oscillating frequency is derived and is shown to be equal to:

$$\alpha = 3\tan\left(\frac{\omega}{\omega_o}\tan\left(\frac{\pi}{3}\right)\right) \cong \frac{3\sin(2\pi/3)}{2}$$
$$= \frac{3\sqrt{3}}{4}\cdot\frac{\Delta\omega}{\omega_o}, \tag{6}$$

where α denotes the phase response and $\Delta\omega = \omega - \omega_o$ indicates the offset frequency. Fig. 4 implies when is small equations (5) and (6) can be combined as

$$\sin\theta \approx \frac{3\sqrt{3}}{4\omega_o}\cdot\frac{I_{osc}}{\beta I_{inj}}\Delta\omega. \tag{7}$$

According to [13], the locking range is obtained from (7) as

$$\Delta\omega \approx \frac{4\omega_o}{3\sqrt{3}}\cdot\frac{\beta I_{inj}}{I_{osc}}. \tag{8}$$

where $\beta = 2/3\pi$ (5-th harmonic is ignored because its factor is a small number). With differential injection inputs, this range must be doubled [13]. The final analytical expression of division range based on injection-locked ring oscillator can then be written as:

$$\Delta\omega \approx \frac{4\omega_o}{3\sqrt{3}}\cdot\frac{4}{3\pi}\cdot\frac{I_{inj}}{I_{osc}}. \tag{9}$$

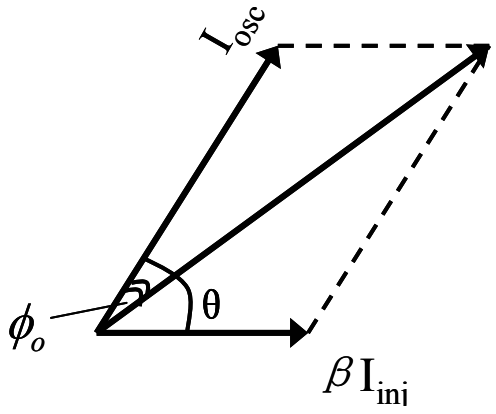

Fig.4. Vector addition diagram of injection-locked mechanism

Furthermore, according to [9], [12] and [13], the locking range of a *LC* injection-locked oscillator is proportional to 1/2*Q*. Since the *Q* of a *LC* tank is generally greater than 10, it can be established that the division range of injection-locked ring divider is larger than *LC* tank injection-locked divider.

5 Simulation Results

The circuit of the proposed frequency divider was implemented in IBM 130nm CMOS process and simulated in SpectreRF of Cadence [15]. With a 1.5 V supply voltage and the DC power consumption from 49.5-54.5 mW, the self-oscillation frequency and output power characteristics of proposed ring oscillator are shown in Fig. 5. It indicates that as I_{ctr} is varied, the self-oscillation frequency varies from 14.9 GHz to 17.1 GHz with an output power range from -30.5 to -24.8 dBm. After the input signal being injected to first and second delay stages the divide-by-4 division range is shown from 58.75 to 66.3 GHz. The performance of proposed injection-locked tunable ring oscillator frequency divider is exhibited in Table 1.

6 Conclusion

A 60-GHz injection-locked tunable ring oscillator frequency divider is designed and simulated in 0.13-µm standard CMOS technology. A new expression for division range of injection-locked dividers is derived in this paper and it shows that the ring oscillator frequency dividers have larger division range when compared the *LC* oscillator frequency dividers.

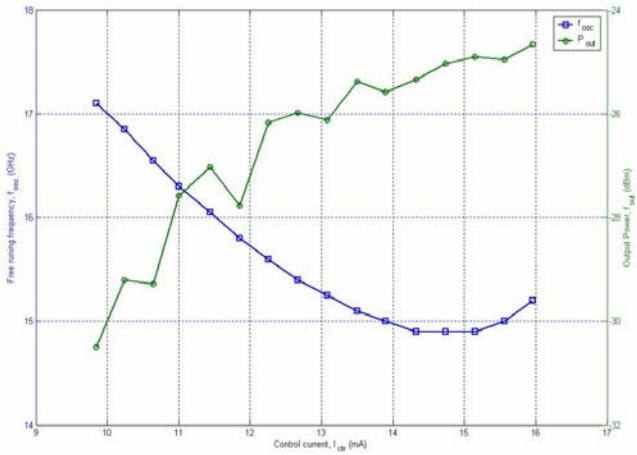

Fig.5. Tuning frequency and output power characteristics of the ring oscillator

Technology	0.13-µm standard CMOS
DC supply voltage	1.5 V
Self-oscillation frequency	14.9 - 17.1 GHz
Divide-by-4 division range	58.75 - 66.3 GHz
Power consumption	49.5 - 54.5 mW
Phase noise @ 1 MHz offset when dividing	-102 dBc/Hz

Table 1. Performance conclusion

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