Hardware Implementation of Configurable Bandwidth Estimation Module in High Speed Networks

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Abstract: - The purpose of self-sizing networks is to provide efficient utilization of network resources while ensuring appropriate Quality of Service (QoS) for each class of traffic. Bandwidth estimation, which estimates the amount of a traffic bandwidth, is useful to allocate proper bandwidth in order to meet a QoS requirement. This paper concerns an hardware implementation of a Configurable Bandwidth Estimation Module(CBEM) on a reconfigurable field-programmable gate array(FPGA) board. CBEM can be configured in one of the two forecasting based rate estimation mechanisms; Moving Average (MA) mechanism and Exponential Smoothing (ES) mechanism. We performed simulation and test to evaluate CBEM in various network conditions. The results show CBEM is practically feasible to be implemented in self-sizing high speed networks.

Key-Words: - Bandwidth Estimation, QoS, Traffic Monitoring, Traffic Measurement.

1 Introduction

In recent years, there has been a tremendous growth in the Internet. New applications present new traffic patterns. The need for dynamic configuration of network devices to adjust to the evolving traffic has grown fast. Understanding the composition and dynamics of the Internet traffic is of great importance for network management. Since arriving traffic is not known a priori, a measurement-based resource allocation scheme must be utilized. This allows the network to follow the transient nature of the traffic in a realtime manner, adapting to its changing characteristics [1].

The concept of bandwidth estimation can be utilized to estimate the amount of bandwidth that should be allocated to a source in order to meet a QoS requirement. Effective bandwidth is generally defined in [2]. The s parameter in [2] cannot be directly estimated from measurement. It must be calculated using the Large Deviations Theory and making a large buffer assumption. Therefore, the direct application of [2] in an online measurement resource allocation scheme is not practical. Numerous ways of evaluating this solution have been defined in literature; however, most of the approaches rely on unrealistic assumptions or invalid approximations. A comparison of several different empirical estimators is described in [3]. The Gaussian [4], Courcoubetis [5], and Norros [6] allocation algorithms are more practical algorithms. However, they still have complexity of implementation.

Our approach is more practically implementable. We adapt forecasting method to estimate traffic bandwidth, not effective bandwidth, in a realtime manner. We design a Configurable Bandwidth Estimation Module (CBEM) that can be configured in one of the two forecasting based rate estimation mechanisms; Moving Average (MA) mechanism and Exponential Smoothing (ES) mechanism. We perform simulation to evaluate CBEM in various network conditions.

This paper is organized as follows: In Section 2, we provide brief feature of the two forecasting methods, MA technique and ES technique, and we describe our CBEM architecture in detail using Differentiated Services (DiffServ) traffic conditioner. Section 3 includes a implementation of CBEM on a FPGA board. In Section 4, we provide a description of our test results. We summarize our findings and discuss future work in Section 5.

2 Configurable Bandwidth Estimation Module

2.1 Forecasting Method

Forecasting can provide effective information to forecast uncertain future using accumulated data. In this paper, we focus on time series analysis method though there are various forecasting methods. Simple MA technique and ES technique are in this category [7].

Simple MA technique is the best-known fore-casting methods. It simply takes a certain number of past periods and adds them together; then divides by the number of periods. Simple MA is effective and efficient approach provided the time series in stationary in both mean and variance. Eq. (1) is used in finding the moving average of order *N*, *MA (n)* for a period *t+1*,

$$MA_{t+1} = (D_t + D_{t-1} + D_{t-2} + ... + D_{t-N+1}) / N \quad (1)$$

where *N* is the number of observations used in the calculation and *Dt* is observed data at *t*. The key point of this method is decision of *N*; large number of *N* results in horizontal strait line, while small number of *N* brings on forecasting results too sensitive to resent data.

One of the most successful forecasting methods is the ES technique. While the simple MA method is a special case of the ES, the ES is more parsimonious in its data usage. Moreover, it can be modified efficiently to use effectively for time series. It is also easy to adjust for past error-easy to prepare follow-on forecasts, ideal for situations where many forecasts must be prepared, several different forms are used depending on presence of trend or cyclical variations. In short, an Es is an averaging technique that uses unequal weights; however, the weights applied to past observations decline in an exponential manner.

$$F_{t+1} = \alpha D_t + (1-\alpha) F_t \quad (2)$$

where: *Dt* is observed data at *t*. *Ft* is the forecasted value, α is the weighted factor, which ranges from 0 to 1. Small α provides a detectable, and visible smoothing. While a large α provides a fast response to the recent changes in the time series and a small amount of smoothing.

2.2 Architecture

DiffServ traffic con-ditioner consists of 3 main components: meter, maker, and shaper/policer. Packet classifier classifies traffic flows into several classes. Then each class has traffic flows with similar characteristics. Meter serves to collect statistics on network flows. Traffic flows are marked and shaped/dropped by marker and shaper/policer, if the traffic is non-confirming its traffic profile.

CBEM can be used in DiffServ traffic conditioner as a meter. Fig. 1 shows logical diagram of traffic conditioner of DiffServ architecture using CBEM.

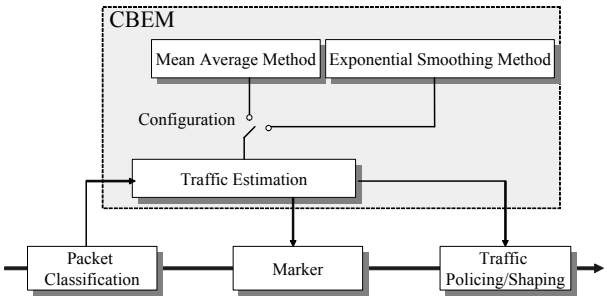

Fig. 1. Logical diagram of CBEM in DiffServ traffic conditioner

CBEM has two forecasting based rate estimation mechanisms; MA mechanism and ES mechanism. CBEM can be configured one of them depending on traffic characteristics and also each mechanism has parameters to be set. As Eq. (1) and Eq. (2) shows, MA mechanism is sensitive to the number of observations and ES mechanism is dependent on the weighted factor. MA mechanism is useful for estimating low bandwidth variation traffic and ES is useful for estimating high bandwidth variation traffic.

2.3 Simulation Results

In this Section, we perform simulation to evaluate CBEM in various network conditions. In our simulations, we compare actual traffic bandwidth with bandwidth estimation results using CBEM. All simulations were performed using the ns-2 [8]. In all the simulations, the link buffer size is set at zero, and link bandwidth is set at 10Mbps. The propagation delay along the link is 1 ms. Fig. 2 shows simulation network topology.

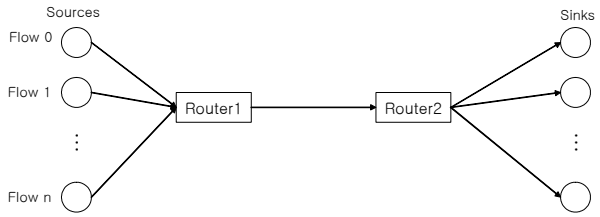

Fig. 2. Simulation network topology

We consider the link shared by four UDP flows. Each UDP flow sends packets at 64Kbps. Fig. 3 shows a plot of the actual input traffic of router 2, along with the estimated bandwidth for each mechanism of CBEM. As Fig. 3 shows, UDP flows send packets at 64Kbps mean data rate, while they have burst traffic characteristics such as 8Mbps peak rate. In case of applying MA mechanism (*N=20*) to CBEM, the estimated bandwidth has 400Kbps peak rate. This result shows MA mechanism can provide high bandwidth utilization, if buffer size is enough to handle burst packet size.

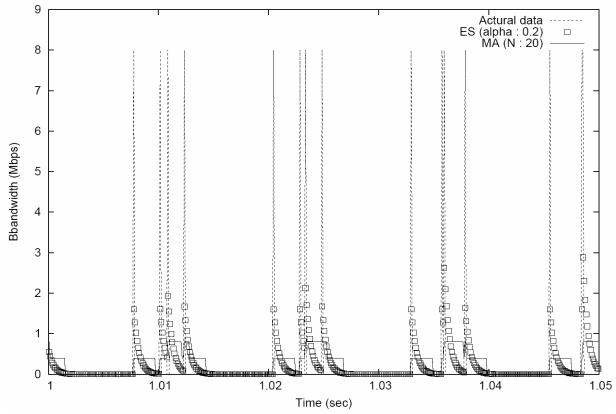

Fig. 3. Actual bandwidth vs. estimated bandwidth – 4 UDP flows

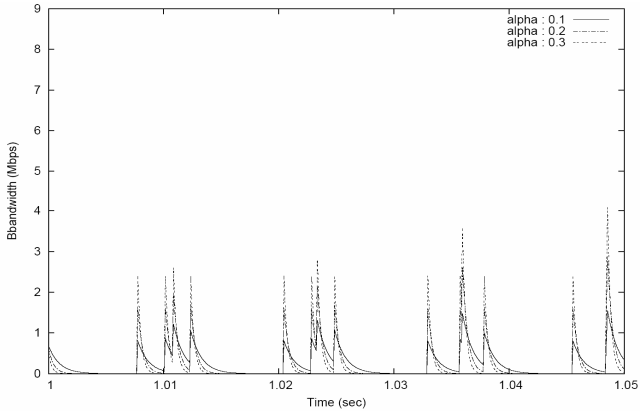

Fig. 4. Difference of bandwidth estimation results when ES has various weight factors – 4 UDP flows

ES mechanism (α=*0.2*) provides the smoothed estimated bandwidth result with 2.9Mbps peak rate. While the result shows still burst traffic characteristic, ES mechanism requires less buffer size then MA mechanism. Fig. 4 shows that the effect of α value variation in ES mechanism. As α value is increasing, the estimated bandwidth results show more burst traffic characteristics.

3. Hardware Implementation

By using the re-configurability of the FPGA, a reconfigurable computing system can reduce execution time by hardwiring the computationally intensive parts of the algorithm. The most important component of this system is that the FPGA consists of uncommitted programmable logic gates and programmable interconnections. These gates and interconnections are configured by the end user in such way as to perform the desired function. Most available reconfigurable computing systems act as co-processing devices of the host system and are directly plugged into the slot of the host system.

We designed the reconfigurable FPGA system used in this work. Fig.5 shows the external view of the FPGA board, where the IC big at the left top is the Intel GCIFX440AC Quad MAC and the IC at the right center is the Xillinx FPGA Virtex-II Pro XC2VP20 with 22032 gate count, and the big IC at the bottom is the PCI controller that controls the communication between the FPGA board and PCI-based computer via PCI-bus.

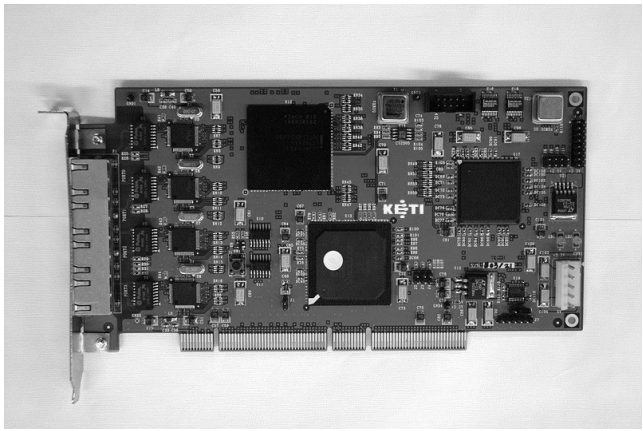

Fig. 5. An external view of the FPGA board

Fig. 6 shows a hardware block diagram of the implemented FPGA board. The FPGA board is composed of a FPGA and a Fast Ethernet MAC/PHY

interface part, and a PCI controller. The FPGA has the following features.

- 22032 logic cells
- Built on a 0.13-micron, 9-layer copper process technology
- 8 Mbits of embedded Block RAM and 1.4 Mbits of distributed RAM
- 622 Mbps to 10.3125 Gbps serial transceivers
- Up to 444 18X18 embedded multipliers

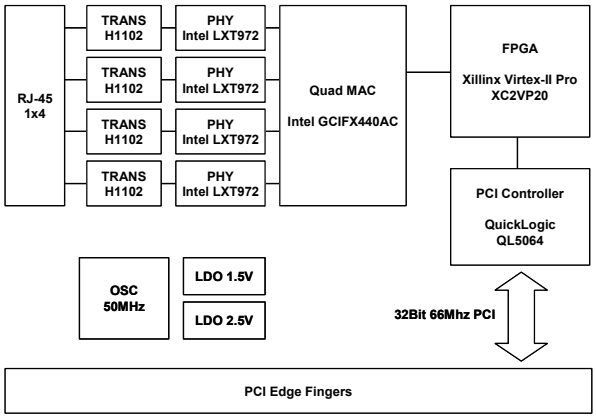

Fig. 6. FPGA board configuration

The VHDL code of the FPGA consists of several blocks such as Interrupt Generation Process, FIFO Read Process, Moving Average Process, and Exponential Smoothing Process. The Ethernet packets are captured by Quad MAC and pushed into the FIFO of the FPGA. The proposed bandwidth estimation algorithms in section 2 are coded such as Moving Average Process and Exponential Smoothing Process. The each processed results are transmitted to host computer through PCI bus.

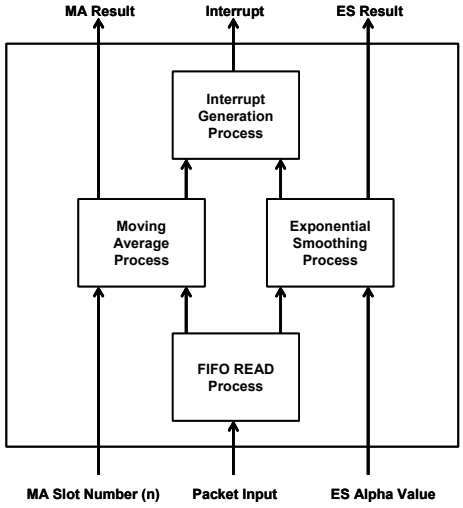

Fig. 7. A functional diagram of the VHDL code

4. Test Results

The validity of the developed CBEM is tested by monitoring FPGA board through PCI-bus. Fig. 8 shows the test environment that consists of FPGA Host, Transmit Host, Receive Host, and Network Tap for mirroring Ethernet packets.

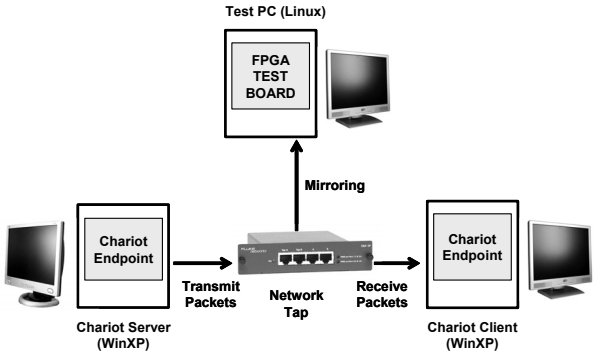

Fig. 8. Test environment

We measured and graphed the result data when N for Moving Average process is 20 and α value for Exponential Smoothing process is 0.1. The results are similar to the simulation at the same parameters.

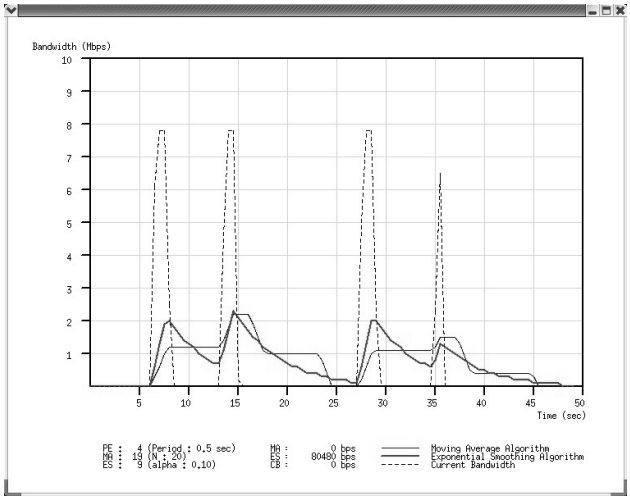

Fig. 9. Test result (MA:19, ES:9)

5. Conclusion

In this paper, we implemented our CBEM that can be configured in one of the two forecasting based rate estimation mechanisms; MA mechanism and ES mechanism. Existing policing mechanism uses long term average rate to limit traffic. This may waste bandwidth capacity during no traffic period and may not cover traffic burst characteristics.

We performed simulation to evaluate CBEM in various network conditions and implemented CBEM on a FPGA board. The simulation and test results show that CBEM is practically feasible to be implemented in high speed networks. If buffer size is large enough, MA mechanism is suitable. Otherwise, ES mechanism is better. If traffic flow has realtime traffic characteristics, ES is good. If traffic flow has non-realtime traffic characteristics, MA mechanism is proper.

We may have a lot of research issues to overcome, for example, how to decide the observation number in MA mechanism and the weighted factor value in ES mechanism for estimating properly various traffic patterns, and more reliable testing. The details of such issues are left to future work.

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