Memory-Efficient and High-Performance Parallel-Pipelined Architectures for 5/3 Forward and Inverse Discrete Wavelet Transform

TZE-YUN SUNG
Department of Microelectronics Engineering
Chung Hua University
707, Sec. 2, Wufu Road
Hsinchu, 30012, TAIWAN

Abstract: - In this paper, high-efficient lifting-based architectures for the 5/3 forward and inverse discrete wavelet transform (DWT) are proposed. The proposed parallel and pipelined architecture consists of a horizontal filter (HF) and a vertical filter (VF). The system delays of the proposed architectures are reduced. Filter coefficients of the biorthogonal 5/3 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architectures, all multiplications are performed using less shifts and additions. The proposed parallel-pipelined architectures are 100% hardware utilization and ultra low-power. The architectures have regular structure, simple control flow, high throughput and high scalability. Thus, they are very suitable for new-generation image compression systems, such as JPEG-2000.

Key-Words: - 5/3 discrete wavelet transform (DWT), IDWT, Parallel-pipelined architecture, Horizontal filter (HF), Vertical filter (VF), Lifting-based architecture, JPEG-2000.

1 Introduction

In the field of digital image processing, the JPEG-2000 standard uses the scalar wavelet transform for image compression [1]; hence, the two-dimensional (2-D) discrete wavelet transform (DWT) has recently been used as a powerful tool for image coding/decoding systems. Two-dimensional DWT demands massive computations, hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). At the kernel of the compression stage of the system is the DWT.

Swelden proposed using the wavelet transform based on lifting scheme for lossy compression [2]. The symmetry of the biorthogonal 5/3 filters and the fact that they are almost orthogonal [2] make them good candidates for image compression application. The coefficients of the filter are quantized before hardware implementation; hence, the multiplier can be replaced by limited quantity of shift registers and adders. Thus, the system hardware is saved, and the system throughput is improved significantly.

In this paper, we proposed a high-efficient architecture for the even and odd parts of 1-D DWT based on lifting scheme. The advantages of the proposed architectures are 100% hardware-utilization, multiplierless, regular structure, simple control flow and high scalability.

The remainder of the paper is organized as follows. Section 2 presents the lifting-based 2-D discrete wavelet transform algorithm. In Section 3, the high-efficient architecture for the 5/3 2-D lifting-based DWT is proposed. Section 4 presents the high-efficient architecture for the 5/3 2-D lifting-based IDWT. Section 5 presents the hardware implementation and performance analysis. Finally, comparison of performance between the proposed architectures and previous works in 2-D DWT is made with conclusions given in Section 6.

2 The Lifting-Based 2-D DWT

Usually the Lifting-based DWT requires less computation compared to the convolution-based approach. However, the savings depend on the length of the filters. During the lifting implementation, no-extra memory buffer is required because of the in-place computation feature of

lifting. This is particularly suitable for the hardware implementation with limited available on-chip memory. Many papers proposed the algorithms and architectures of DWT [4]-[10], but they require massive computation. In 1996, Sweldens proposed a new lifting-based DWT architecture, which requires half of hardware compared to the conventional approaches [2].

The basic principle of the lifting scheme is to factorize the polyphase matrix of a wavelet filter into a sequence of alternating upper and lower triangular matrices and a diagonal matrix [3].

Let $h(z)$ and $g(z)$ be the lowpass and highpass analysis filters. The corresponding polyphase matrices are defined as [3]

$$P(z)=\begin{bmatrix} h_e(z) & h_o(z) \\ g_e(z) & g_o(z) \end{bmatrix} \quad (1)$$

$$g(z)=g_e(z^2)+z^{-1}g_o(z^2) \quad (2)$$

$$h(z)=h_e(z^2)+z^{-1}h_o(z^2) \quad (3)$$

A factorization of $P(z)$ can lead to upper and lower triangular matrix multiplication as:

$$P(z)=\begin{bmatrix} 1 & \alpha(1+z^{-1}) \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ \beta(1+z) & 1 \end{bmatrix} \quad (4)$$

where $\alpha=-1/2$ and $\beta=1/4$.

The architecture of DWT based on lifting scheme involves splitting module, lifting module and scaling module is shown in Figure 1.

3 The High-Efficient Architecture for 5/3 2-D Lifting-Based DWT

The equations of the 5/3 1-D DWT based on lifting scheme is represented as

$H(i)=x(2i+1)+\alpha(x(2i)+x(2i+2))$ (5)

$L(i)=x(2i)+\beta(H(i)+H(i-1))$ (6)

According to eqs. (5) and (6), the architecture of 5/3 1-D DWT based on lifting scheme is shown in Figure 2.

The 5/3 2-D DWT is a multilevel decomposition technique, that decomposes into four subbands such as *HH*, *HL*, *LH* and *LL*. The mathematical formulas of 5/3 2-D DWT are defined as follows:

$$HH(i,j)=H(2i+1,j)+\alpha(H(2i,j)+H(2i+2,j)) \quad (7)$$

$$HL(i,j)=H(2i,j)+\beta(HH(i,j)+HH(i-1,j)) \quad (8)$$

$$LH(i,j)=L(2i+1,j)+\alpha(L(2i,j)+L(2i+2,j)) \quad (9)$$

$$LL(i,j)=L(2i,j)+\beta(LH(i,j)+LH(i-1,j)) \quad (10)$$

According to eqs. (7), (8), (9) and (10), the architecture of 5/3 2-D DWT based on lifting scheme can be derived and shown in Figure 3. The proposed system architecture is shown in Figure 4. In system architecture, the architecture of horizontal filter and the architecture of vertical filter are shown in Figure 5 and 6, respectively. Figure 7 shows architectures of line delays LD1, LD2 and LD in vertical filter. The architectures of PE(α) and PE(β) in horizontal filter (HF) and vertical filter (VF) are shown in Figure 8. The proposed architecture for 5/3 2-D lifting-based DWT is described clearly.

In the proposed architecture of DWT, the data flows of the horizontal filter and the vertical filter can be derived. The architecture performs in $(4N^2(1-4^{-j})+9N)/6$ computation time, when the size of the input image is $N\times N$ and the number of compression level is j. The architecture of 5/3 2-D DWT involves four processor elements, 3.5N+8 registers and seven multiplexers. The hardware utilization is 100%.

4 The High-Efficient Architecture for 5/3 2-D Lifting-Based IDWT

The equations of the 5/3 1-D IDWT based on lifting scheme is represented as follows [3]:

Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000.

The vertical filter is represented as

$L(2i,j)=LL(i,j)-\beta(LH(i,j)+LH(i-1,j))$ (11)

$L(2i+1,j)=LH(i,j)-\alpha(L(2i,j)+L(2i+2,j))$ (12)

$H(2i,j)=HL(i,j)-\beta(HH(i,j)+HH(i-1,j))$ (13)

$H(2i+1,j)=HH(i,j)-\alpha(H(2i,j)+H(2i+2,j))$ (14)

The Horizotal filter is represented as

$x(i,2j)=L(i,j)-\beta(H(i,j)+H(i,j-1))$ (15)

$x(i,2j+1)=H(i,j)-\alpha(x(i,2j)+x(i,2j+2))$ (16)

According to eqs. (11), (12), (13) and (14), the architecture of the vertical filter (IVF) for IDWT is derived and shown in Figure 10. From eqs. (15) and (16), the architecture of the horizontal filter (IHF) for IDWT is derived and shown in Figure 11. In the horizontal filter for IDWT, the architecture of PE(α/β) is shown in Figure 12.

In the proposed architecture of IDWT, the data flows of the horizontal filter and the vertical filter can be derived. The architecture performs in $(4N^2(1-4^{-j})+9N)/6$ computation time. The hardware utilizations of the vertical filter (IVF) and the horizontal filter (IHF) are 100%. The architecture of 5/3 2-D IDWT involves four processor elements, 2N+15 registers and ten multiplexers.

5 Hardware Implementation and Performance Analysis

In the proposed architectures, the multiplier can be replaced by simple shifters and adders. The proposed architecture of 8×8 DWT has been synthesized by Xilinx FPGA Express tools, written in Verilog® [11], and emulated on the Xilinx XC2V4000 FPGA platform [12]-[13]. The chips have been synthesized by TSMC 0.18 μm 1P6M CMOS cell libraries. The core size and power consumption can be obtained from the reports of Synopsys® design analyzer and PrimPower® [14], respectively. The reported core sizes of DWT and IDWT processors are $256\times260\mu m^2$ and $328\times332\mu m^2$, respectively. The power dissipations of DWT and IDWT processor are 5.69 mW and 8.76 mW at 1.8V with clock rate of 50MHz. Figures 13 and 14 show the layout views of the implemented 8×8 DWT and IDWT core processor, respectively.

The 512×512 original image Lena is shown in Figure 15(a) and the reconstructed image Lena is shown in Figure 15(b). By the proposed architectures with fixed point operation, the peak-signal-to-noise ratio (PSNR) of the reconstructed image Lena is 44dB. The proposed 2-D DWT/IDWT processors have been applied to many images with great satisfactions.

6 Conclusion

Filter coefficients are quantized before implementation using the biorthogonal 5/3 wavelet. The hardware is cost-effective and the system is high-speed. The architecture reduces power dissipation by m compared with conventional architectures in m-bit operand (low-power utilization).

In this paper, the high-efficient and low-power architectures for 2-D DWT and IDWT have been proposed. The architectures for DWT and IDWT perform compression and decompression in $(4N^2(1-4^{-j})+9N)/6$ computation time, where the time unit is an addition operation. The control complexity is simple. The comparison of the proposed architectures to other commonly used architectures in 2-D DWT is shown in Table 1 [15], [16], [17]. So far, the papers of 5/3 2-D lifting-based IDWT are rarely published. The proposed architecture for 2-D IDWT is very suitable for VLSI implementation. The design analysis of the proposed architecture is valuable for the future research.

The proposed architectures have been verified by Verilog-HDL and implemented on FPGA. The hardware code can be reused and become as IP. The advantages of the proposed architectures are 100% hardware utilization and ultra low-power. The architectures have regular structures, simple control flows, high throughputs and high scalabilities [18].

References:

[1] *ITU-T Recommendation T.800. JPEG2000 Image Coding System– Part 1, ITU Std.*, July 2002. *http://www.itu.int/ITU-T/.*

[2] W. Sweldens, The Lifting Scheme: A Custom-Design Construction of Biorthogonal Wavelet, *Applied and Computational Harmonic Analysis*, Vol. 3, 1996, pp.186-200.

[3] I. Daubechies, W. Sweldens, Factoring Wavelet Transforms into Lifting Schemes, *J.Fourier Anal. Appl.*,Vol.4, 1998, pp. 247-269.

[4] G. Beylkin, R. Coifman, V. Rokhlin, *Wavelet in Numerical Analysis in Wavelets and their Applications*, New York: Jones and Bartlett, 1992.

[5] A. N. Akansu, R. A. Haddad, *Multiresolution Signal Decomposition: Transform, Subbands and Wavelets*, New York: Academic, 1992.

[6] I. Sodagar, H.-J. Lee, P. Hatrack, Y.-Q. Zhang, Scalable Wavelet Coding for Synthetic/Natural Hybrid Images, *IEEE Trans. Circuits and Systems for Video Technology*, Vol. 9, 1999, pp. 244-254.

[7] D. Taubman, High Performance Scalable Image Compression with EBCOT, *IEEE Trans. Image Processing*, Vol. 9, 2000, pp.1158-1170.

[8] R. Kronland-Martinet, J. Morlet, A. Grossman, Analysis of Sound Patterns through Wavelet Transform, *Int. J. Pattern Recognit. Artif. Intell*., Vol. 1, No. 2, 1987, pp.273-302.

[9] M. A. Stoksik, R. G. Lane, D. T. Nguyen., Accurate Synthesis of Fractional Brownian Motion Using Wavelets, *Electronic Letters*, Vol. 30, No. 5, 1994, pp.384-284.

[10] K. Parhi, T. Nishitani, VLSI Architectures for Discrete Wavelet Transforms," *IEEE Trans. VLSI Systems*, Vol. 1, No. 2, 1993, pp.191-202.

[11] D. E. Thomas, P. H. Moorby, *The Verilog Hardware Description Language*, Fifth Edition, Kluwer Academic Pub., 2002.

[12] Model ModelSim Products: *http://www. model.com/products.*

[13] Xilinx FPGA products, *http://www. xilinx.com/products*.

[14] Synopsys FPGA Express, *http://www. synopsys.com/ products*.

[15] P. Wu., L. Chen, An Efficient Architecture for Two-Dimensional Discrete Wavelet Transform,

IEEE Trans. on Circuits and System for video Tech., No.11, 2001, pp.536-545.

[16] T. Park, S. Jung, High speed lattice based VLSI architecture of 2D Discrete Wavelet Transform for Real Time Video Signal Processing, *IEEE Trans. on Consumer Electronics*, No.48, 2002, pp.1026-1032.

[17] Andra. K, Chakrabarti. C and Acharya. T, A VLSI Architecture for Lifting-Based Forward and Inverse Wavelet Transform, *IEEE Trans. on Signal Processing*, No.50, 2002, pp.966-977.

[18] T.-Y.Sung, Y.-S. Shieh, A High-Speed / Ultra Low-Power Architecture for 2-D Discrete Wavelet Transform," *2005 IEEE International Conference on Systems and Signals (ICSS-2005)*, Kaohsiung, Taiwan, 2005, pp.326-331.

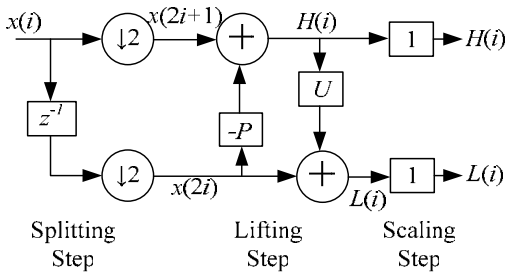

Fig.1. The architecture of DWT based on lifting scheme

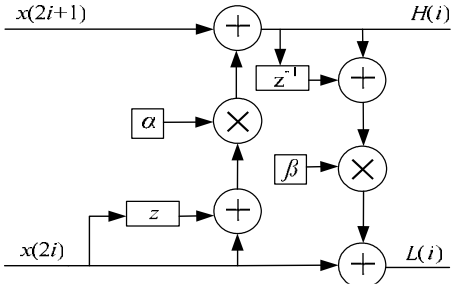

Fig.2. 5/3 1-D lifting-based DWT

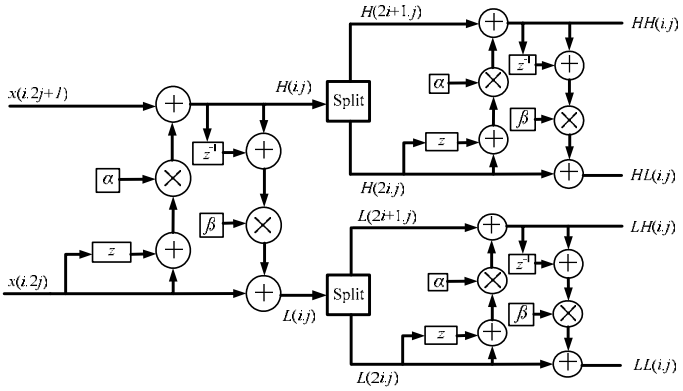

Fig.3. 5/3 2-D lifting-based DWT

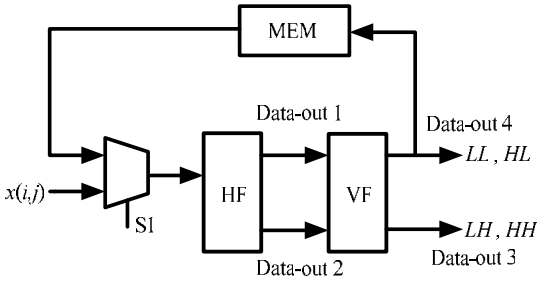

Fig.4. The proposed system architecture of 5/3 2-D lifting-based DWT

Table 1 The comparisons of the proposed architectures to other commonly used architectures in 2-D DWT (C: Convolution-base, L: Lifting-base)

Architecture	Multipliers	Adders	Storage size	Computing time	Control complexity	Hardware ultilization
Wu[15] (C)	$4K$	$4K$	$K+KN$	$0.5N^2$~$0.67N^2$	Medium	100%
Park[16] (C)	$4K$	$4K$	$K(N+j)$	$0.5N^2$~$0.67N^2$	Complex	-
Andra [17] (L)	4	8	$4N$	$0.5N^2$~$0.67N^2$	Medium	100%
This work (L)	0	8	$3.5N$	$0.5N^2$~$0.67N^2$	Simple	100%

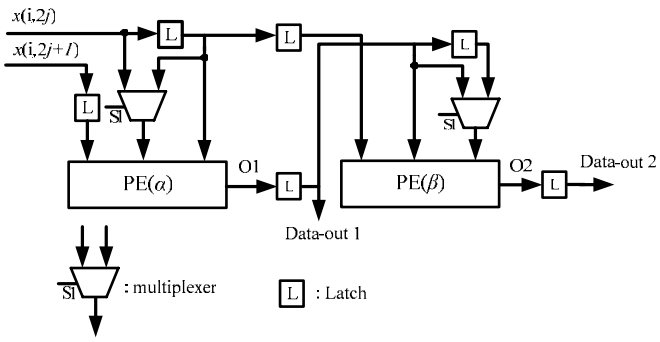

Fig.5. The architecture of horizontal filter (HF)

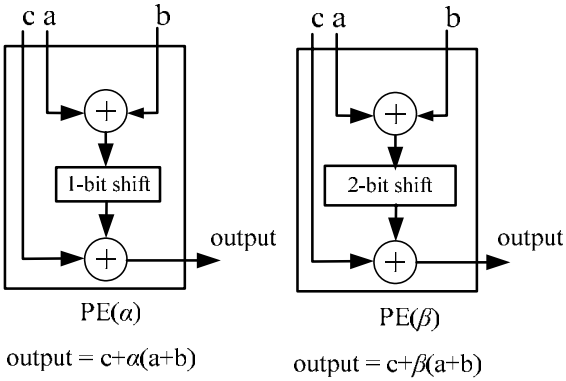

Fig. 8.The architectures of PE(α) and PE(β)

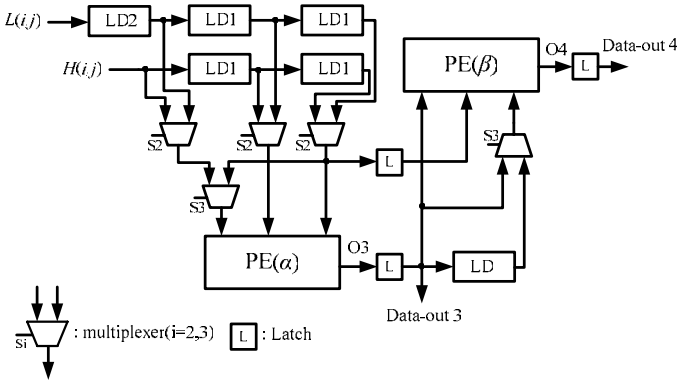

Fig.6. The architecture of vertical filter (VF)

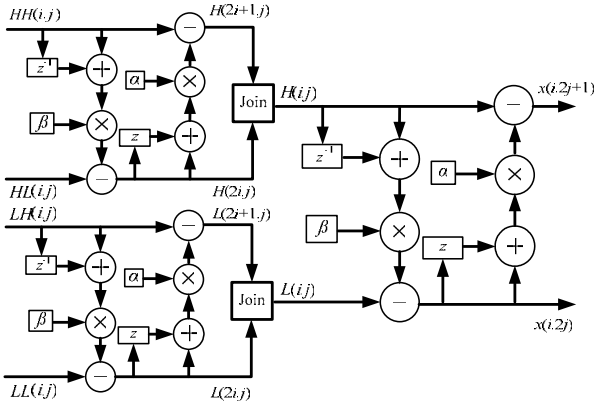

Fig.9. 5/3 2-D lifting-based IDWT

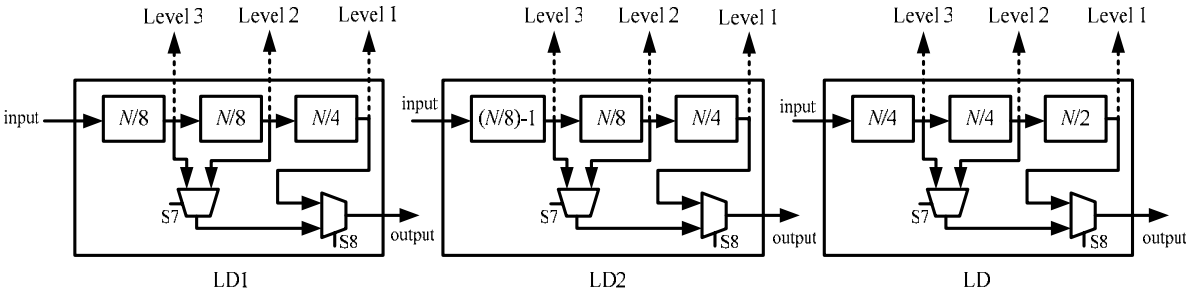

Fig.7. The architectures of LD1, LD2 and LD

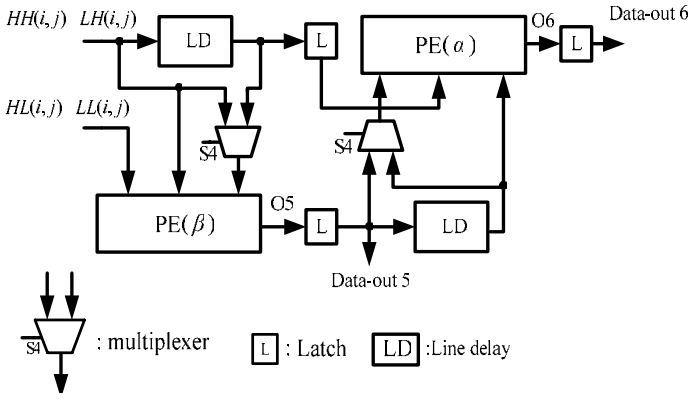

Fig. 10. The architecture of Inverse vertical filter (IVF)

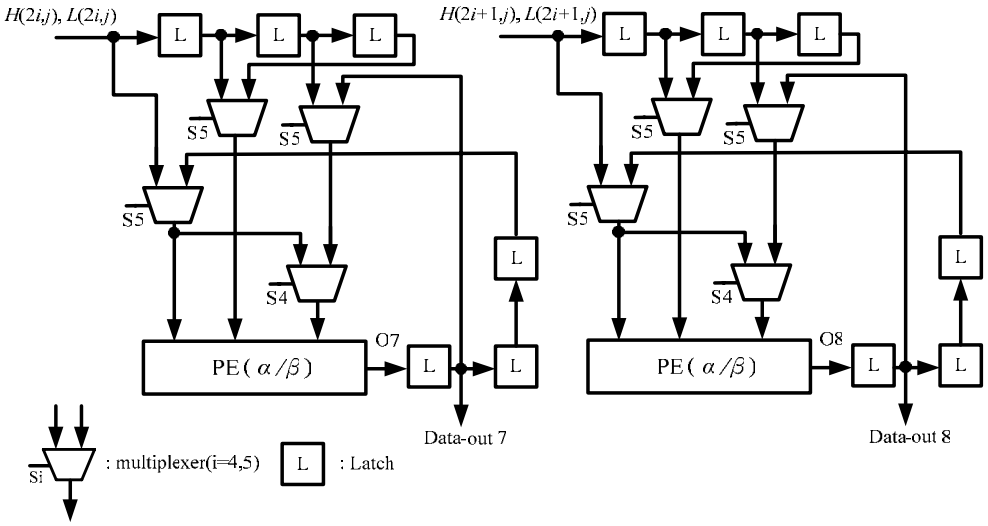

Fig.11. The architecture of inverse horizontal filter (IHF)

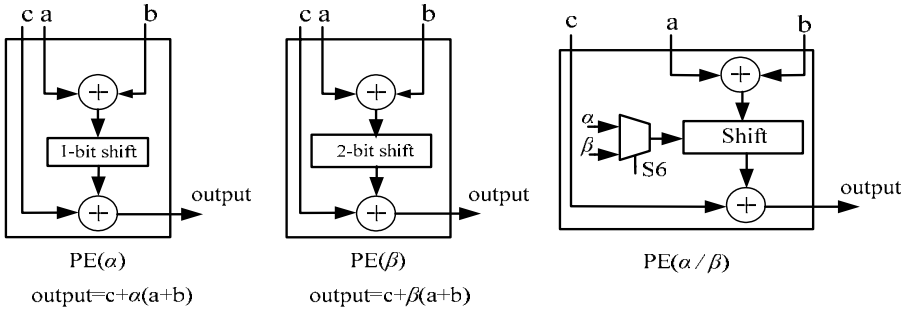

Fig. 12. The architectures of PE(α), PE(β)and PE(α/β)

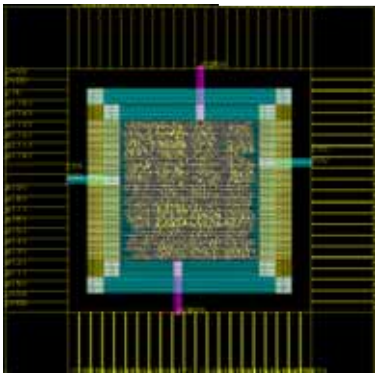

Fig.13.The Layout view of the proposed 2-D DWT core processor

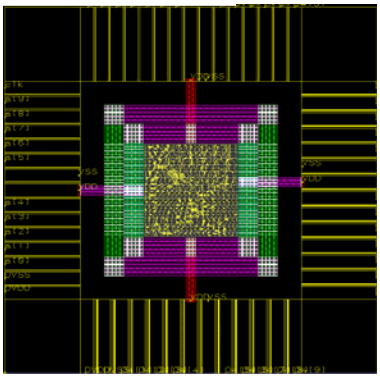

Fig.14. Layout view of the proposed 2-D IDWT core processor

(a)

(b)

Fig.15 (a) Original image (b) Reconstructed image