Memory-Efficient and High-Speed Line-Based Architecture for 2-D Discrete Wavelet Transform with Lifting Scheme

TZE-YUN SUNG
Department of Microelectronics Engineering
Chung Hua University
707, Sec. 2, Wufu Road
Hsinchu, 30012, TAIWAN

Abstract: - In this paper, a high-efficient lined-based architecture for the 9/7 discrete wavelet transform (DWT) based on lifting scheme is proposed. The proposed parallel and pipelined architecture consists of a horizontal filter (HF) and a vertical filter (VF). The critical path of the proposed architecture is reduced. Filter coefficients of the biorthogonal 9/7 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architecture, all multiplications are performed using less shifts and additions. The proposed architecture is 100% hardware utilization and ultra low-power. The architecture has regular structure, simple control flow, high throughput and high scalability. Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000.

Key-Words: - 9/7 discrete wavelet transform (DWT), horizontal filter (HF), vertical filter (VF), lined-based architecture, lifting scheme, JPEG-2000.

1 Introduction

In the field of digital image processing, the JPEG-2000 standard uses the scalar wavelet transform for image compression [1]; hence, the two-dimensional (2-D) discrete wavelet transform (DWT) has recently been used as a powerful tool for image coding/decoding systems. Two-dimensional DWT demands massive computations, hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). At the kernel of the compression stage of the system is the DWT.

Swelden proposed using the biorthogonal 9/7 wavelet based on lifting scheme for lossy compression [2]. The symmetry of the biorthogonal 9/7 filters and the fact that they are almost orthogonal [2] make them good candidates for image compression application. The coefficients of the filter are quantized before hardware implementation; hence, the multiplier can be replaced by limited quantity of shift registers and adders. Thus, the system hardware is saved, and the system throughput is improved significantly.

In this paper, we proposed a high-efficient architecture for the even and odd parts of 1-D DWT based on lifting scheme. The advantages of the proposed architectures are 100% hardware-utilization, multiplierless, regular structure, simple control flow and high scalability.

The remainder of the paper is organized as follows. Section 2 presents the lifting-based 2-D discrete wavelet transform algorithm, and derives new mathematical formulas. In Section 3, the high-efficient architecture for the lifting-based 2-D DWT is proposed. Finally, comparison of performance between the proposed architectures and previous works is made with conclusions given in Section 4.

2 The Lifting-Based 2-D DWT Algorithm

Usually the Lifting-based DWT requires less computation compared to the convolution-based approach. However, the savings depend on the length of the filters. During the lifting implementation, no-extra memory buffer is required because of the in-place computation feature of lifting. This is particularly suitable for the hardware implementation with limited available on-chip memory. Many papers proposed the algorithms and architectures of DWT [3], [4], [5], [6], [7], [8], [9], but they require massive computation. In 1996, Sweldens proposed a new lifting-based DWT architecture, which requires half of hardware compared to the conventional approaches [2]. The discrete wavelet transform factoring into lifting scheme is represented as [10]:

$$\tilde{P}=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}\begin{bmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \delta(1+z) & 1\end{bmatrix}\begin{bmatrix}\zeta & 0\\ 0 & 1/\zeta\end{bmatrix} \quad (1)$$

where α,β,γ and δ are the coefficients of lifting scheme, and ζ and $1/\zeta$ are scale normalization factors.

The architecture based on lifting scheme consists of splitting module, two lifting module and scaling module. The architecture of 9/7 1-D DWT based on lifting scheme is shown in Figure 1.

2.1 The 9/7 2-D DWT Algorithm

According to the architecture of 9/7 1-D DWT based on lifting scheme, the architecture of modified 9/7 2-D DWT based on lifting scheme can be derived and shown in Figure 2. The equations of the 2-D DWT based on lifting scheme is represented as

The horizontal filter (HF) is represented as:

$$H^1(i,j)=x(i,2j+1)+\alpha(x(i,2j)+x(i,2j+2))$$
$$L^1(i,j)=x(i,2j)+\beta(H^1(i,j)+H^1(i,j-1))$$
$$H^2(i,j)=H^1(i,j)+\gamma(L^1(i,j)+L^1(i,j+1)$$
$$L^2(i,j)=L^1(i,j)+\delta(H^2(i,j)+H^2(i,j-1))$$

The vertical filter (VF) is represented as:

High frequency part:

$$HL^1(i,j)=H^2(2i,j)+\beta(HH^1(i,j)+HH^1(i-1,j))$$
$$HH^2(i,j)=HH^1(i,j)+\gamma(HL^1(i,j)+HL^1(i+1,j))$$
$$HL^2(i,j)=HL^1(i,j)+\delta(HH^2(i,j)+HH^2(i-1,j))$$
$$HH(i,j)=HH^2(i,j)\times 1/\zeta^2$$
$$HL(i,j)=HL^2(i,j)$$

Low frequency part:

$$LH^1(i,j)=L^2(2i+1,j)+\alpha(L^2(2i,j)+L^2(2i+2,j))$$
$$LL^1(i,j)=L^2(2i,j)+\beta(LH^1(i,j)+LH^1(i-1,j))$$
$$LH^2(i,j)=LH^1(i,j)+\gamma(LL^1(i,j)+LL^1(i+1,j))$$
$$LL^2(i,j)=LL^1(i,j)+\delta(LH^2(i,j)+LH^2(i-1,j))$$
$$LH(i,j)=LH^2(i,j)$$
$$LL(i,j)=LL^2(i,j)\times\zeta^2$$

2.2 The modified 9/7 2-D DWT Algorithm

According to eq. (1), the transform matrix of the 9/7 DWT based on lifting scheme is modified as

$$\tilde{P}_1(z)=\begin{bmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+z) & 1\end{bmatrix}\begin{bmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \delta(1+z) & 1\end{bmatrix}\begin{bmatrix}\zeta & 0\\ 0 & 1/\zeta\end{bmatrix}$$
$$=\begin{bmatrix}1/\alpha & (1+z^{-1})\\ 0 & 1/\alpha\end{bmatrix}\begin{bmatrix}1/\beta & 0\\ (1+z) & 1/\beta\end{bmatrix}\begin{bmatrix}1/\gamma & (1+z^{-1})\\ 0 & 1/\gamma\end{bmatrix}\begin{bmatrix}1/\delta & 0\\ (1+z) & 1/\delta\end{bmatrix}\begin{bmatrix}\alpha\beta\gamma\delta\zeta & 0\\ 0 & \alpha\beta\gamma\delta/\zeta\end{bmatrix}$$
$$=\begin{bmatrix}1 & 1+z^{-1}\\ 0 & 1/\alpha\end{bmatrix}\begin{bmatrix}1/\alpha\beta & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}1 & 1+z^{-1}\\ 0 & 1/\beta\gamma\end{bmatrix}\begin{bmatrix}1/\gamma\delta & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}\alpha\beta\gamma\delta\zeta & 0\\ 0 & \alpha\beta\gamma/\zeta\end{bmatrix}$$
$$=\begin{bmatrix}1 & 1+z^{-1}\\ 0 & A\end{bmatrix}\begin{bmatrix}B & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}1 & 1+z^{-1}\\ 0 & C\end{bmatrix}\begin{bmatrix}D & 0\\ 1+z & 1\end{bmatrix}\begin{bmatrix}K_0 & 0\\ 0 & K_1\end{bmatrix} \quad (2)$$

where

$A=1/\alpha$, $B=1/\alpha\beta$, $C=1/\beta\gamma$, $D=1/\gamma\delta$, $K_0=\alpha\beta\gamma\delta\zeta$ and $K_1=\alpha\beta\gamma/\zeta$.

The modified horizontal filter (HF) is represented as:

$$H^1(i,j)=A\times x(i,2j+1)+x(i,2j)+x(i,2j+2)$$
$$L^1(i,j)=B\times x(i,2j)+H^1(i,j)+H^1(i,j-1)$$
$$H^2(i,j)=C\times H^1(i,j)+L^1(i,j)+L^1(i,j+1)$$
$$L^2(i,j)=D\times L^1(i,j)+H^2(i,j)+H^2(i,j-1)$$

The modified vertical filter (VF) is represented as:

High frequency part:

$$HH^1(i,j)=A\times H^2(2i+1,j)+H^2(2i,j)+H^2(2i+2,j)$$
$$HL^1(i,j)=B\times H^2(2i,j)+HH^1(i,j)+HH^1(i-1,j)$$
$$HH^2(i,j)=C\times HH^1(i,j)+HL^1(i,j)+HL^1(i+1,j)$$
$$HL^2(i,j)=D\times HL^1(i,j)+HH^2(i,j)+HH^2(i-1,j)$$

Low frequency part:

$$LH^1(i,j)=A\times L^2(2i+1,j)+L^2(2i,j)+L^2(2i+2,j)$$
$$LL^1(i,j)=B\times L^2(2i,j)+LH^1(i,j)+LH^1(i-1,j)$$
$$LH^2(i,j)=C\times LH^1(i,j)+LL^1(i,j)+LL^1(i+1,j)$$
$$LL^2(i,j)=D\times LL^1(i,j)+LH^2(i,j)+LH^2(i-1,j)$$

Finally, four subbands of HH, HL, LH and LL are performed by HH^2, HL^2, LH^2 and LL^2. The equations of four subbands are represented as follows:

$$HH(i,j)=HH^2(i,j)\times K_0^2=HH^2(i,j)\times\alpha^2\beta^2\gamma^2\delta^2\zeta^2$$
$$HL(i,j)=HL^2(i,j)\times K_1K_0=HL^2(i,j)\times\alpha^2\beta^2\gamma^2\delta$$
$$LH(i,j)=LH^2(i,j)\times K_1K_0=LH^2(i,j)\times\alpha^2\beta^2\gamma^2\delta$$
$$LL(i,j)=LL^2(i,j)\times K_1^2=LL^2(i,j)\times\alpha^2\beta^2\gamma^2/\zeta^2$$

According to the equations of modified horizontal filter (HF), the architecture for modified horizontal filter (HF) is proposed and shown in Figure 3. The proposed architecture for modified horizontal filter (HF) consists of input-delay unit, middle-delay unit, back-delay unit, five multiplexers and two processing elements (PEs). The PE(*A/B*) performs O1 and PE(*C/D*) performs O2. Similarly, the proposed architecture for modified vertical filter (VF) is shown in Figure 4. The proposed architecture for modified vertical filter (VF) consists of two delay units (2 Ds), seven long-delay (8 Ds) units, eight multiplexers and two processing elements (PE(*A/B*) and PE(*C/D*)). The architecture of scaling normalization (SN) is shown in Figure 5. The architecture of PE is shown in Figure 6. The

proposed PE architecture reduces the critical path [11]-[15].

3 The High-Efficient Architecture for Lifting-Based 2-D DWT

In 8×8 2-D DWT, it requires 106 clocks to perform 2-D DWT. Clock cycles 2 to 66 perform O1, clock cycles 7 to 70 perform O2, clock cycles 24 to 87 perform O3, and clock cycles 42 to 106 perform O4. Every PE requires $N\times N$ clocks to perform the output. The data flow for HF is shown in Table 1, and the data flow for VF is shown in Table 2. Every PE requires $N\times N$ clocks to perform the output.

Filter coefficients of the biorthogonal 9/7 wavelet low-pass filter are quantized before implementation in the high-speed computation hardware. In the proposed architecture, all multiplications are performed using shifts and additions after approximating the coefficients as a booth binary recoded format. The coefficients of 9/7 wavelet filter with BBRF are shown in Table 3. The multiplier is replaced by a carry-save-adder (CSA(4,2)) and four hardwire shifters in processing element (PE) [13]-[14]. The architecture of replaced multiplier ($\otimes$) in PE(*A/B*), PE(*C/D*) and SN is shown in Figure 7.

The proposed 2-D DWT processor is shown in Figure 8. The proposed system architecture including the core processor for 9/7 2-D lifting-based DWT is shown in Figure 9. The system architecture has been verified by Verilog®-hardware description language (HDL) and implemented on FPGA.

The chip has been synthesized by TSMC $0.18\,\mu m$ 1P6M CMOS cell libraries. The core size and power consumption can be obtained from the reports of Synopsys® design analyzer and PrimPower® [16], respectively. The reported core sizes of DWT processor is $256\times260\,\mu m^2$. The power dissipations of the proposed DWT processor is 5.69 mW at 1.8V with clock rate of 50MHz. Figure 10 shows the layout view of the implemented 8×8 DWT processor.

4 Conclusion

Filter coefficients are quantized before implementation using the biorthogonal 9/7 wavelet. The hardware is cost-effective and the system is high-speed. The architecture reduces power dissipation by *m* compared with conventional architectures in *m*-bit operand (low-power utilization).

In this paper, the high-efficient and low-power architecture for 2-D DWT have been proposed. The architecture performs compression in $4\cdot(1-2^{-2j})\cdot N^2/3\cdot T_a$ computation time, where the time unit (T_a is time of addition operation). The critical path is $2T_a$ and the output latency time is $4N\cdot T_a+8$. The buffer size is $N^2/4+7N+11$. The control complexity is simple. The comparison between previous works [11] [15] and this work is shown in Table 4.

The advantages of the proposed architecture are 100% hardware utilization and ultra low-power. The architecture has regular structure, simple control flow, high throughput and high scalability. Thus, it is very suitable for new-generation image compression systems, such as JPEG-2000.

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Table 3. The coefficients of 9/7 wavelet filter (BBRF: Booth binary recoded format)

Coefficients	Value	BBRF
A	0.63046362	0.101000011
B	11.90000408	$1100.00\tilde{1}01$
C	21.37814969	$10101.01\tilde{1}$
D	2.553775411	$1.100\tilde{1}001$
T	0.001430992	0.000000001
U	0.012411931	0.0000001101
R	0.004165267	0.0000000101

Table 1. The data flow of HF

Clock	*Input*	O1	O2
0	*x(0,0)*		
1	*x(0,1)*		
2	*x(0,2)*		
3	*x(0,3)*	$H^1(0,0)$	
4	*x(0,4)*	$L^1(0,0)$	
5	*x(0,5)*	$H^1(0,1)$	
6	*x(0,6)*	$L^1(0,1)$	
7	*x(0,7)*	$H^1(0,2)$	$H^2(0,0)$
8	*x(1,0)*	$L^1(0,2)$	$L^2(0.0)$
9	*x(1,1)*	$H^1(0,3)$	$H^2(0,1)$
10	*x(1,2)*	$L^1(0,3)$	$L^2(0.1)$
11	*x(1,3)*	$H^1(1,0)$	$H^2(0,2)$
12	*x(1,4)*	$L^1(1,0)$	$L^2(0.2)$
13	*x(1,5)*	$H^1(1,1)$	$H^2(0,3)$
14	*x(1,6)*	$L^1(1,1)$	$L^2(0,3)$
15	*x(1,7)*	$H^1(1,2)$	$H^2(1,0)$
16	*x(2,0)*	$L^1(1,2)$	$L^2(1,0)$
17	*x(2,1)*	$H^1(1,3)$	$H^2(1,1)$
18	*x(2,2)*	$L^1(1,3)$	$L^2(1,1)$
19	*x(2,3)*	$H^1(2,0)$	$H^2(1,2)$
20	*x(2,4)*	$L^1(2,0)$	$L^2(1,2)$

Table 2. The data flow of VF

Clock	*Input*	O3	O4
24	*x(3,0)*	$HH^1(0,0)$	
25	*x(3,1)*	$HL^1(0,0)$	
26	*x(3,2)*	$HH^1(0,1)$	
27	*x(3,3)*	$HL^1(0,1)$	
28	*x(3,4)*	$HH^1(0,2)$	
29	*x(3,5)*	$HL^1(0,2)$	
30	*x(3,6)*	$HH^1(0,3)$	
31	*x(3,7)*	$HL^1(0,3)$	
32	*x(4,0)*	$LH^1(0,0)$	
33	*x(4,1)*	$LL^1(0,0)$	
34	*x(4,2)*	$LH^1(0,1)$	
35	*x(4,3)*	$LL^1(0,1)$	
36	*x(4,4)*	$LH^1(0,2)$	
37	*x(4,5)*	$LL^1(0,2)$	
38	*x(4,6)*	$LH^1(0,3)$	
39	*x(4,7)*	$LL^1(0,3)$	
40	*x(5,0)*	$HH^1(1,0)$	
41	*x(5,1)*	$HL^1(1,0)$	
42	*x(5,2)*	$HH^1(1,1)$	$HH^2(0,0)$
43	*x(5,3)*	$HL^1(1,1)$	$HL^2(0,0)$
44	*x(5,4)*	$HH^1(1,2)$	$HH^2(0,1)$
45	*x(5,5)*	$HL^1(1,2)$	$HL^2(0,1)$
46	*x(5,6)*	$HH^1(1,3)$	$HH^2(0,2)$
47	*x(5,7)*	$HL^1(1,3)$	$HL^2(0,2)$

Table 4. The comparison between previous works and this work
(T_a : time of addition operation, T_m : time of multiplication operation.)

Architecture	Andra [11]	Wu [15]	This work
Buffer size	N^2	$N^2/4+5.5N$	$N^2/4+7N+11$
Multipliers	6	6	---
Adders	8	8	13
Critical Path	$T_m+2\cdot T_a$	T_m	$2\cdot T_a$
Computation time	$\frac{4}{3}(1-2^{-2j})\cdot N^2\cdot T_m$	$(22j+\frac{4}{3}N^2(1-2^{-2j})+6N(1-2^{-j}))\cdot T_m$	$\frac{4}{3}(1-2^{-2j})\cdot N^2\cdot T_a$
Control complexity	Medium	Medium	Simple
Power consumption	High	High	Low
Chip area	Large	Large	Small
Throughput	Low	Low	High
Hardware Utilization	50%	100%	100%

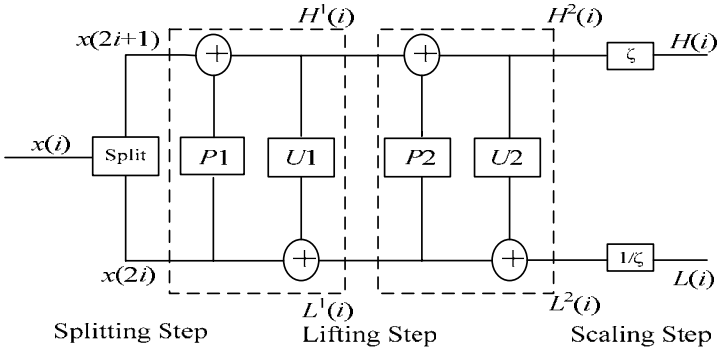

Fig.1. The architecture of 9/7 1-D DWT based on lifting scheme ($P1=\alpha(1+z)$, $U1=\beta(1+z^{-1})$, $P2=\gamma(1+z)$ and $U2=\delta(1+z^{-1})$)

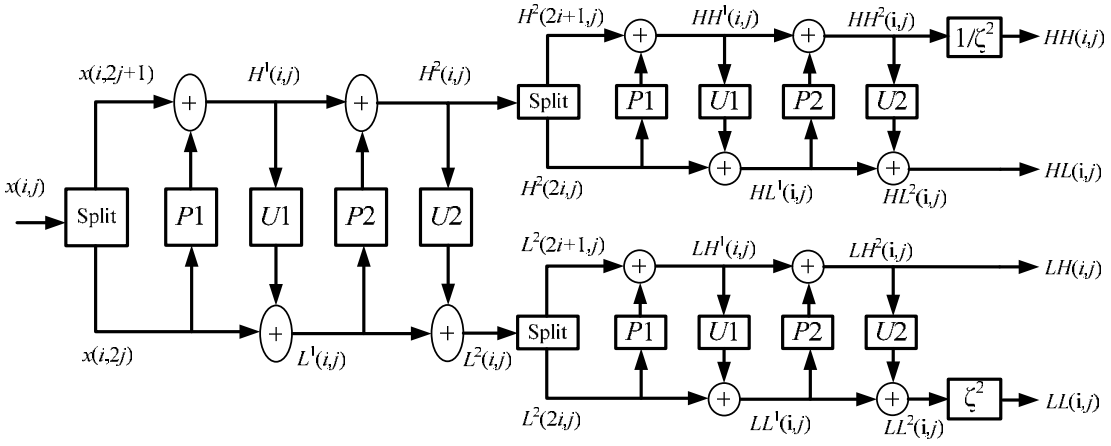

Fig.2. The architecture of modified 9/7 lifting-based DWT

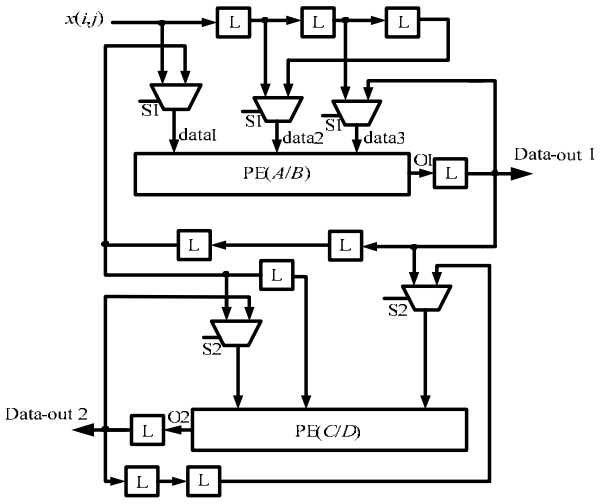

Fig.3. The proposed architecture for horizontal filter (HF) (L: delay unit, S1, S2: select inputs for multiplexers)

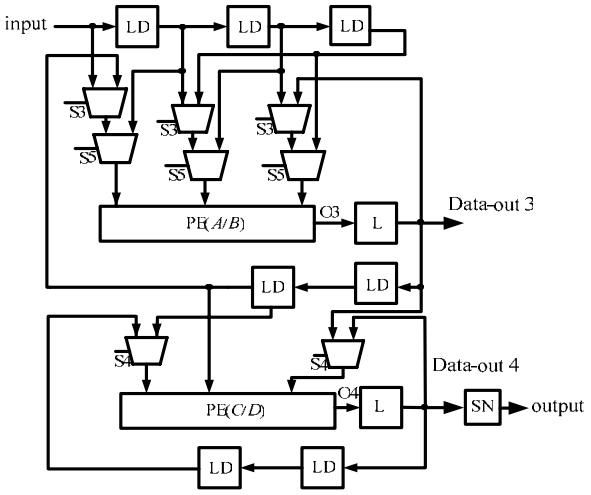

Fig.4. The architecture for vertical filter (VF) (L: delay unit, LD: long delay unit, S3, S4, S5: select inputs for multiplexers, SN: scaling normalization)

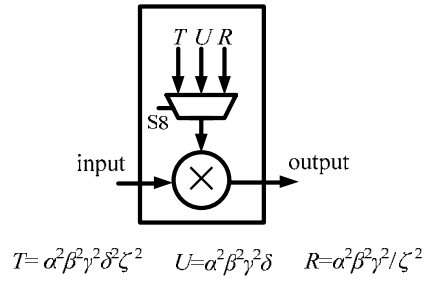

Fig.5. The architecture for scaling normalization (SN)

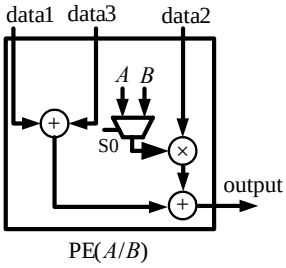

Fig.6. The architecture of PE(*A/B*)
(The PE(*C/D*) has the same architecture)

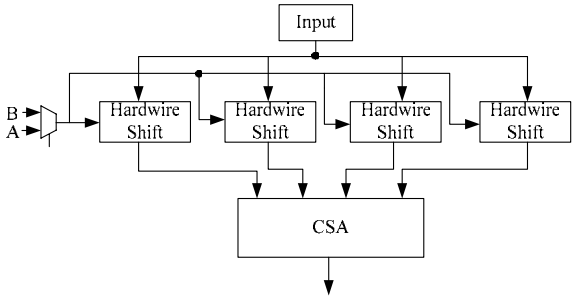

Fig.7. The architecture of replaced multiplier (⊗) in PE(*A/B*), PE(*C/D*) and SN

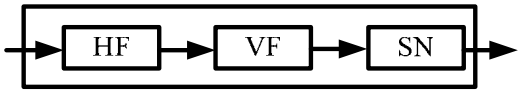

Fig.8. The 2-D DWT processor

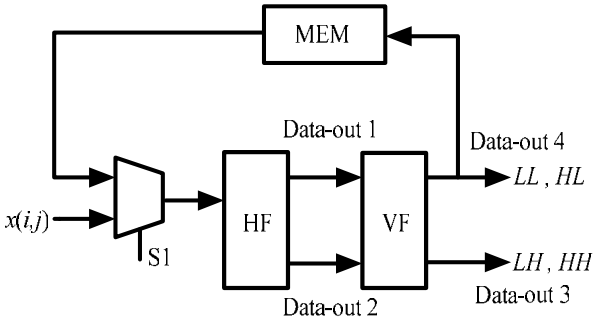

Fig.9. The proposed system architecture for 9/7 2-D lifting-based DWT

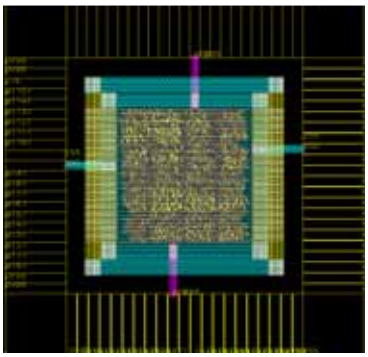

Fig.10. The layout view of the implemented 8×8 DWT processor