

Memory-Efficient and High-Performance 2-D DCT and IDCT Processors Based on CORDIC Rotation

TZE-YUN SUNG
 Department of Microelectronics Engineering
 Chung Hua University
 707, Sec. 2, Wufu Road
 Hsinchu, 30012, TAIWAN
 bobsung@chu.edu.tw

Abstract: - Two-dimensional discrete cosine transform (DCT) and inverse discrete cosine transform (IDCT) have been widely used in many image processing systems. In this paper, efficient architectures with parallel and pipelined structures are proposed to implement 8×8 DCT and IDCT processors. In which, only one bank of SRAM (64 words) and coefficient ROM (6 words) is utilized for saving the memory space. The kernel arithmetic unit, i.e. multiplier, which is demanding in the implementation of DCT and IDCT processors, has been replaced by simple adders and shifters based on the CORDIC algorithm. The proposed architectures for 2-D DCT and IDCT processors not only simplify hardware but also reduce the power consumption with high performances.

Key-Words: - DCT, IDCT, parallel and pipelined architecture, low-power, CORDIC.

1 Introduction

With the rapid growth of modern communication applications and computer technologies, image compression is increasingly in demand. Discrete cosine transform (DCT) has been widely used in the image compression task. Moreover, DCT is adopted by the JPEG, MPEG-4 and H.264 standards.

Conventionally, the double size fast Fourier transform (FFT) algorithm can be used to implement DCT. Nevertheless, FFT involves complex-valued computations. Specifically, for N -point DCT, the number of processor units required is $2 \log 2N$ and the order of computation time is $O(\log 2N + 1)$ by FFT. The VLSI chip implementations of DCT for real-time applications can be found in [1]-[8].

CORDIC (COordinate Rotation DIgital Computer) is a well-known technique that was (and still is) widely used for the calculation of many elementary functions including sine and cosine functions. In this paper, the CORDIC approach to the implementation of fast DCT and IDCT is presented. The proposed CORDIC-based parallel and pipelined architectures for the development of two dimensional DCT and IDCT processors can simplify the hardware complexity and reduce the power consumption as well.

The remainder of this paper proceeds as follows. In Section 2, the CORDIC algorithm is reviewed briefly. In Section 3, fast and efficient CORDIC-

based 2-D DCT and IDCT algorithms are presented. The implementations of the proposed low-power, parallel and pipelined architectures for 2-D DCT and IDCT processors are given in Section 4. Finally, conclusion can be found in Section 5.

2 Review of CORDIC Algorithm

The basic CORDIC algorithm is given by [9]-[10]

$$x_{i+1} = x_i - \sigma_i 2^{-i} y_i \tag{1}$$

$$y_{i+1} = y_i + \sigma_i 2^{-i} x_i \tag{2}$$

$$z_{i+1} = z_i - \sigma_i \alpha_i \tag{3}$$

where $i=0, 1, 2, \dots, n-1$, and

$$\alpha_i = \arctan(2^{-i}) \tag{4}$$

In the i^{th} micro-rotation, the direction of rotation denoted by σ_i is determined by $sign(z_i)$ with $z_n \rightarrow 0$ in the rotation mode; $\sigma_i = -sign(x_i) \cdot sign(y_i)$ with $y_n \rightarrow 0$ in the vectoring mode; and the corresponding scale factor $k_i = \sqrt{1 + \sigma_i^2 2^{-2i}}$. After n micro-rotations, the product of all the scale factors is given by

$$K_1 = \prod_{i=0}^{n-1} k_i = \prod_{i=0}^{n-1} \sqrt{1 + \sigma_i^2 2^{-2i}} = \prod_{i=0}^{n-1} \sqrt{1 + 2^{-2i}} \tag{5}$$

One may take the iteration sequence: $\{0, 0, 0, 1, 2, \dots, n\}$ for the CORDIC algorithm in the circular coordinate system to expand the convergence range of angles as follows.

