Third-Order Quadrature Oscillator with Grounded Capacitors Using CCIIs

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Abstract: A new third-order quadrature oscillator is presented. Outputs of two sinusoids with 90^o phase difference are available in the quadrature oscillator circuit. The oscillation condition and oscillation frequency are orthogonal controllable. The proposed circuit employs only grounded capacitors and is ideal for integration. Experimental results are included to confirm the theoretical analysis.

Key-Words: current conveyor, quadrature oscillator, active circuit, current-mode, third-order

1 Introduction

Current conveyors have been found useful in many applications. In recent years, their applications and advantages in the synthesis of sinusoidal oscillators have received considerable attention [1-2] Quadrature oscillator is used because the circuit provides two sinusoids with 90^o phase difference, as for example in telecommunications for quadrature mixers and single-sideband generators or for measurement purposes in vector generators or selective voltmeters. Therefore, quadrature oscillators constitute an important unit in many communication and instrumentation systems [3-9]. Two-integrator loop technique was developed to realize quadrature oscillators by using operational amplifiers or transconductance elements in [3-4]. Holzel [5] proposed a new method for realizing quadrature oscillator consists of two allpass filters and an inverter using operational amplifiers. Ahmed *et al.* [6] proposed two quadrature oscillator circuits that realized base on the allpass filters and the non-inverting integrators as building blocks using operational transconductance amplifiers (OTAs). Soliman [7] describes several quadrature oscillator circuits based on the modification of two-integrator loop technique using current conveyors. Because the high-order network has high accuracy and high quality factor, it gives good frequency response with low distortion [8]. Prommee and Dejhan [8] proposed two third-order quadrature oscillators using OTAs. In 2005, Horng *et al.* [9] proposed three third-order quadrature oscillator circuits each circuit uses three second-generation current conveyors (CCIIs).

In this paper, another CCIIs based third-order quadrature oscillator circuits are presented. The oscillation condition and oscillation frequency of each proposed quadrature oscillator are orthogonal controllable. The proposed quadrature oscillator uses only grounded capacitors. The use of only grounded capacitors is especially interest from the fabrication point of view [10].

2 Circuit Description

Using standard notation, the port relations of a CCII can be characterized by $v_x = v_y$, $i_z = \pm i_x$ and $i_y = 0$. The CCIIs based third-order quadrature oscillator is shown in Fig. 1.

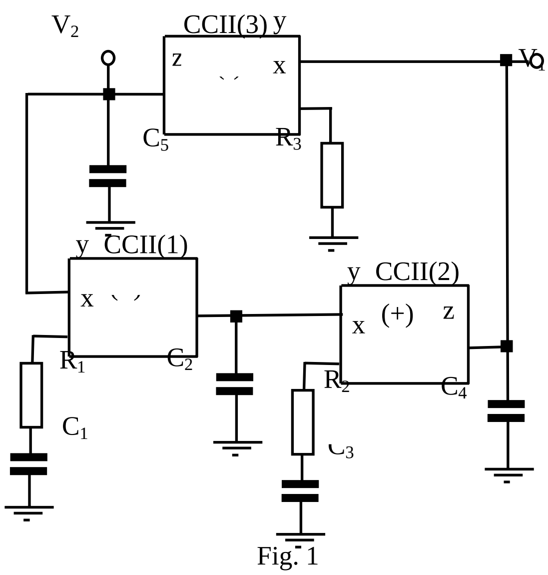

Fig. 1

The characteristic equation of the circuit in Fig. 1 can be expressed as

$$s^3C_1C_2C_3C_4C_5R_1R_2R_3 + s^2C_2C_4C_5R_3(C_1R_1 + C_3R_2) + sC_2C_4C_5R_3 + C_1C_3 = 0 \quad (1)$$

The oscillation condition and oscillation frequency can be obtained as

$$R_3 = \frac{C_1^2 C_3^2 R_1 R_2}{C_2 C_4 C_5 (C_1 R_1 + C_3 R_2)} \quad (2)$$

$$\omega_o = \frac{1}{\sqrt{C_1 C_3 R_1 R_2}} \quad (3)$$

>From equations (2) and (3), the oscillation condition and oscillation frequency can be orthogonal controllable. From Fig. 1, the voltage transfer function from V_2 to V_1 is

$$\frac{V_2(s)}{V_1(s)} = -\frac{1}{sC_5R_3} \quad (4)$$

Under sinusoidal steady state, equation (4) becomes

$$\frac{V_2(j\omega)}{V_1(j\omega)} = \frac{1}{\omega C_5 R_3} e^{j90^o} \quad (5)$$

The phase difference, ϕ, between V_2 and V_1 is

$$\phi = 90^o \quad (6)$$

ensuring the voltages V_2 and V_1 to be in quadrature.

The proposed quadrature oscillator employs only grounded capacitors. The use of grounded capacitors is particularly attractive for integrated circuit implementation [10]. Moreover, the z terminals of the three CCIIs in the proposed circuit are connected to the grounded capacitors, respectively. This design offers the feature of a direct incorporation of the parasitic compensation capacitance (C_p) of each CCII as a part of the main capacitance [11]. Moreover, each x terminal of the three CCIIs in the proposed circuit is connected to single resistor, respectively. This design offers the feature of a direct incorporation of the parasitic resistance (R_x) of each CCII as a part of the main resistance. From equation (5), the magnitude of V_2 and V_1 need not the same. For the applications need equal magnitude quadrature outputs, another amplifying circuits are needed.

3 Non-Ideal Effects

Taking the non-idealities of the CCIIs into account, the relationship can be rewritten as:

$$v_x = \beta(s) v_y \text{ and } i_z = \pm \alpha(s) i_x \quad (7)$$

where $\alpha(s)$ and $\beta(s)$ represent the frequency transfers of the internal current and voltage followers of the CCII, respectively. They can be approximated by the following first order lowpass functions [12].

$$\alpha(s) = \frac{\alpha_o}{1 + s/\omega_\alpha} \quad (8)$$

$$\beta(s) = \frac{\beta_o}{1 + s/\omega_\beta} \quad (9)$$

where $\alpha_o = 0.9914$, $\omega_\alpha = 3.8 \times 10^9$ rad/s, $\beta_o = 0.9999$, $\omega_\beta = 6.48 \times 10^9$ rad/s. Assuming the circuits are working at frequencies much less than the corner frequencies of $\alpha(s)$ and $\beta(s)$, namely, $\alpha(s) = \alpha = 1 - \varepsilon_1$ and ε_1 ($|\varepsilon_1| \ll 1$) denotes the current tracking error and $\beta(s) = \beta = 1 - \varepsilon_2$ and ε_2 ($|\varepsilon_2| \ll 1$) denotes the voltage tracking error of the CCII. The characteristic equation of Fig. 1 becomes

$$s^3C_1C_2C_3C_4C_5R_1R_2R_3 + s^2C_2C_4C_5R_3(C_1R_1 + C_3R_2) + sC_2C_4C_5R_3 + C_1C_3\alpha_1\alpha_2\alpha_3\beta_1\beta_2\beta_3 = 0 \quad (10)$$

The modified oscillation condition and oscillation frequency are

$$R_3 = \frac{C_1^2 C_3^2 R_1 R_2 \alpha_1\alpha_2\alpha_3\beta_1\beta_2\beta_3}{C_2 C_4 C_5 (C_1 R_1 + C_3 R_2)} \quad (11)$$

$$\omega_o = \frac{1}{\sqrt{C_1 C_3 R_1 R_2}} \quad (12)$$

From equations (11) and (12), the tracking errors slightly change oscillation condition. However, the tracking errors have no effects on the oscillation frequency. Moreover, the oscillation condition and oscillation frequency still can be orthogonal controllable. The passive sensitivities are all low and obtained as

$$S^{\omega_o}_{C_1,C_3,R_1,R_2} = -\frac{1}{2}.$$

4 Experimental Results

Experiments were made to verify the feasibility of Fig. 1. The plus-type CCII was implemented using one AD844, the minus-type CCII was implemented using two AD844s from Analog Devices. Fig. 2(a) represents the experimental results of Fig. 1 with $C_1 = C_2 = C_3 = C_4 = C_5 = 1$ nF, $R_1 = R_2 = 1$ kΩ, $R_3 = 300$ Ω and the power supply $\pm$12V. Fig. 2(b) shows the experimental results of the oscillation frequencies of Fig. 1 by varying the value of the resistor R_2 with $C_1 = C_2 = C_3 = C_4 = C_5 = 1$ nF, $R_1 = 1$ kΩ and R_3 was varied with R_2 by equation (2) to ensure the oscillations will start. The highest oscillation frequency is 205.6 kHz from the bread board implementation.

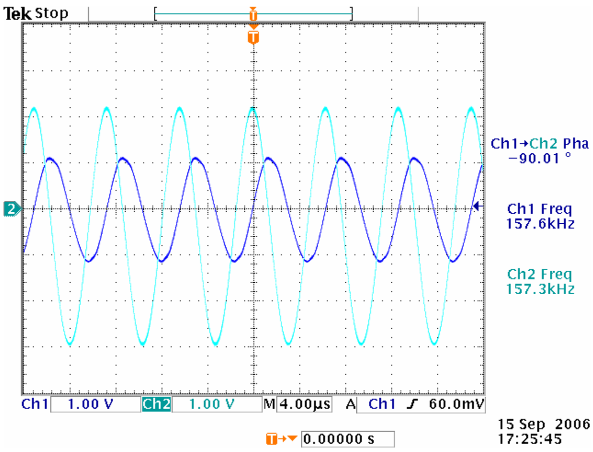

Fig. 2 (a)

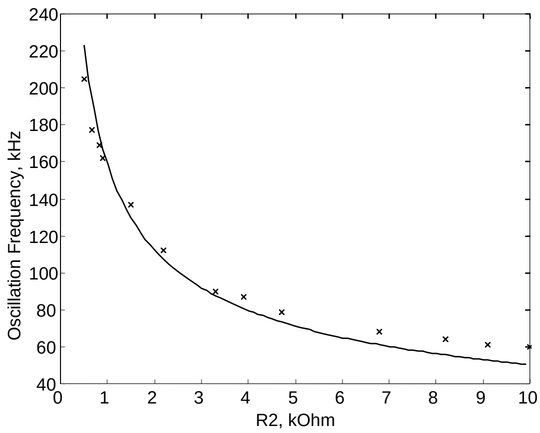

Fig. 2(b)

5 Conclusion

In this paper, a new third-order quadrature oscillator is proposed. Outputs of two sinusoids with 90^o phase difference are available in the proposed quadrature oscillator. The oscillation condition and oscillation frequency of the proposed quadrature oscillator are orthogonal controllable. The proposed circuit employs only grounded capacitors. The z terminals of the three CCIIs in the proposed circuit are connected to the grounded capacitors, respectively. This design offers the feature of a direct incorporation of the parasitic compensation capacitance as a part of the main capacitance. Each x terminal of the three CCIIs in the proposed circuit is connected to single resistor, respectively. This design offers another feature of a direct incorporation of the parasitic resistance as a part of the main resistance.

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