VHDL Modelling of the Open Short Tester

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Abstract: - IC (Integrated Circuitry) testing requires the very advanced and sophisticated Advance Test Equipment (ATE) that costs multi million USD. The cost of IC testing is increasing yearly and it will exceed the cost of manufacturing in future. The manufacturers are interested to lower down the manufacturing cost. Low cost tester is one of the options to reduce the manufacturing cost. The low cost FPGA realization of Open/Short Test on IC is introduced to reduce the IC test cost. The open short test is selected, because it is the first IC test. The Very High Speed Integrated Circuit Hardware Description Language (VHDL) is used to model the Open/Short Test on IC and the design is capable to perform the open/short test.

Key-Words: - open short test, VHDL modelling, IC tester

1 Introduction

The cost of an integrated circuit (IC) includes the design cost, the manufacturing cost and the testing cost. The IC testing becomes more challenging and complex when the IC become smaller and more transistors accommodated in a single IC. A very advance and sophisticated ATE that costs multi million USD is required to perform the IC testing. The manufacturers always try to reduce the manufacturing costs to control the IC selling price.

The low cost FPGA realization of open/short tester approach can reduce the manufacturing costs. The FPGA is a programmable logic device (PLD) that can be programmed to perform any digital tasks. The implementation cost of the FPGA is low because the FPGA is reprogrammable and has very high density of logics available for programming and also acts as storage elements.

A prototype of FPGA open/short tester is designed. The prototype tester can measure 4 IC pins only to perform the open short test, because the same method can be duplicated to support more test pins. It can be easily duplicated to measure 8 IC pins, 16 IC pins or even 100 IC pins by increasing the number of hardware designed. The FPGA open/short tester is more cost effective compare to the Agilent technologies and Tektronix testers.

2 ESD Test

The IC fabrications are dominated by the advanced Complementary Metal Oxide Semiconductor (CMOS) technology because the CMOS IC will have low static power consumption, high noise margin and high integration. However the MOS devices are particularly vulnerable to ESD event [1]. The ESD phenomena become a serious problem for IC products fabricated by deep-submicron CMOS technologies. Electrostatic discharge (ESD) refers to the sudden transfer (discharge) of static charge between objects at different electrostatic potential [2]. It belongs to the family of electrical problems known as electrical overstress (EOS). Other members of EOS family include lighting and electromagnetic pulses (EMP). ESD/EOS is responsible for nearly 40% of the failed integrated circuits (ICs) returned by customer [1].

The three primary ESD test methods are HBM (Human Body Model), MM (Machine Model) and CDM (Charge Device Model). The models used to perform device testing cannot duplicate the full spectrum of all possible ESD events. But these models have been proven to be successful in reproducing over 95% of all ESD field failure signatures [3].

3 Open Short Test

The PN junction diodes are used as the ESD clamp device. The ESD clamp device is shown in Fig 1. The bonding pad is used to connect the internal circuits of an IC to the outside world and between the bonding pad and Input/Output (I/O) pins, there will be electrostatic discharge (ESD) clamp circuit to protect the IC from the ESD event.

The simple ESD clamp circuit consists of a pair diodes connect in series as shown on Fig 1. Open/short circuit test on IC is performed by determine the whether both diodes which connected in series are function correctly or not. The diodes pair is used to perform the open short test.

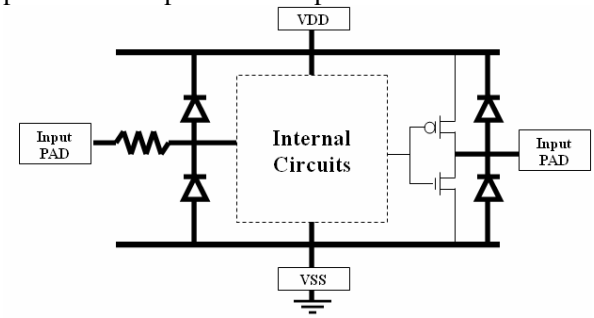


Fig 1: The diodes serve as the ESD clamp device

A precision measurement unit (PMU) is used to perform the open/short test. The PMU is the DC measurement devices. It clamps the voltage and current into a specific limited range of voltage and current. It also can set the upper and lower limit of the measure value to determine whether the device under test (DUT) is pass or fail the open/short test. It will forces the current and measures the voltage or vice versa. The following steps are used to test the upper ESD diode:

- Ground all the pins including V_{SS} and V_{DD}
- The PMU is used to force a positive current of ~100µA to one IC pin at a time.
- The PMU clamps the voltage at +5.0V.
- The upper PMU test limit is set to fail the open test if the measured result is >1.5V.
- The lower PMU test limit is set to fail the short test if the measured result is <0.2V.

Fig 2 shows the configuration to measure the upper ESD diode.

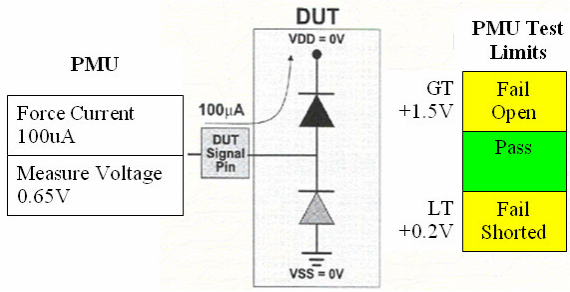


Fig 2: PMU pump 100uA into the I/O pin and measure the voltage drop across the upper diode.

The following steps are used to test the lower ESD diode:

- Ground all pins including V_{SS} and V_{DD}
- The PMU is used to force a negative current of ~ -100µA to one IC pin at a time.
- The PMU clamps the voltage at -5.0V.
- The upper PMU test limit is set to fail the short test if the measured result is > -0.2V.
- The lower PMU test limit is set to fail the open test if the measured result is < -1.5V.

Fig 3 shows the configuration to test the lower ESD diode.

The PMU is clamped the voltage at 5V in order to test the upper diode. The upper diode will be in forward bias and the lower diode will be in reverse bias because the V_{DD} now is grounded (0V). The 100uA current will flow through the good upper diode and give a voltage drop about 0.4-0.7V across the upper diode.

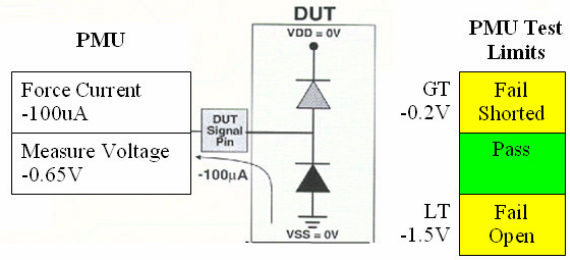


Fig 3: PMU pump -100uA into the I/O pin and measure the voltage drop across the lower diode

The voltage measured is greater than 1.5V, if the pin is open circuit. This may caused by malfunction diode or the broken wire between the IC package and the die. No current will flow through the diode and the measured voltage will be floating ~ 5V.

The voltage measured is less than 0.2V, if the pin fails the short test. The short circuit may cause by the test pin falsely in touch with other I/O pins which already ground in the first place. The current will flows to the ground that has lower resistance instead of the diode that has higher resistance.

Same theory is applied in test for lower diode, where everything will happen in the reverse way as all the supplied input voltage and output are in negative polarity.

4 Field Programmable Gate Array

The field programmable gate array (FPGA) has the similar architecture as general Complex Programmable Logic Device (CPLD). The main different between a FPGA and a CPLD is the different functional logic that used in their design. In the CPLD, the functional logic is called PLD but the functional logic in FPGA is called complex logic block (CLB). The density and size of a CLB is much smaller compare to size and density of a PLD. But inside a FPGA, there is much more CLBs compare to the numbers of PLDs inside the CPLD. These

CLBs are distributed across the entire chip and connected through the programmable interconnection [5, 6].

The UP2 Education Board is used for the FPGA realization. The UP2 Education Board is a stand-alone experiment board based on an Altera FLEX® 10K device and includes a MAX® 7000 device. The FLEX® 10K device is actually categorized as the Field Programmable Logic Array (FPGA) family. On the other hand the MAX® 7000 device can be categorized as Complex Programmable Logic Device (CPLD) family.

5 VHDL

VHDL is a programming language that describes a digital logic block by function, data flow behaviour, and/or structure. This hardware description language (HDL) is used to model the behaviour or function of the designed digital logic block and then only configure the PLD, such as FPGA or CPLD.

6 Design Methodology

The design of the FPGA Realization of Open/Short Test on IC is separated into a several digital blocks as shown on Fig 4. There are five main modules, step down frequency module, state machine module, storage module, display module and PC interface module.

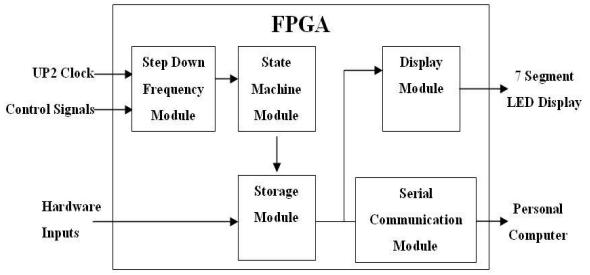
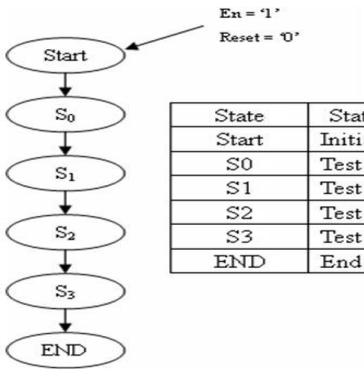


Fig 4: Digital Blocks of FPGA Realization of Open/Short Test on IC

A step down frequency module is required to provide a clock signal that synchronises both the FPGA chip and the hardware circuitries. In Altera UP2 Education Board, a 25.175 MHz crystal oscillator is attached. However the hardware designed properly working at lower frequency than 25.175MHz. The step down frequency module step downs the frequency to the lower frequency. The frequency divide-by-N (f / N) technique is used to step down the frequency. The behaviour of a counter is modelled, which will toggle its output after N counts of the input clock signal.

A finite state machine (FSM) is designed and is implemented using the VHDL. The FSM is used to automate a test sequence to perform the open/short test on Integrated Circuit (IC). The Moore machine is implemented as FSM, since the output of each state is fixed. The FSM is shown in Fig 5.



State	State Representation
Start	Initial state
S0	Test Pin No.1
S1	Test Pin No.2
S2	Test Pin No.3
S3	Test Pin No.4
END	End of Test

Fig 5: State Diagram and State Representation of the Designed Moore Machine

The FSM module controls the sequence of the IC pin that performing the open/short test. The result of the open/short tests on each individual IC pin are fetched into the FPGA to determine weather the IC pin pass or fail the open/short test. The data storage modules are used to store the open/short test results on each individual IC pin tested. The open/short test result carries two bits of binary information. An 8-bits register is required to store the result of the 4 pin IC open/short test and the result of the test is displayed using the dual-digit 7-segment displays attached at the UP2.

7 Simulation Results

The step down frequency module is designed using the VHDL by setting the counter value, N = 1258. The specifications of the step down frequency module are:

$f_1 = f_0 (1/2N)$

Input frequency, f_0 = 25.175MHz

Output frequency, f_1 = 10KHz

The simulation result is shown in Fig 6. The output clock time period is 100.015us that is more than 100us that expected. The reason behind this is due the delay of logics required in construct the step down frequency module.

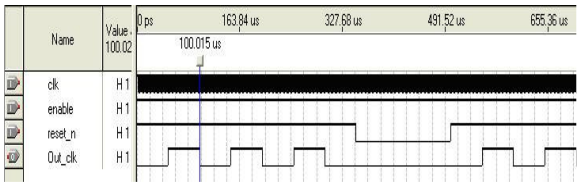


Fig 6: Simulation Result of the Step Down Frequency Module

The state machine specifications are on Table 1 and the simulation result is shown in Fig 7. As shown in Fig 7, the "StateOutput" changed from START → S0 → S1 → S2 → S3 →END as per design specifications required. The "Y" node is the IC pin that selected to perform the open/short test. The "Z000", represent the first IC pin is selected to perform open/short test on IC and other 3 IC pins are shorted. While the "Y" output is "0Z00", it represent the second IC pin is selected to undergo the open/short test and the rest of 3 IC pins are shorted.

Table 1: StateOutput and Y Value

State	State Output Value	Y Value
Start	0000	ZZZZ
S0	0001	Z000
S1	0010	0Z00
S2	0100	00Z0
S3	1000	000Z
End	1111	ZZZZ

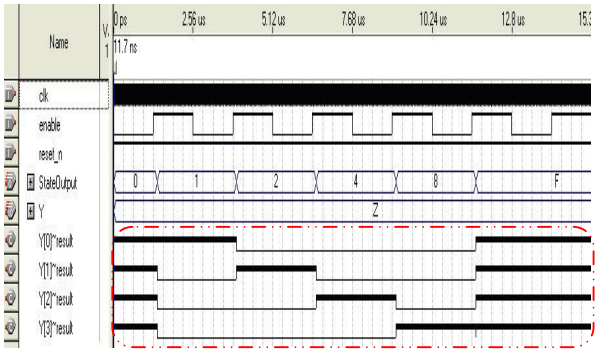


Fig 7: Simulation Result of the State Machine Module

Fig 8 shows the simulation result of the storage module designed. The input ports are Input0, Input1, Input2 and Input3 and the 8-bits storage register is "StoreResult". With Input0="11", Input1="01", Input2="10" and Input3="11", the expected result of 8-bits register is "11100111" or "E7"in hexadecimal.

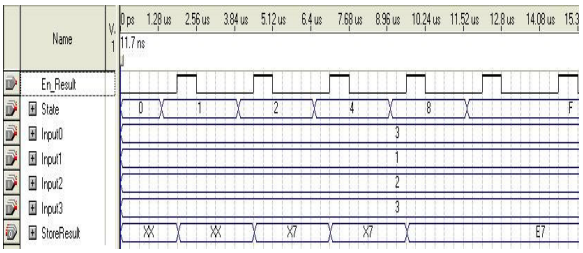


Fig 8: Simulation Result of Storage Module

The dual 7-segment display output values are shown in Table 2 and the simulation result is shown in Fig 9. At the first positive edge, the state is START, and the output for the Digit1 and Digit2 of the dual-digit 7-segment displays are "00" and "00". At the second positive edge, the state is P1, where it means test the IC pin number one, the Digit1 and Digit2 will show alphabet "P" and "1" and its corresponding value is "98" and "CF". The third positive edge, the state change to "RP1" where it shows the open/short test result of IC pin one. For this case, the IC pin number one fails the open test. Digit1 and Digit2 will show alphabet "F" and "S" and the corresponding value is "B8" and "81".

Table 2: The Dual-Digit 7-Segment Output Value

STATE	Digit1 Value (Hexadecimal)	Digit2 Value (Hexadecimal)
START	00	00
P1	98	CF
P2	98	92
P3	98	86
P4	98	CC
Fail Short	B8	A4
Fail Open	B8	81
Pass	98	A4
Undefined	B8	B8
END	FF	FF

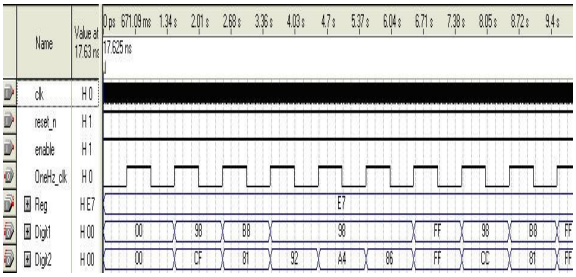


Fig 9: Simulation Result of the Display Module

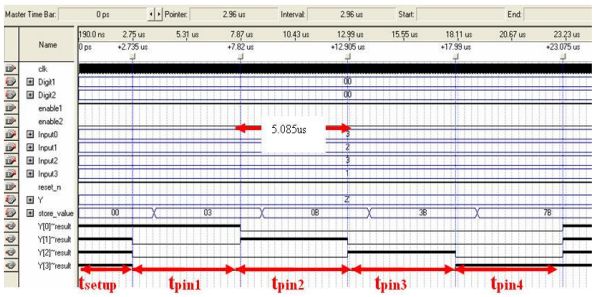


Fig 10: Simulation Result of Open/Short Test

The time required to perform open/short test on 4 upper protecting diodes are shown in Fig 10. The time required to perform open/short test on 4 upper protecting diodes are $T_{upper}=t_{setup}+Nt_{pin}$. The T_{setup} is the setup time of the open/short tester, N is the number of the IC pins tested and T_{pin} is the time required to perform the test on an upper protecting diode. The setup time, t_{setup} is 2.735us and $t_{pin} = t_{pin1} - t_{pin2}$ = 5.085us. For N = 4, the T_{upper} = 23.075us. The time required performing the open/short test on the lower protecting diode, T_{lower} is equal to the time required to perform open/short test on upper protecting diode. The total time, T_{tot} required to perform the open/short test on both the upper and lower protecting diode is $T_{tot}=T_{lower}+T_{upper}+T_{delay}$ = 3.04615ms. The T_{delay}, 3ms is required to turn on the negative voltage supply using a mechanical relay.

8 Conclusions

The open/short test design is successfully modelled using VHDL and the simulation results show that the designs are working well. The VHDL codes are successfully downloaded to the FPGA to perform the open/short test. The design consists of frequency step down module, state machine module, storage module and display module. The total time required to perform the 4 pins open/short test is 3.04615ms.

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