A Programmable ASIC Design of a Low Sensitivity Sampled Data Filter

Dr. Sherif Michael
Electrical and Computer Engineering Department / Space Systems Academic Group

Naval Postgraduate School, Monterey, California, 93943 USA

Abstract: *- In this paper, a CMOS custom Integrated Circuit featuring a multi-stage Universal Switched-Capacitor (SC) Filter is introduced. The network is based on the Generalized Immittance Converter (GIC) configuration, known for its excellent passive and active sensitivities. CMOS switches were used for elements relocation and are digitally controlled to select and realize different filter topologies. Switches were also used to control banks of binary-weighted capacitors that determine the filter center frequency, quality factor as well as its order. The bilinear transformation was utilized in the SC implementation of the filter resistive elements. Extra care was considered in the design procedure to minimize the effect of stray capacitors on the network transfer functions. The result was a general purpose digitally programmable multi-stage network that can equally compete with the best available stray insensitive filter. The design also inherits the low active and passive sensitivities the GIC enjoys.*

Key-Words*: ASIC – VLSI – Programmable Filters – Switched Capacitors- Low Sensitivity – Low Power*

1 Introduction:

Continuous analog circuits are composed of resistors, capacitors, and active devices. However, the performance of these circuits depends upon the accuracy of the resistors and capacitors. Especially in filters, this becomes a serious problem because the RC product must be accurately defined for a desired performance. To obtain a sufficient accuracy, most of the circuits designed using these elements need external timing. Another serious problem is the changes in the passive components values as temperature varies. Resistor and capacitor values do not change by the same amount and in the same direction, which may pose a serious problem for precision design. Besides these undesirable properties, large values of time constants require large values of components which could be unrealistic in VLSI implementation.

Sampled data techniques provide a unique solution to the problem of the implementation of analog Integrated Circuits. Filters using switched-capacitor (SC) techniques overcome a major obstacle to filter-on-a-chip fabrication, by simulating resistors with high-speed switched capacitors. Such approach, eliminates the necessity for precise integrated resistor values that require costly trimming procedures and permits fabrication of precise monolithic analog capacitor filter. This result is due to the fact that the circuit performance and accuracy is determined by capacitor ratios. Ratios of elements are always easier to control. Current MOS IC technology can implement capacitor ratios to within about 0.1% of the specified values. Since the only concern is the ratio rather than absolute individual values of capacitors, therefore, very small capacitance values can be used in the integrated circuit, resulting in smaller chip areas.

There are several topologies in the literature that correspond to different transformations to realize a resistor using switched capacitor techniques [1-3]. In this research the Bilinear SC resistor realization is used due to its well known advantages over other transformations [2]. It can be easily shown that this realization results in an equivalent resistor $R_{eq} = 1/4Cf_c$ where f_c is the sampling frequency. The goal in this research was to adapt this technique to the design of a general purpose programmable filter. Other SC techniques for resistor emulations were also considered, namely, Modified open-loop floating resistor (MOFR) and toggle-switched capacitor and inverter (TSC) or (TSI). Only the Bilinear topology was considered in this design.

1.1 The Programmable Filter:

The availability of a fully integrated analog filter with digitally controlled "programmable" coefficients has been the goal of many researchers due to its several attractions. One possibility of a compact, versatile integrated filter under remote control, opens up many novel

and independent application areas. This is especially true, due to the increasing interest in Neural Networks, where such filter would be useful. Also when the programmable filter is combined with a permanent reference memory which is user-programmable, would form an economical and versatile device for dedicated stand-alone applications. The need for such a device was motivated by advancement in MOS and semiconductor technologies as well as the continuous upgrading of system specifications to take advantage of the available technologies to the limits.

Previously, the author presented a continuous digitally programmable active filter design [4]. The design was based on the Generalized Immittance Converter GIC filter which is well known for its excellent performance [5&6] and shown in Fig.1.

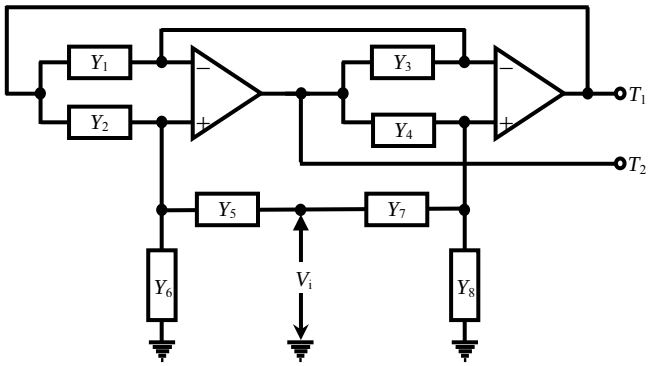

Fig. 1. The Generalized Immittance Converter (GIC)

The GIC configuration was specifically chosen due to its low active and passive sensitivity compared to any available biquadratic section. The corresponding transfer functions, T_1 and T_2 are shown below:

$$T_1 = \frac{v_{(1)}}{v_i} = \frac{Y_1Y_4Y_5 + Y_3Y_7\left(Y_2 + Y_6\right) - Y_3Y_5Y_8}{Y_1Y_4\left(Y_5 + Y_6\right) + Y_2Y_3\left(Y_7 + Y_8\right)}$$

$$T_2 = \frac{v_{(2)}}{v_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4\left(Y_5 + Y_6\right) + Y_2Y_3\left(Y_7 + Y_8\right)}$$

By appropriately selecting the admittances elements, different filtering topologies can be realized as shown in Table 1 below:

Filter Type	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8
Lowpass	G	C	C+G/Q_p	G	G	0	O	G
Highpass	G	G	C	G	0	G	C	G/Q_p
Bandpass	G	G	C	G	0	G	G/Q_p	C
Notch	G	G	C	G	G	0	C	G/Q_p

Table 1. GIC Filter Admittance Values for four Topologies.

Fig.2. shows the programmable GIC filter with the corresponding switching arrangements to realize different filtering topologies, listed in Table1.

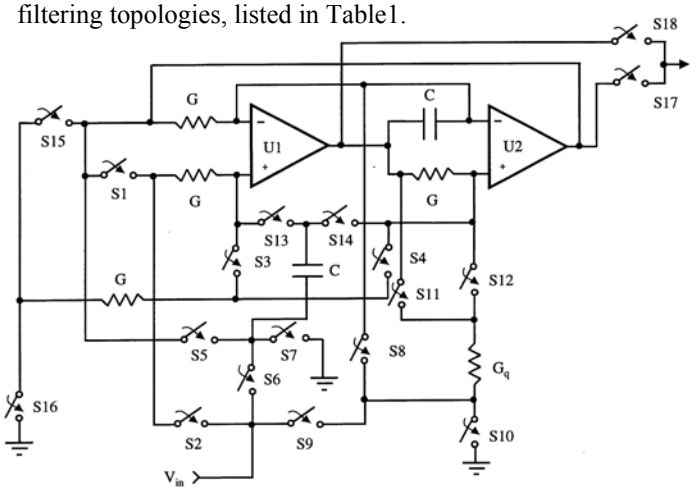

Fig. 2. The GIC filter with Programmable Topologies.

This realization is done by relocating the different passive elements shown using CMOS switches, according to the previous Table.. These switches are driven by a digital decoding circuit of Fig. 3 below, whose binary input is used for selecting the filter topology. This is the minimized logic of Table 2.

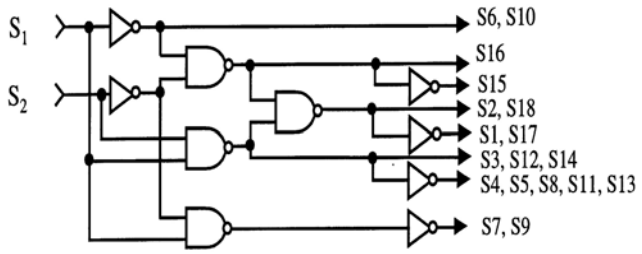

Fig. 3. Control Logic used to drive Fig. 2, CMOS Switches.

S_1	S_2	Topology	Active Switches							
0	0	Notch Filter	S2	S3	S6	S10	S12	S14	S15	S18
0	1	High-Pass Filter	S1	S3	S6	S10	S12	S14	S16	S17
1	0	Band-Pass Filter	S1	S3	S7	S9	S12	S14	S16	S17
1	1	Low-Pass Filter	S2	S4	S5	S8	S11	S13	S16	S18

Table 2. The Truth Table of the Logic Circuit of Fig. 2.

The filter center frequency f_o , as well as Q_p are selected using two sets of binary words that control banks of binary weighted capacitors to select f_o , shown in Fig 4.a, Each set replaces the capacitor C of Fig. 2. Another network containing a set of binary weighted Switched-Capacitors, representing a Bilinear equivalent variable resistors, to select Q_p, shown in Fig. 4.b. This network replaces the admittance G_q of Fig. 2. These programmable networks provide the capability of individually and independently programming both of the filter center frequency and Q_p.

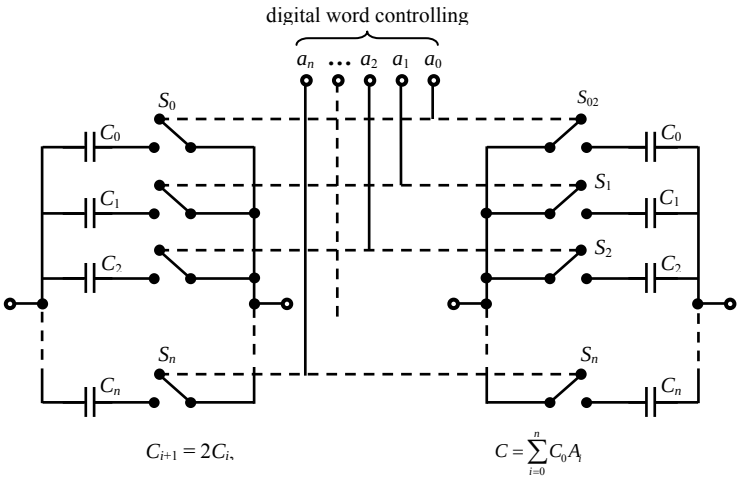

Figure 4.a. Capacitors realization for ω_p programmability.

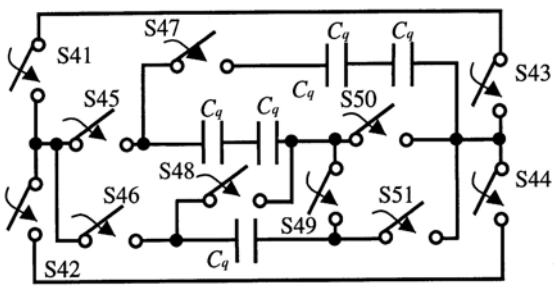

Fig.4.b. Bilinear SC network for Q_p Programmability.

To reduce the parasitic capacitors effects several design techniques, including manipulation of popular frequency transforms, for the switched-capacitor implementation of the filter resistors had to be incorporated. These designs contributed to several modifications to the original GIC design. Fig 5, illustrates the final modified design proposed in this paper..

Sample computer simulations of the programmable filter are shown in Fig. 6. Where Fig. 6.a, illustrates an example of a Band-Pass Filter center frequency programming. Figs. 6.b&c, show the programming of the cutoff frequencies of a High-Pass and Low-Pass Filters, respectively. While Fig. 6.d, illustrates the Band-Pass Filter Quality Factor (Q_p) programmability design, including all controlling switches.

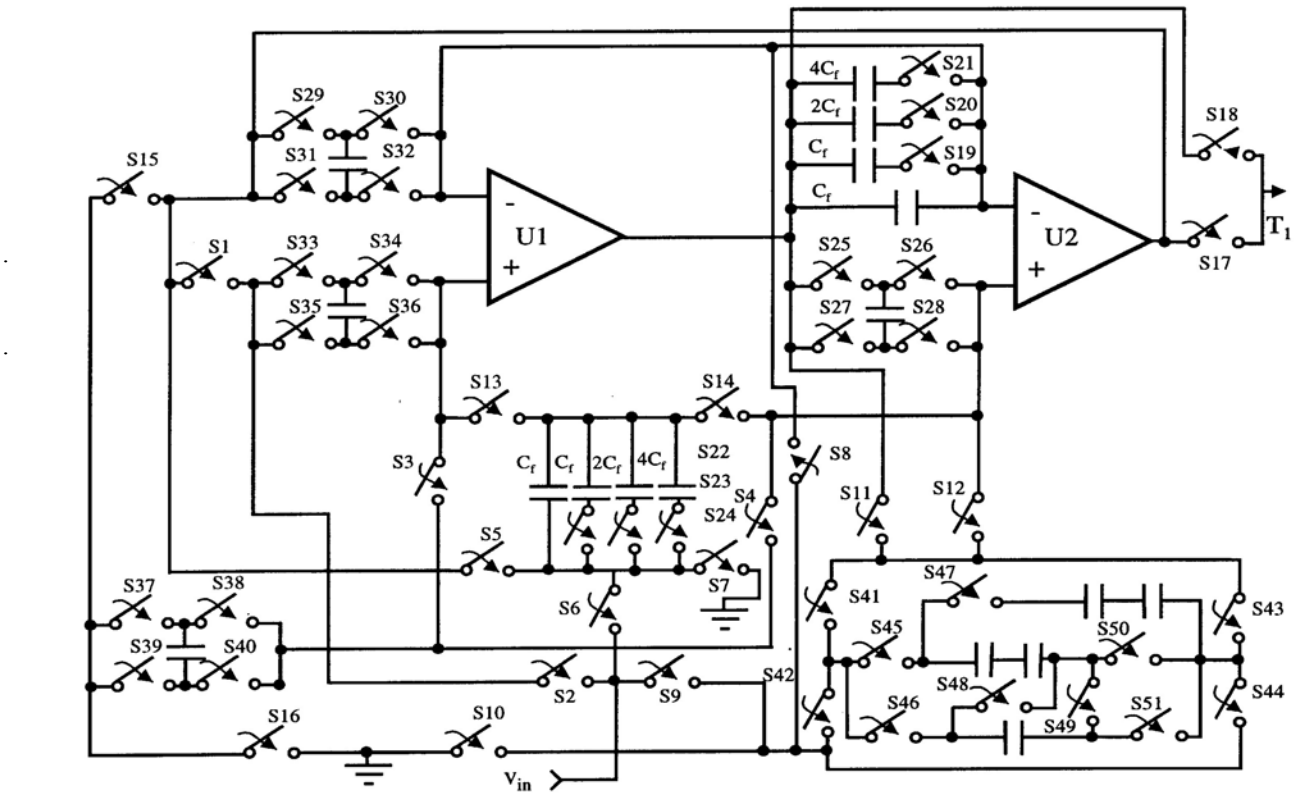

Fig 5. The Modified Switch-Capacitor Programmable GIC

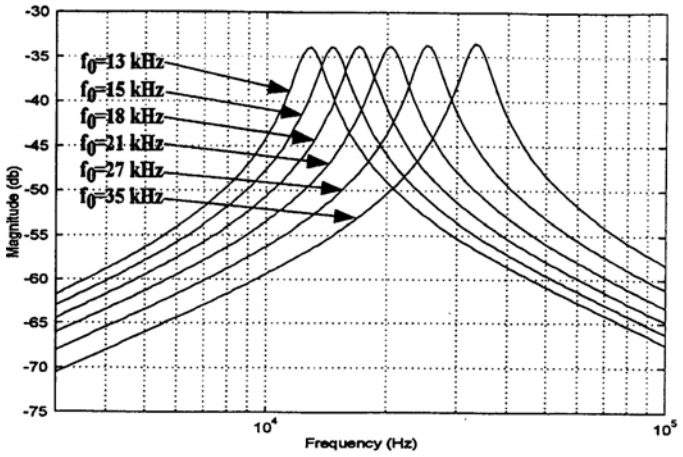

Fig. 6.a. The Band-Pass center frequency programmability.

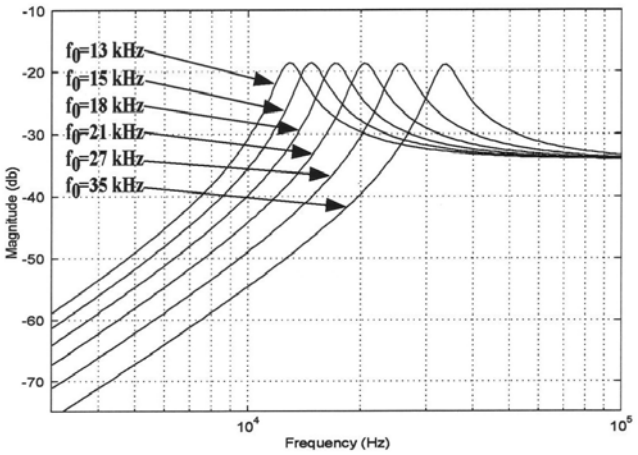

Fig. 6.b. High-Pass Responses for different corner frequencies

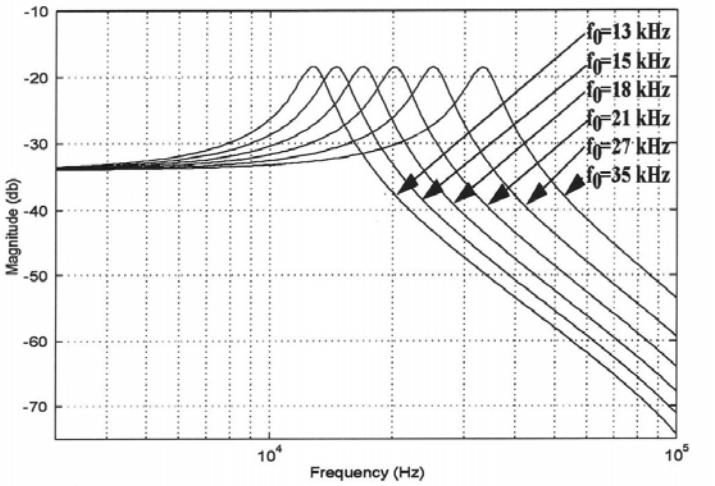

Fig. 6.c. The Low-Pass cutoff frequency programmability.

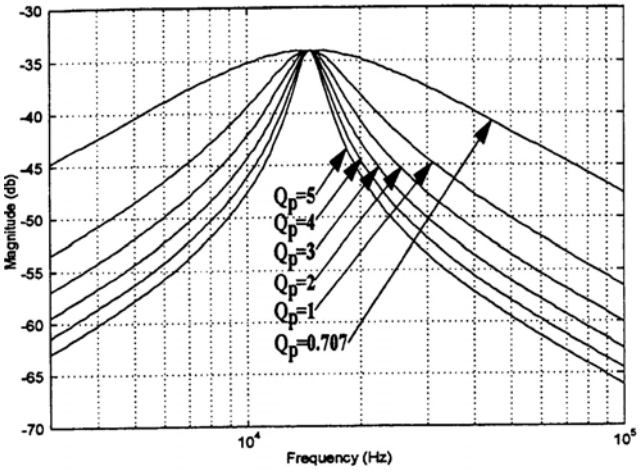

Fig. 6.d. Effect of changing Q_p on the Band-Pass response.

Three identical sections of this Biquadratic Programmable GIC filter were implemented on a CMOS VLSI chip using the MOSIS 2-microns Process. Such layout provided the user with the capability of cascading up to three biquad filter sections to form a 6th order programmable filter. This task can be easily done through external pin-out connections. Fig. 7 illustrates the floor plan of this three-stage Biquad filter design. While VLSI chip layout is depicted in Fig 8. Detailed transfer function and theoretical sensitivity derivations demonstrating the attractive features of this design along with experimental results will be reported in a future full paper.

2 Conclusions:

A CMOS custom integrated circuit featuring a multi-stage SC filter is presented. The Chip was manufactured using MOSIS 2-microns process. The 40 pin prototype chip included three programmable biquadratic sections. Each section is a universal SC analog filter that can be digitally selected to perform a low-pass, high-pass, band pass or notch filtering function. Each section can be independently digitally controlled for center frequency and quality factor selection. The result is very versatile analog building block that can be of great use in many applications.

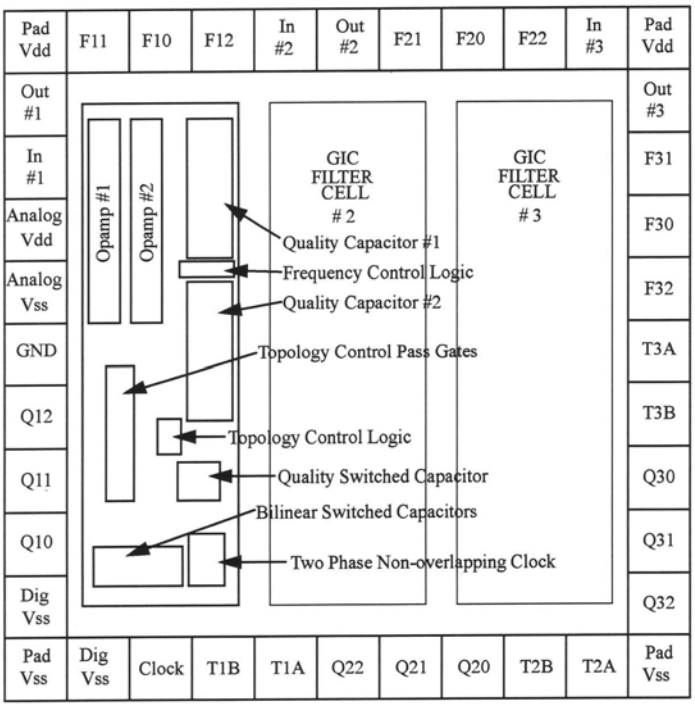

Fig. 7. Floor Plan of the 3 Stage Programmable GIC Filter.

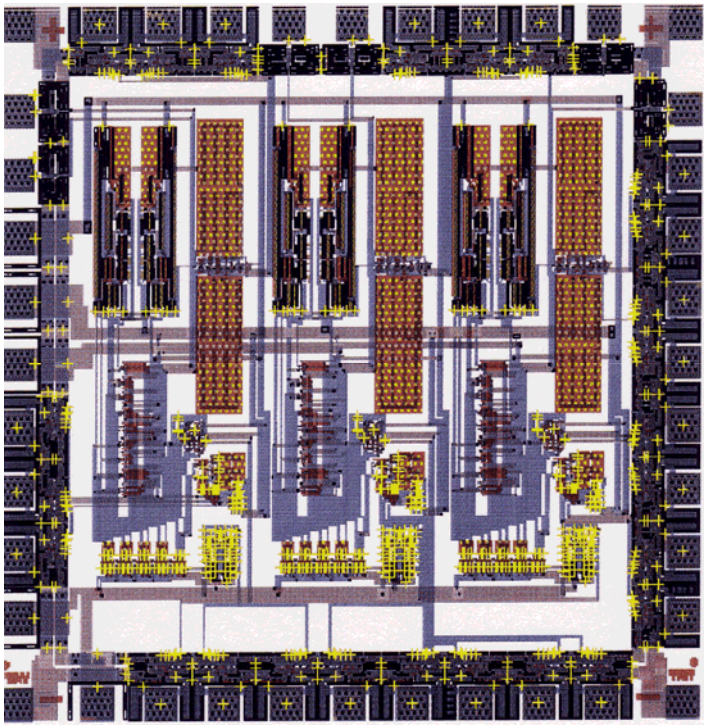

Fig. 8. The VLSI Layout of the Programmable GIC Filter.

References:

[1] R.W. Brodersen, P.R. Gray, and D.A. Hodges, "MOS Switched Capacitor Filters", IEEE Proceedings VOL 67, No 1 pp 61-75, Jan. 1979.

[2] G.C. Temes, H.J. Orchard, and M. Johanbegloo, "Switched-Capacitor Filter Design Using the Bilinear Z-Transform", IEEE transactions on Circuits and Systems, VOL CAS-25, pp 1039-1044,dec. 1986.

[3] D.J. Allstot, R.W. Brodersen, P.R. Gray, "An Electronically Programmable Switched-Capacitor Filter", IEEE Journal of Solid State Circuits, VOL SC-14, No. 6, pp 1034-1041, Dec. 1979.

[4] S. Michael & P. Andresakis, "Digitally Controlled Programmable Active Filters", Proceedings of the 19th Asilomar Conference on Circuits and Systems, Pacific Grove, CA, Nov.1985 pp 18-22.

[5] B.B. Bhattacharyya, W.B. Mikhael, and A. Antoniou, "Design of RC-Active Networks By Using Generalized Immittance Converters", Proceedings of the 19th International Symposium on Circuit Theory pp 290-293, April 1973.

[6] W. B. Mikhael and S. Michael, l"Composite Operational Amplifiers: Generation and Finite-Gain Applications," IEEE Transactions on Circuits and Systems, Vol. CAS-34, No. 5, pp. 449-460, May 1987.

[7] S. Michael and W. B. Mikhael, "Inverting Integrator and Active Filter Applications of Composite Operational Amplifiers," IEEE Transactions on Circuits and Systems, Vol. CAS-34, No. 5, pp. 461-470, May 1987.

[8] S. Michael, " The results of the VLSI Implementation of High Performance Switched Capacitor Analog Building Blocks.", Proceedings of the 38th Midwest Symposium on Circuits and Systems, Rio de Janeiro, Brazil, August, 1995.