A Novel Higly Accurate Current Mirror

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Abstract: A novel current mirror that can work in weak and strong inversion is proposed. The mirror is capable of copying current down to nano-ampere range. The proposed scheme eliminates the DC matching error caused by the difference between drain-to-source voltages of both input and output transistors. The proposed configuration was verified using ORCAD simulator in 0.8μm CMOS process technology. Simulation results confirm the functionality and accuracy of the approach.

Key words: -Current mirror, DC matching error, Analog blocks, Mismatch, weak inversion, novel mirror

1 INTRODUCTION

Current mirrors are core structure for almost all analog and mixed mode circuits and the performance of analog structures largely depends on their characteristics. CMs are used to perform identity operations, current amplification, biasing and loading elements. Analog-to-Digital and Digital-to-Analog converters are additional circuits that use current mirrors [1,2]. In many applications, the performance of the simple current mirror is inadequate, because of a systematic gain error and low output resistance. It is well known that current mirrors suffer from transistor mismatch and DC matching errors. In the past two decade, a series of high performance current mirrors in MOS technology has been reported [1, 2, 3]. The CMs available in the literature [2] are based on one or combination of the following design techniques.

1. Triode region CMs
2. Sub-threshold region CMs
3. Bulk-driven MOSFETs based CMs
4. Level shifter based CMs
5. Self cascode MOSFET based CMs
6. Floating gate MOSFET based CMs

Low power current mirrors using low supply voltages are attractive for all designers. Two widely used current mirrors with both low systematic gain errors and high output resistance are the stacked cascode mirror [4] and the improved Wilson current mirror [5, 6]. DC matching error is always present in these designs but its percentage varies form one approach to another. Its presence causes deterioration in the performance of the A/D converters [7, 8]. The Cascode current mirror reported in [9] is a good solution but consumes substantially voltage headroom. A novel current mirror for portable application was presented in [12]. The drawback of this mirror is the range of the input current is 1uA to 500uA. In this paper, a new design for a novel current mirror that can copy current in nano-ampere range and eliminate the DC matching error is presented. The proposed CM can be used for all modes of operations, sub-threshold, triode and saturation.

2 PROPOSED STRUCTURE

CMs can be designed to operate either in triode region, or in sub-threshold region or in saturation region. However, it may be noted that most of the CMs have been designed to operate in saturation region only. This is because the designing of the CMs based on saturated MOSFETs is simpler and the resultant structure is suitable for high frequency applications. Thus the requirements for the CMs are;

- For CMs built using MOSFETs operating in triode region, it is mandatory to ensure $V_{ds1}=V_{ds2}$ in addition to $V_{gs1}=V_{gs2}$
- CMs built using saturated MOSFETs require $V_{gs1}= V_{gs2}$. However, if V_{dsl} equals V_{ds2} then the short channel effect can be eliminated.
- The requirements of the CMs operating in sub-threshold regions are the same as the CMs with saturated MOSFETs implying $V_{gsl}=V_{gs2}$ However, sub-threshold MOSFETs require large W/L and low input current.

Fig 1 shows the proposed current mirror. It consists of two transistors M_1 and M_2 that represent the mirror cell and a second generation

current –controlled current conveyor to keep $V_{DS2} = V_{DS1}$. The CCCII characteristic can be modeled as

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

From equation 1, $v_y = v_x + i_x r_x$

With reference to figure 1, the Conveyer Z terminal is connected to the gates of M1 and M2. This will ensure that $i_z = 0$ As a consequence $i_x = 0$ and hence $v_y = v_x$ which means the drain-to-source voltages of M1 and M2 are equal.

Moreover, the voltage Vz can be used to control the biasing mod of M1 and M2.

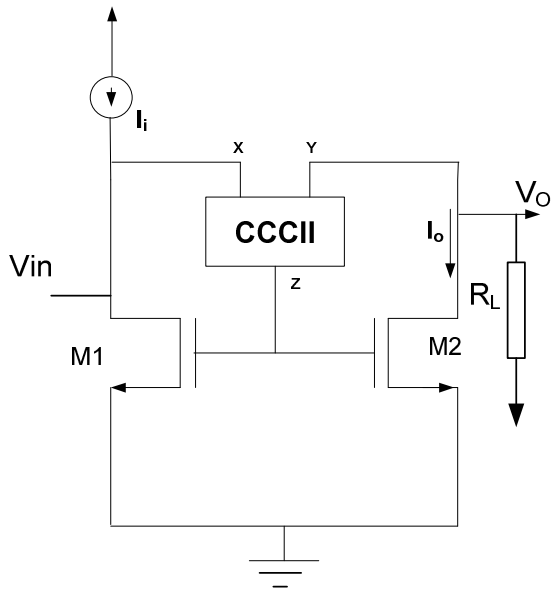

Fig1. Proposed new current mirror circuit

The current conveyor is implemented using the basic structures presented in [10] and is shown in Fig 2.

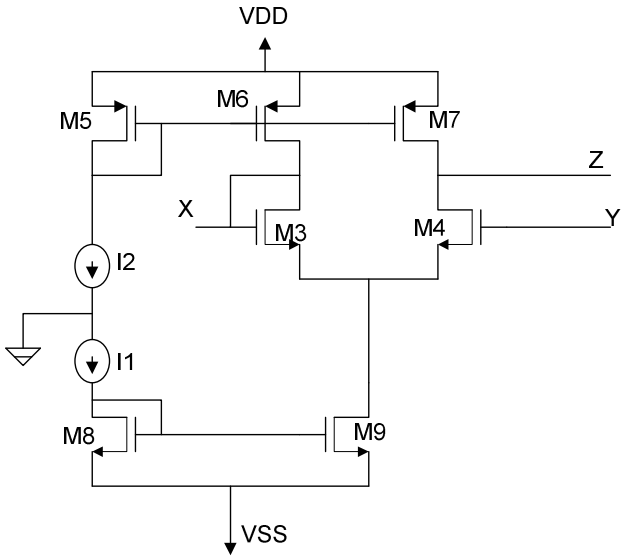

Fig2. Complete current conveyor circuit diagram

Figure 3 illustrates the complete circuit diagram of the proposed scheme. Here M1 and M2 are the mirror transistors, M3-M9 are the conveyor transistors. R_L is the load resistance. If the input current Is in nano-ampere range, RL can be large up to 200k. the load resistance will be less as the input current goes up. This is because the voltage across R_L will effect the biasing of the transistor M_4 and can drive it to cut off.

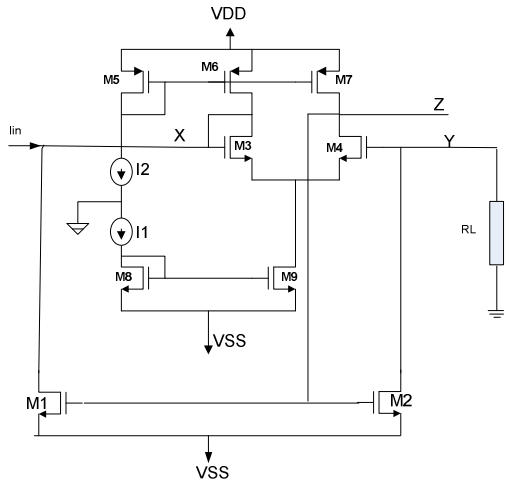

Figure 3. Proposed Current mirror

Simulation results: The proposed current mirror was simulated using ORCAD simulator in 0.8µm CMOS process. The input current was varied from 0 to 200 nA with load resistance RL=100k > plot of the input current versus the output current is

shown in Figure 4. It is clear from the plot the maximum error is around 2%

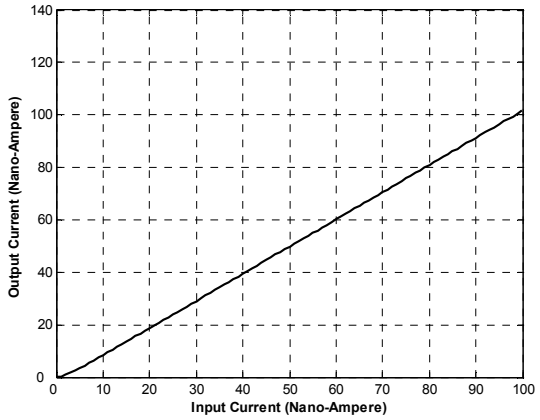

Figure4. Plot of the output current Vs the input current

If the current is increased, RL must be decrease because the output resistance of the mirror will decrease. Simulation of the mirror for microampere current range is shown in figure 5. Here the error decreases to around 0.1%.

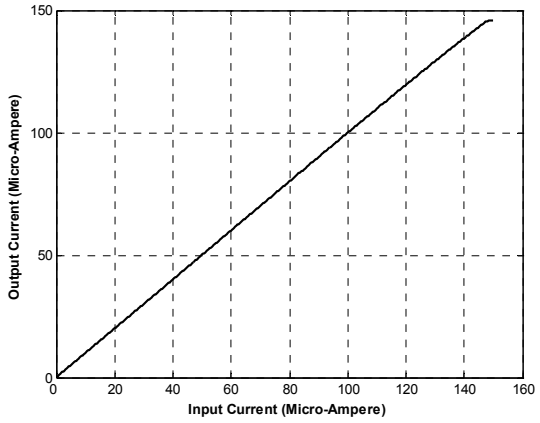

Figure 5. The output current Vs the input current for microampere range.

It is evident from the plot the output current is the exact replica of the input current.

3 CONCLUSION

Using two MOS transistors and one second-generation current-conveyer a current mirror with negligible DC-matching error has been developed developed. The proposed mirror can copy current down to nano ampere range with high accuracy. The proposed configuration was verified by simulation using industry standard parameters in ORCAD simulator level 49.

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