An InGaAs/GaAs Superlattice-Base Heterostructure-Emitter Bipolar Transistor (SB-HEBT)

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Abstract: - A novel InGaAs/GaAs superlattice-base heterostructure-emitter bipolar transistor (SB-HEBT) with structure is proposed and demonstrated by two-dimensional analysis. As compared to the traditional HEBT, the studied superlattice-base device exhibits a higher collector current, a higher current gain of 246 and a lower base-emitter (B-E) turn-on voltage of 16 mV attributed to the increased charge storage of minority carriers in the InGaAs/GaAs superlattice-base region by tunneling behavior. The low turn-on voltage can reduce the operating voltage and collector-emitter offset voltage for low power consumption in circuit applications.

Key-Words: superlattice-base, heterostructure-emitter, bipolar transistor, current gain, turn-on voltage, tunneling, offset voltage

1 Introduction

Heterojunction bipolar transistors (HBTs) have emerged to be one of the promising high-speed devices because of their expected potential based on a high current gain, a high current-handing capability, and an extremely high frequency performance [1]. Typically, a relatively large base-emitter (B-E) turn-on voltage severely limits the minimum operated voltage and causes a large collector-emitter offset voltage (ΔV_{CE}), which increases the power consumption in circuit applications [2].

Over the past years, some approaches have been used to reduce the B-E turn-on voltage. One approach is to adopt a small energy-gap n-type emitter layer between confinement and base layers for eliminating the spike barrier blocking the electron injection from the emitter to the base [3-5]. Nevertheless, if the small energy-gap emitter layer is too thick, the transistor will perform with inferior confinement effect. Then, the charge storage in neutral-emitter region enhances the base recombination current and increases the total base current [5]. On the other hand, if a thinner as well as small energy-gap emitter layer is employed, the device will serve as conventional HBTs and the turn-on is still considerably large. Another approach is to use a low energy-gap material as base layer [6-9]. Though InGaAs and GaAsSb ternary alloys have lower energy gap to control and improve the turn-on voltage, they introduces compressive strain and the layer thickness is critical due to a lattice mismatch with GaAs material. For the strain relation effects, the InGaAs quantum-well-based heterojunction as phototransistor has already been reported [10]. Furthermore, the use of the $In_xGa_{1-x}As_{1-y}N_y$ as base layer was well demonstrated to further reduce the energy gap of base and it effectively improved the problem associated with excess strain [8]. However, the blocking effect of collector current at base-collector heterojunction could introduce a large knee voltage reducing the collector current.

In this article, a new InGaAs/GaAs superlattice-base heterostructure-emitter bipolar transistor (SB-HEBT) with structure is first reported and demonstrated. The addition of a thinner as well as small energy-gap emitter layer eliminates the potential spike at B-E junction, and the average energy gap in the base region is decreased by the use of the superlattice-base structure. As compared to the traditional HEBT, the minority charge storage in the superlattice-base region is enhanced and the collector current is substantially increased.

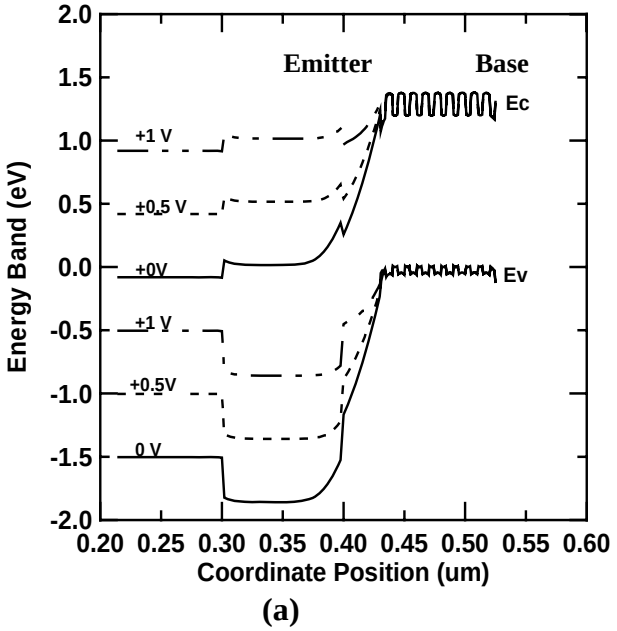
2 Device Structures

The device structure of the superlattice-base device (labeled device A) includes a 0.5 μm $n^+ = 1 \times 10^{19}$ cm^{-3} GaAs subcollector layer, a 0.5 μm $n^- = 5 \times$

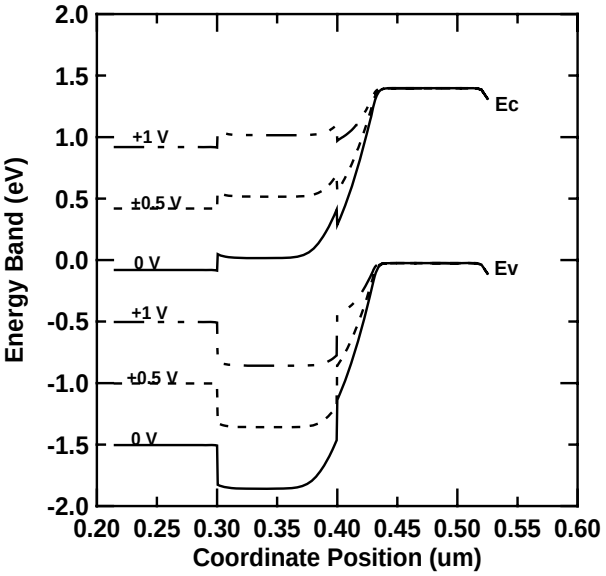
10^{16} cm^{-3} GaAs collector layer, a $p^+ = 5 \times 10^{18}$ cm^{-3} InGaAs/GaAs superlattice base, a 300 Å $n = 5 \times 10^{17}$ cm^{-3} GaAs emitter layer, a 0.1 μm $n = 5 \times 10^{17}$ cm^{-3} $In_{0.49}Ga_{0.51}P$ confinement layer, and a 0.3 μm $n^+ = 1 \times 10^{19}$ cm^{-3} GaAs cap layer. The superlattice base consists of ten-period 50 Å $In_{0.2}Ga_{0.8}As$ layers and nine-period 50 Å GaAs layers. For comparison, the conventional InGaP/GaAs HEBT (labeled device B), has a structure similar to the device A except that a 950 Å $p^+ = 5 \times 10^{18}$ cm^{-3} GaAs bulk base layer is employed to replace the superlattice base. A two-dimensional (2D) semiconductor simulation package SILVACO was used to analyze the energy band, distributions of electrons and holes, and dc performances of the two devices [11]. The two-dimensional analysis takes into account the Poisson equation, continuity equation of electrons and holes, Shockley-Read-Hall (SRH) recombination, Auger recombination, and Boltzmann statistics, simultaneously. The emitter and collector areas are 50 × 50 and 100 × 100 μm^2, respectively.

3 Results and Discussion

The energy band diagrams near the B-E junction for the devices A and B are illustrated in Figs. 1(a) and 1(b), respectively. Obviously, the potential spikes at B-E junction of both devices are completely eliminated, even at $V_{EB} = 1.0$ V. The employments of a thin n-GaAs emitter layer between confinement and base layers enable the pn junction to act as a homojunction, and it helps to lower the energy band at emitter side for eliminating the potential spike.



(a)

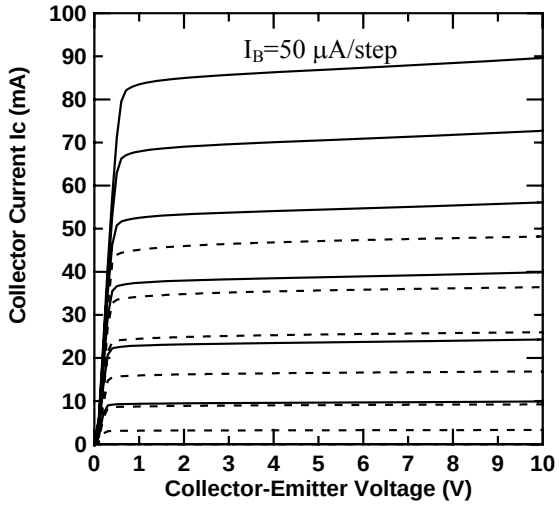


(b)

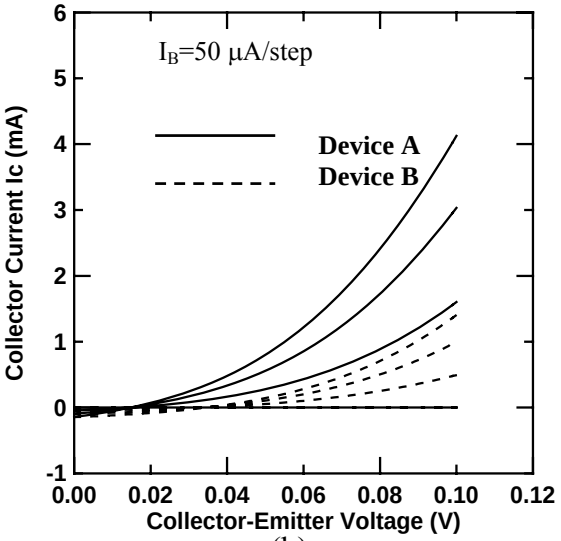
Fig. 1. Energy band diagrams near the base-emitter junction of (a) device A and (b) device B. The devices A and B represent the heterostructure-emitter bipolar transistors with and without the superlattice-base structures, respectively.

Figure 2 shows the simulated common-emitter current-voltage (I-V) characteristics of the two devices at room temperature. Clearly, the device A exhibits a higher collector current and a larger current gain than the device B. An enlarged view near the origin of the I-V characteristics is depicted in Fig. 2(b). As seen in the figure, a relatively lower offset voltage of 16 mV at $I_B = 50$ μA is observed for the device A, while the device B shows a larger value of about 40 mV. Figure 3 depicts the calculated Gummel plots of the two devices at $V_{BC} = 0$ V. The E-B turn-on voltage of the device A is 0.966 V at the current level of 1 μA, which is 40 mV lower than the 1.006 V in the traditional HEBT. The low E-B turn-on voltage can reduce the operating voltage and collector-emitter offset voltage for substantially decreasing the power consumption in circuit applications. The current gains are 246 and 70 at $V_{BE} = 1.25$ V for the device A and B, respectively. In both devices, the ideality factor n_c for collector current is nearly equal to unity at low current levels. This means that the thermionic emission and diffusion mechanisms dominate the electron transportation across the E-B junction. On the other hand, the ideality factors for base current n_b of 1.9 at low current levels are near the same, which means that the employment of InGaAs/GaAs superlattice base does not increase the base recombination current and degrade the device performance.

In order to investigate the device mechanism, the charge distributions near the B-E junction at equilibrium and under forward bias are simulated in Figs. 4(a) and 4(b), respectively. Because of the considerable valence-band energy difference (ΔEv) at InGaAs/GaAs heterojunction, part of holes in p^+-GaAs barriers are trend to transfer into the p^+-InGaAs wells in the superlattice-base region and the efficient holes concentration in the wells is higher than the barriers for the device A, as seen in Fig. 4(a). Similarly, the electrons in the wells have heavier concentration than the barriers. Under forward B-E bias, the minority carrier storage in the base region of the device A is further increased than the device B as depicted in Fig. 4(b). The phenomenon is due to the electron tunneling through the suplerlattice base incorporating the thermal diffusion. The more carrier storage in the base substantially causes the collector current to increase and the B-E turn-on voltage to decrease. On the other hand, attributed to the use of GaAs/InGaAs superlattice base in the device A, the effective valence band discontinuity (ΔEv) at the base-emitter junction (n-InGaP/n-GaAs/p^+-InGaAs) is equivalent approximately the sum of the valence band discontinuities at the InGaP/GaAs and InGaAs/GaAs heterojunctions. Substantially, the confinement effect for holes and the emitter injection efficiency could be enhanced, as compared to the conventional InGaP/GaAs HEBT. Nevertheless, at relatively large B-E forward bias the large amounts of electron storage in the superlattice base region will result in large base bulk recombination and base current as seen in Figs. 3 and 4(b), Though the device A has a slightly high base current, the large ratio of collector to base currents is still achieved.



(a)



(b)

Fig. 2. (a) Simulated common-emitter current-voltage characteristics at room temperature of devices A (solid line) and B (dashed line). (b) Enlarged view near the origin of the current-voltage characteristics.

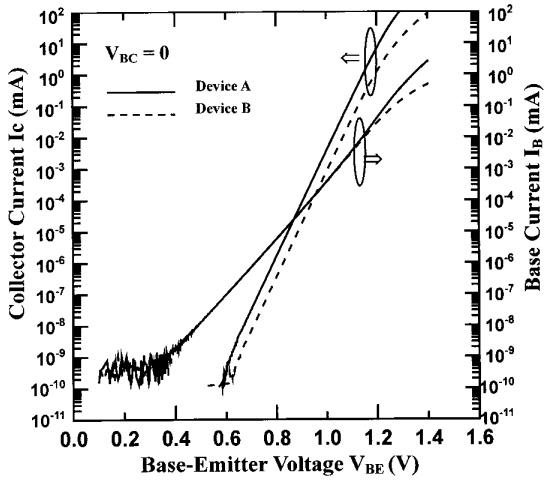


Fig. 3. Calculated Gummel plots of devices A and B at V_{BC} = 0 V.

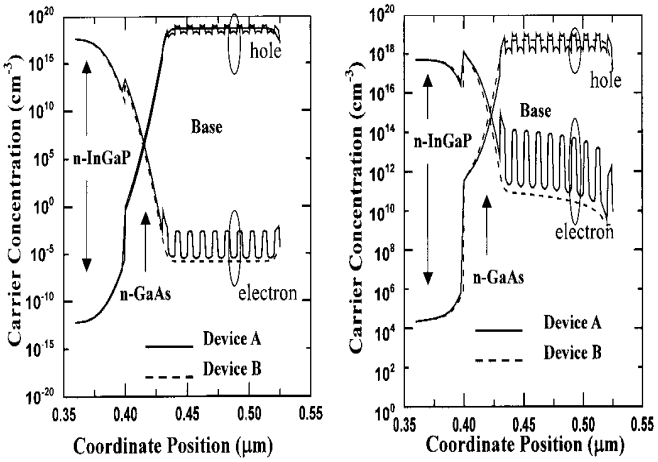


Fig. 4. Charge distributions near the base-emitter junction (a) at equilibrium and (b) under forward bias.

4 Conclusion

In conclusion, a newly designed InGaP/GaAs HEBT with InGaAs/GaAs superlattice-base structure is investigated by two-dimensional analysis. As compared to the traditional HEBT, the proposed device exhibits a higher collector current, a higher current gain, and lower turn-on voltage, simultaneously, because of the increase of minority carrier's storage in the InGaAs/GaAs superlattice base by tunneling behavior at B-E forward bias. Consequently, the proposed device provides good potential for digital and analog circuit applications.

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