InGaP/InGaAs Complementary Pseudomorphic Doped-Channel HFETs

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Abstract: - The device and inverter characteristics based on InGaP/InGaAs n- and p-channel complementary pseudomorphic doped-channel HFETs are demonstrated. Particularly, the saturation voltage of the n-channel device is substantially reduced because the two-dimensional electron gas (2DEG) is formed and modulated in the InGaAs strain channel. Experimentally, an extrinsic transconductance of 109 (11.5) mS/mm and a saturation current density of 32.5 (-27) mA/mm are obtained for the n-channel (p-channel) device. Furthermore, the noise margins NM_H and NM_L values are up to 1.317 and 0.28 V, respectively, at a supply voltage of 2.0 V for complementary logic inverter application.

Key-Words: InGaP/InGaAs, complementary, doped-channel, HFETs, transconductance, saturation current, noise margin

1 Introduction

The vertical monolithic integration of the heterostructure field-effect transistors (HFETs) by the continuous growth of successive layers permits the different devices to be optimized separated on the same wafer, which provides the reduction of fabrication complexity [1-4]. Among of the integrated devices, the co-integration of n- and p-channel HFETs has attracted considerable attention for extremely low power dissipation associated with complementary logic circuit applications [1, 2]. With respect to the identical transistor performances, high output current and linearity are especially essential for signal amplification in circuit applications. In general, due to the relatively high transconductance high electron mobility transistors (HEMTs) are the main members of the complementary-HFETs family, however, they suffered from poor device linearity and were not suitable for linear amplifier applications [5, 6]. On the other hand, doped-channel field-effect transistors (DCFETs) could achieve high output currents and good device linearity, nevertheless, the channel concentrations were fixed and the drain-to-source (D-S) saturation voltages were relatively large [7, 8]. Significantly, the noise margins of the inverters are severely limited by the considerable saturation voltages. In other words, DCFETs could be promise for linear amplifier applications, while they are not good fit for inverter applications.

In this work, high-performance InGaP/InGaAs n- and p-channel complementary pseudomorphic DCFETs on the same chip are first fabricated and demonstrated. The saturation voltage of the n-channel device is substantially improved and the large noise margins of the complementary logic inverter are achieved.

2 Experiments

The device structures were grown on an (100) oriented semi-insulating GaAs substrate by low-pressure metal-organic chemical-vapor deposition system (LP-MOCVD). The epitaxial structures consisted of a 0.5 μm undoped GaAs buffer layer, a 100 Å ($p^+ = 5 \times 10^{17}$ cm^{-3}) $In_{0.2}Ga_{0.8}As$ p-channel layer, a 200 Å undoped $In_{0.49}Ga_{0.51}P$ layer, a 200 Å undoped GaAs layer, a 200 Å undoped $In_{0.49}Ga_{0.51}P$ layer, a 100 Å ($n^+ = 7 \times 10^{17}$ cm^{-3}) $In_{0.2}Ga_{0.8}As$ n -channel layer, a 200 Å ($n^- = 5 \times 10^{16}$ cm^{-3}) $In_{0.49}Ga_{0.51}P$ layer, and a 300 Å ($n^+ = 4 \times 10^{19}$ cm^{-3}) GaAs cap layer. A mesa structure provided the required isolation to distinguish the n- and p-channel regimes. After covering the n-channel regime and removing the n^+-GaAs cap, 200 Å n^--$In_{0.49}Ga_{0.51}P$, 100Å n^+-$In_{0.2}Ga_{0.8}As$, and 200Å i-$In_{0.49}Ga_{0.51}P$ layers

in the p-channel regime by selectively etching. The electron and hole mobility of 3840 and 450 $cm^2/V{\cdot}s$ at 300 K from Hall measurements are obtained for the n- and p-channel devices, respectively. Drain and source ohmic contacts were obtained by alloying evaporated AuGeNi metal at 400 ^0C for 30 sec. Sequentially, the n^+-GaAs cap of the n-channel device and the 200Å i-GaAs layer of the p-channel device are recessed, and then the gate metal Au was simultaneously deposited on the $In_{0.49}Ga_{0.51}P$ layers of both the integrated devices. The schematic cross section of the integrated devices is shown in Fig. 1. The gate dimension and the D-S spacing were 1 × 70 μm^2 and 3 μm, respectively.

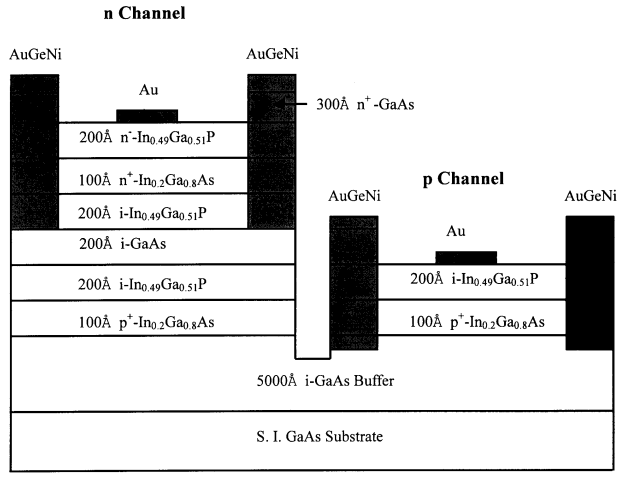

Fig. 1. Schematic cross section of the integrated n- and p-channel InGaP/InGaAs complementary pseudomorphic doped-channel HFETs with a gate dimension of 1 × 70 μm^2.

3 Results and Discussion

Figure 2(a) and 2(b) illustrates the corresponding band diagrams of the n- and p-channel devices at equilibrium, respectively. With respect to the n-channel device, the device acts as enhancement-mode transistor because the doping level of the n^+-InGaAs channel layer is not so heavy and the channel is entirely depleted at equilibrium. Another, due to the considerable conduction band discontinuity (ΔEc ~ 0.38 eV) at $In_{0.49}Ga_{0.51}P/In_{0.2}Ga_{0.8}As$ heterojunction [8], it provides a large potential barrier preventing the injection of electrons from channel into the gate electrode and increases the forward gate bias. Furthermore, it forms subband and two-dimensional electron gas (2DEG) in the n^+-InGaAs strain channel [7], which could efficiently increase the channel concentration. Similarly, the lower channel doping enable the p-channel device to behavior as enhancement-mode transistor when compared to the traditional DCFET. The gate potential barrier for holes is also large by the large valence band discontinuity (ΔEv) at $In_{0.49}Ga_{0.51}P/In_{0.2}Ga_{0.8}As$ heterojunction.

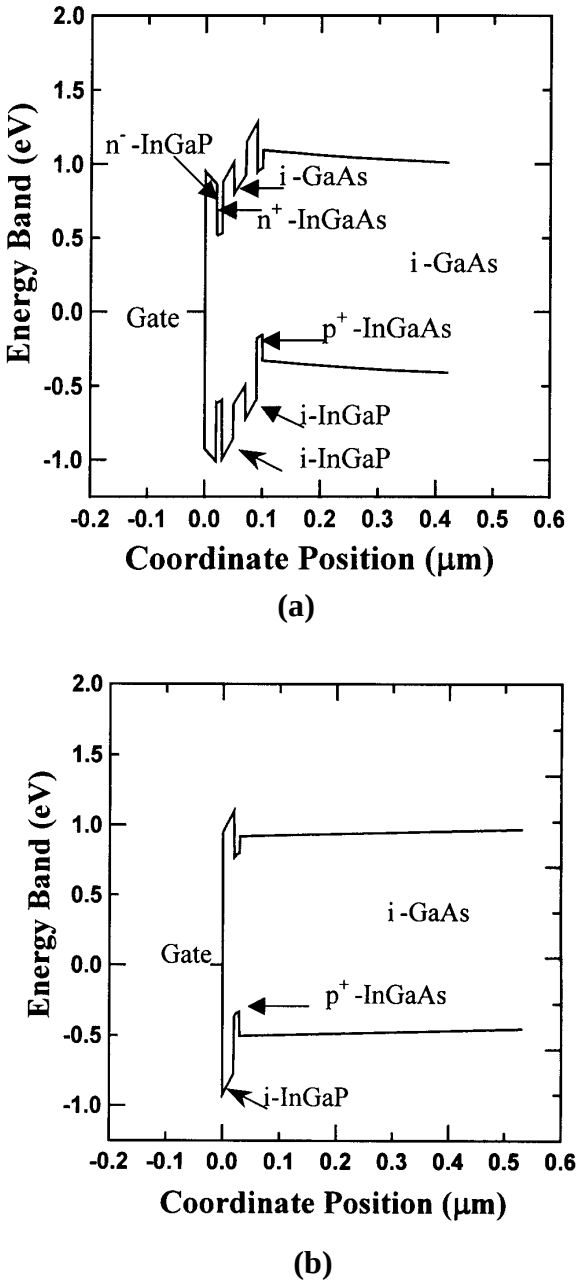

Fig. 2. Corresponding band diagrams of the (a) n-channel and (b) p-channel HFETs at equilibrium.

The experimental D-S current-voltage characteristics of the n- and p-channel devices are depicted in Fig. 3(a) and 3(b), respectively. In the n-channel device, the saturation voltage is less than the previously reported DCFET [7]. When the

positive gate voltage is biased, the Schottky depletion region under gate metal shrinks and most of carriers in the 2DEG may be increased and modulated. This will substantially reduce the channel resistance and the drain current in the linear region rapidly increases with the increase of the forward gate bias.

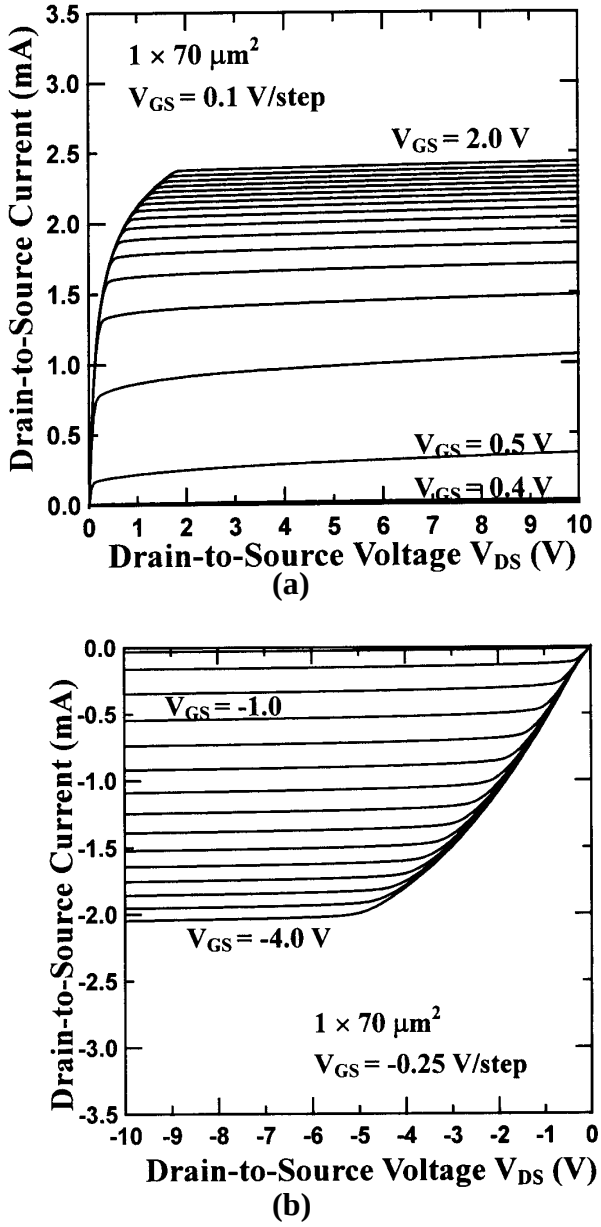

Fig. 3. Experimental drain-to-source current-voltage characteristics of the (a) n-channel and (b) p-channel devices.

For the complementary logic inverter application, the low saturation voltage of the n-channel transistor could reduce the V_{OL} and V_{IH} values, and substantially increases the noise margins. Based on the studied integrated pseudomorphic DCFETs, the voltage transfer characteristic of the complementary logic inverter is illustrated in Fig. 4. At the supply voltage of 2.0V, the V_{IH}, V_{IL}, V_{OH}, and V_{OL} values are 0.66, 0.4, 1.977, and 0.12 V, respectively, as defining output voltage to input voltage with a –1 slope. According to the above voltages, large noise margins NM_H and NM_L of 1.317 and 0.28 V are obtained.

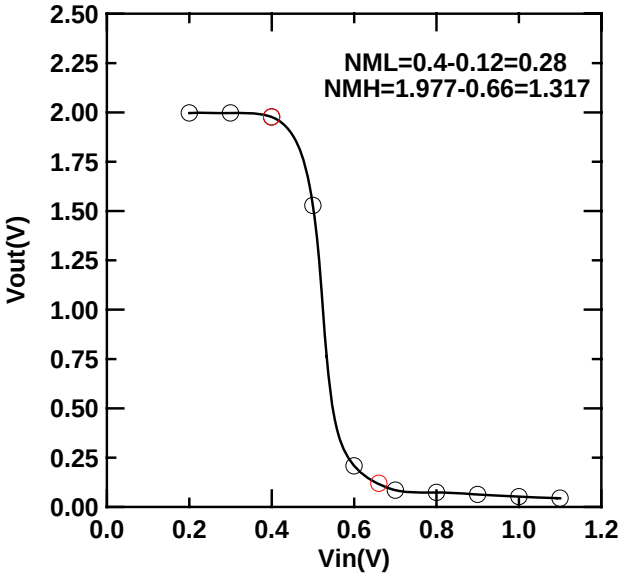

Fig. 4. The voltage transfer characteristic of the complementary logic inverter at supply voltage of 2.0V.

4 Conclusion

In conclusion, the integration of InGaP/InGaAs n- and p-channel complementary pseudomorphic DCFETs have been successfully fabricated and investigated. The integrated devices exhibit good transistor performances and large noise margins in inverter logic by the reduction of the channel resistance in the linear region with the increase of the forward gate bias. The devices employing the pseudomorphic doping-channel structures provide good promise for the reduction of fabrication complexity and practical circuit applications.

Acknowledgment

This work was supported by the National Science Council of the Republic of China under Contract No. NSC 96-2221-E-017-012.

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