An Auto Calibrator for TIQ Based Flash ADC Designs

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Abstract: - This paper presents a calibrator circuit to minimize mainly the process parameter variations related problems of TIQ Based Flash ADC designs. The simulations are carried out using 0.35µ CMOS technology in two directions; to correct the input analog range deviations, and to catch the possible missing codes due to process parameter and temperature variations. The designed TIQ based flash ADC core under calibration is 5b with the performance of 2Gs/s, and has a low power supply of 3.3V. However, the calibrator has power supply of 5V.
Key-Words: - TIQ, Auto Calibration, CMOS, Flash ADC

1 Introduction

The Threshold Inverter Quantization (TIQ) Technique has been advertised in the literature for an alternative approach to traditional analog part of the CMOS Flash ADC designs [1], [2], [3], [4], [5], [6], [7]. This technique does not use any resistor or capacitor array. In addition, it uses less chip area and no DC power consumption. TIQ approach is basically depends on the proper sizing of the transistors in a cascaded two identical CMOS inverters. The large signal behaviour of a CMOS inverter must be investigated to understand the TIQ technique. The examination of Fig. 1 at the Vin = Vout point can give a brief idea about the TIQ approach [1], [7].

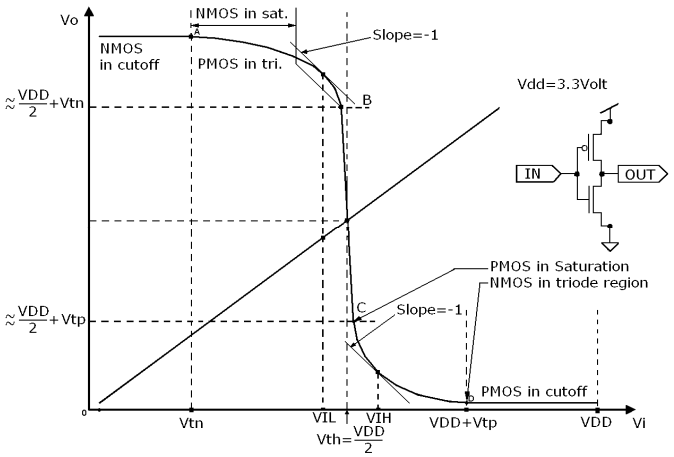

Fig. 1. Voltage transfer curve of a CMOS Inverter

The mathematical expression of the threshold point of any quantizer sub-unit can be derived approximately as [7]:

$$Vth = \frac{r\left(V_{DD} - |Vtp|\right) + Vtn}{1 + r}, \qquad (1)$$

$$\text{where} \quad r = \left(\frac{\left(k'_p \frac{W}{L} \right)_p}{\left(k'_n \frac{W}{L} \right)_n} \right)^{1/2} \qquad (2)$$

This expression shows the nonlinear relationship between threshold value of a CMOS inverter and transistor aspect ratios in a CMOS inverter. In fact, by using the higher level SPICE models (such as BSIM3 Level 49) and a powerful simulation tool, the specific threshold voltage values of the any specific TIQ comparator cells are obtained more accurately. Fig. 2 shows the block diagram of the complete TIQ based analog part, in which a specific quantizer is magnified.

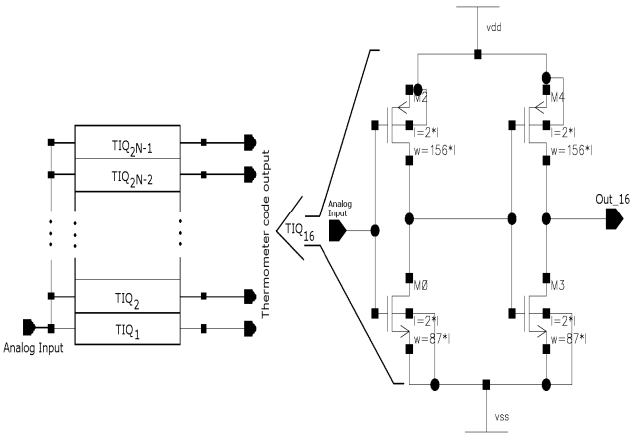

Fig. 2. TIQ Based analog quantizer magnifying TIQ cell_16

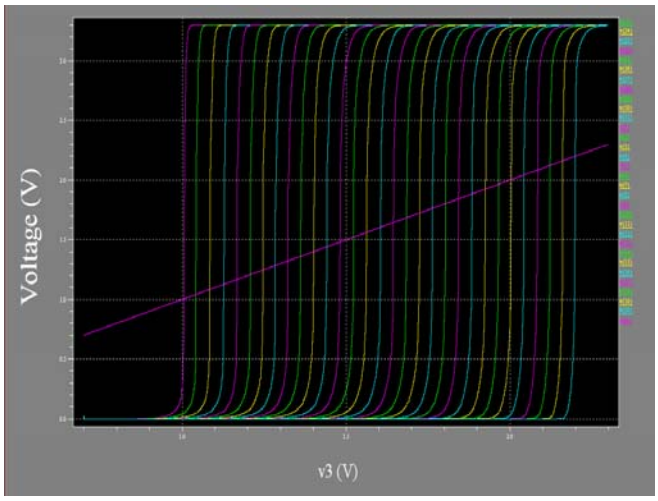

Fig. 3. The DC simulation result of the TIQ quantizer block (i.e. the thermometer code output)

Fig. 3 shows the thermometer code outputs, in which highly linear quantization process are observed. This technique, no doubt, yields the fastest voltage comparison operation especially for low resolution flash structures when compared to any kind of traditional comparator structures (such as auto-zero type, clocked type, or differential amplifier based comparators) in the literature except for the following disadvantages [1]:

- Single ended nature results in sensitivity to substrate noise coupling effects.
- Linearity measures and analog range of the converter are affected by process parameter variations.
- Bad power supply rejection ratio (PSRR) due to almost linear dependency to the power supply voltage (Vdd) results in requirement of a high quality Vref voltage source as can be visualized in (1).

However, the proposed circuit minimizes some of these effects listed above, and operates as a fast self-calibrator before ADC starts its conversion operation. The main idea of this circuit is to keep very high performance nature of the TIQ approach, but to sacrifice the other unique nature of it, which is less chip area, unfortunately.

2 The Auto Calibrator Circuit

The proposed auto calibrator circuit is shown in Fig. 4. This circuitry can be implemented as either on chip or off chip form; or even partially off chip. The principle of operation can be summarized as follows:

At the beginning, the *cal_ sel* push-button is tied to logic high, which connects the analog input side of the ADC to a pre-defined *dc_set* value, and also clock pulses to the counter. Several simulations were carried out to be able to catch the optimum dc set value. The best result was obtained in the middle of the analog input range of the ADC under calibration. Next, the 5-bit ring counter counts until the desired digital output code is reached.

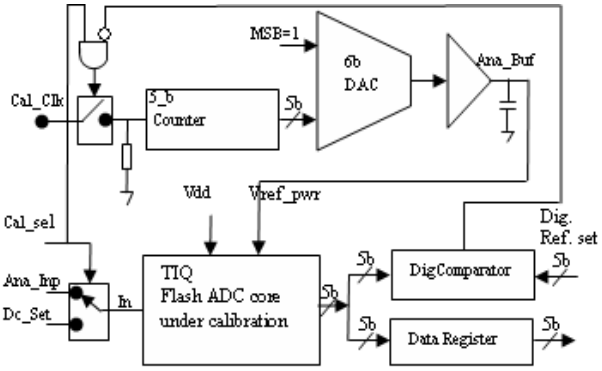

Fig. 4. The Auto Calibrator block diagram

The counter binary outputs drives a 6-b DAC with a DC offset. For this purpose, in fact, a special purpose 6-bit DAC, of which MSB bit is tied to logic high to eliminate the pre-selected useless range of Vref_pwr value (from 0 to 2.5V), was designed. As a result, a 5-bit digitally-controlled analog reference voltage source for the TIQ quantizer block only was implemented. Note that the power supply voltage of the digital part of ADC is not changed here. The output of the DAC, however, must be buffered to be able to used as a power supply voltage for the analog part of the ADC, which is the TIQ quantizer block. Fortunately, TIQ part consists of CMOS inverters only, and therefore it consumes power only on transition regions. It was investigated that a simple opamp based analog buffer output has small enough output resistance to be able to drive the Vref_pwr point together with a large off-chip decoupling capacitor. Fig. 5 shows how the selected buffer circuit follows to a randomly changed large signal input voltage swing. It can be seen that the buffer tracks exactly the input voltage swing especially for the critical voltage range of between 2.5 to 3.25 volts, in which the required new analog reference value will eventually be settled during the calibration cycle.

The digital comparator unit compares the ADC output code with the internally set desired binary reference code corresponding to the input dc_set value mentioned above. After the required Vref value is reached, the counter clock switch is closed by the A/B logic gate, which is also controlled by the digital comparator output. Now, the ADC is ready to operate. Therefore, the cal_sel button is released to switch the ADC input back to the analog input signal (i.e. normal conversion mode). This process is very fast

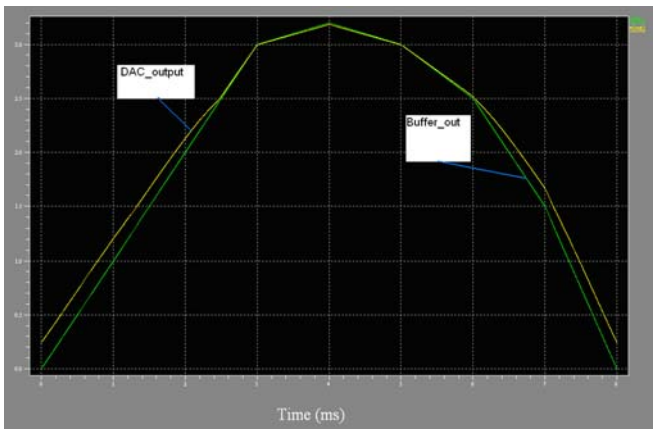

Fig. 5. Analog Buffer circuit tracking performance for large signal input swing

(may be in microseconds) and can not be recognized by the user. The output data is directly taken from the ADC outputs, and latched into an output register.

3 Simulation Results

Fig. 6 shows the simulation results of the calibrator. The counter clock signal, DAC output, buffer output, and DC_set value waveforms are plotted to be able to indicate the calibration process clearly. As can be seen in Fig. 6, the counting starts from the point where DAC out=2.5 volts and stops at 3.05Volts. Here, the original vendor specified simulation model parameter set (AMIS 0.35µ CMOS process typical model, SPICE Level-49 BSIM3) is changed from typical to slow one. The reference dc voltage was set to 1.6 volts as an example. Hence, although the original design value of Vref was 3.3 volts, the required new value of the Vref voltage due to process parameter change was reached at a different value, 3.05V. It can be observed from Fig. 7 that all binary codes are obtained without any loss.

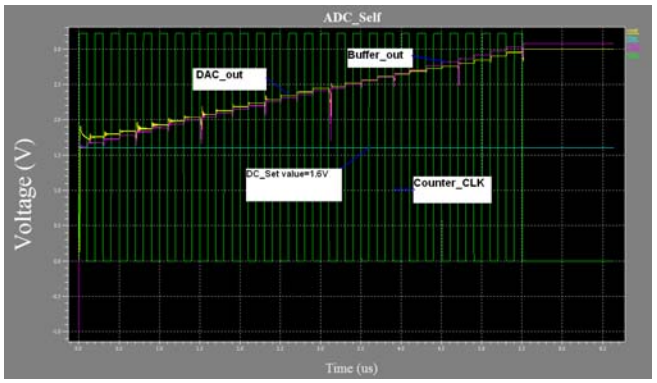

Fig. 6. Simulation of the calibrator for the case: DC set value= 1.6V, dig_ref set binary value= 10100

On this calibrator circuit, different statistical analysis can be carried out, such as:

- To change the simulation model parameters, so called the corner analysis, to investigate the new analog input range of the converter and monotonicity without calibration.
- To change the dc set value for different dc voltage levels and search for the number of missing codes each time to get the optimized dc set value.
- To set the dc ref input to the optimized dc value found from the analysis above, but change the simulation model parameters to search the new required Vref values caught, and to count the missing codes if any (i.e. monotonicity analysis). Also, compare the new analog input range with the original one.

These analyses were carried out in this study and the results are reported in the following section.

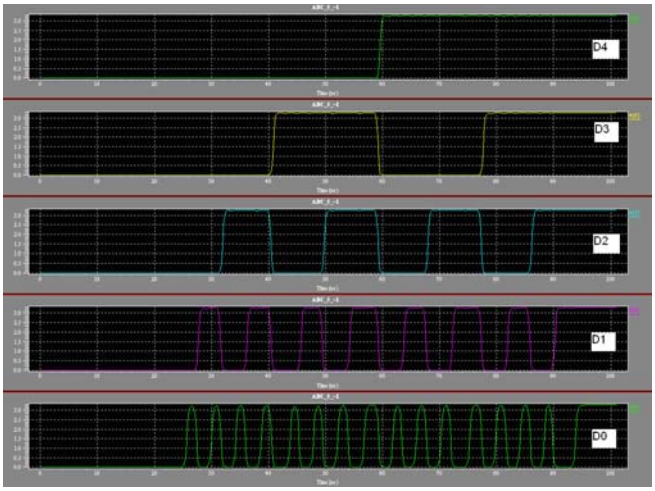

Fig. 7. The Binary outputs of the TIQ based Flash ADC after calibration for a ramp input signal.

4 Conclusion And Discussions

In conclusion, an auto calibration circuit for TIQ based flash ADC cores was designed and simulated. The proposed circuit composed of a special purpose 6-bit R-2R type DAC, a large-swing opamp-based analog buffer with low output resistance, a 5-bit ring counter, and a TIQ based 5-bit flash ADC under calibration designed in 0.35µ CMOS technology. During the design and simulation, Tanner Tools Pro IC design software was used.

The 5-bit flash ADC core was working at very high speed, 2 Gs/s. More detailed simulation results including dc and ac measures of the ADC core are decided to be published in another paper. This paper was especially focused on the calibrator part.

To test the calibrator performance, three different spice model parameters (typical, slow, and fast model

parameters) obtained from the vendor (AMIS) were used. As was expected, small deviation in analog range was observed whenever the model parameter set is changed. To compensate the deviation, the Vref voltage of the TIQ quantizer is automatically changed until the set value of the original design is met. Table I shows the proposed calibrator performance under different model parameter sets for two different *dc_set* values. For the DC-set values, which are close to analog range end points, unfortunately, the required Vref value for the TIQ quantizer unit exceeds the circuit power supply voltage of 3.3 volts. Hence, the power supply voltage for the DAC, counter and analog buffer circuit needed to be increased to 5V. Otherwise, there would be a strong possibility of having some missing codes due to process parameter variations. That means a second power supply voltage requirement, which is one disadvantage of this calibrator. On the other hand, for the DC-set values closer to the mid-point of the analog range give better calibration results. It can be seen from the Table I that, the captured power supply voltage value of Vref is close to the original value of 3.3V. Analog range deviation still exists even after the calibration. However, threshold values closer to the desired points have been achieved around the center quantization region, but it was not so good at end points. One point to remind here that, the monotonic flash ADC is guaranteed in TIQ technique [1]. However, the linearity measures (DNL and INL) will definitely show some deviations due to process parameter variations, as well as during the calibration process in this study. Thanks to the nature of TIQ technique that DNL measures are negligible for the cases before and after the calibration. Therefore the calibrator does not make important changes on DNL measures. On the other hand, INL errors are reduced after the calibration especially for the fast model parameter cases as long as DC set value is kept at the mid point, 1.65 V.

Although they are not depicted here, the thermometer code outputs observed after every calibration process have shown the monotonicity of the TIQ technique.

Table 1. The Auto Calibrator Performance Statistics

	Original Design With typical model	DC Set Value=1.65V Binary 10001				DC Set Value=1.05V Binary 00010	
		With slow model before calibration	With slow model after calibration	With fast model before calibration	With fast model after calibration	With slow model After calibration	With fast model after calibration
Analog Range (Vpp)	1.201	1.07	1.05	1.376	1.32	0.86	1.54
INL (LSB)	0.125	0.53	-0.33	0.84	0.54	-0.59	0.89
DNL (LSB)	+/- 0.025	+0.154	+0.171	-0.217	-0.175	0.186	-0.22
Number of missing codes	0	0	0	0	0	0	0
Corresponding Vref value (V)	3.3	3.3	3.27	3.3	3.21	2.96	3.56
Corresponding LSB value (mV)	40	35.5	34.9	45.8	44	28.66	51.3

For the Flash cores which have higher level of resolution, the selected counter and the DAC resolution levels are suggested to be increased for a better and faster calibration operation. Also, using an up-down counter rather than a ring counter may be an alternative and better way to implement as a future work. On the other hand, at higher sampling rates, the power consumption will be increased in both analog and digital part of the converter. As a result, there might be possible unwanted glitches or fluctuations on the analog buffer output, which will be denoted as the supplying Vref voltage for the analog part of the ADC. A proper selection of an off-chip regulation capacitor connected to the node Vref may reduce this effect.

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