Implicit Identification of Non-Robustly Unsensitizable Paths

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Abstract: This paper presents a novel approach for identifying non-robustly unsensitizable paths using the bounded gate delay model. It is shown that many non-robust paths will remain undetected unless the delay values are calculated at the path level rather than considering calculations at the circuit level bounded delay. As an initial step a canonical data structure is generated where each circuit path is identifiable and the method operates implicitly on this structure. Experimental results show this implicit approach identifies efficiently a large number of non-robustly unsensitizable paths that were not identified in previous work.

Key–Words: Non-Robust Sensitization , Timing Analysis, Bounded Delays

1 Introduction

Delay testing identifies timing defects within manufactured circuits. Modern circuits contain an exponential number of path delay faults (PDFs) and test pattern generators need to exhaustively check the input space to prove that a targeted path is unsensitizable. There are often many different ways to non-robustly sensitize a given path [11]. Various non-robust tests differ in the number and positions of off-input transitions along the targeted path. A high-quality non-robust test is one for which all off input transitions provide enough slack to propagate the on input transition with a high degree of certainty. Identifying such non-robust paths requires knowledge about the delays in the circuit. Including the timing information for off input path removal can yield in higher quality non-robust tests [7]. Paths that cannot be tested under robust and nonrobust sensitization are called non-robustly untestable paths. All non-robustly testable path have to be selected determine the tiiming of the circuit.

In this paper non-robust sensitization conditions are achieved under the bounded delay model. The work in [6] proposed a technique for non-robust fault simulation using bounded delay model, by keep tracking of the hazards generated in the circuit they achieved a high quality non-robust test. Further they use the bounded delay model to determine the timing of the circuit. Therefore it is legal to use bounded delay model for sensitization. A non-robust sensitization under the bounded delay model gives more realistic coverage than the existing methods because traditional non-robust test assumes zero delay for all off path gates. Also the test found by this algorithm are invalidated by other circuit delays.

Generally, the bounded delays are calculated in the circuit oriented graph structure, where the delay of the circuit is traced in topological order and the delays of each line is the sum of delays of its input and the gate delay. However the delay of a line depends only on certain lines. Therefore summing the delays of all the input will be inappropriate.

A unique characteristic of the approach is the representation of the circuit is in a canonical form as a Zero Suppressed Binary Decision diagram (ZBDD) [4]. Since the problem of sensitization and updating the bounded delay are subjected to paths, ZBDDs can be used for the whole process. This canonical data structure stores the paths in the topological order which helps to find the sensitization condition in a single traversal. The ZBDD data structure gives the flexibility of identifying non-robust paths implicitly, so working on the canonical data structure will more appropriate than the circuit structure.

The presentation of the paper is organized as follows. Section 2 gives the sufficient background information about this paper and explains each method with a motivation example. Section 3 describes the proposed method and the conditions used for pruning the Non-robustly unsensitizable paths followed by

algorithm. The experimental results of the proposed methods are presented and analyzed in section 4.

2 Rationale and Motivation Example

A path P_T starting at input line T is a logical path composed of gates and wire segments from the primary input to the primary output line T has a primary input transition $T \in \{rising, falling\}$ and will be denoted by T_f or T_r ; respectively.

A path is said to be **sensitizable** if there is a logical signal that makes all the off input to settle to a non-controlling value under the logical signal.A path is said to be **false path** if it can never propagate a transition to the primary output.A path is said to **non-robustly sensitizable** when the off-input arrives earlier than the on-input in other words on-path $(ncv \rightarrow cv)$ is said to be unsensitizable when the off-input $(cv \rightarrow ncv)$ arrives later than the on-path.

The proposed technique utilizes some of the important properties of **Zero Suppressed Binary Decision Diagram (ZBDD)** for the whole process. The ZBDD is a canonical data structure which is suited toward efficiently storing sets if product terms rather than the sum of product terms as in the case of BDD. In a ZBDD, the absence of a variable V is interpreted as a $V = 0$, unlike the BDDs where the variable V is interpreted as don't-care. This property makes the ZBDD to effectively represent sets of paths as sets of path variables. Fig 3 shows a ZBDD representing all the paths in the circuit shown is Fig 1.We use two ZBDD variables l_r and l_f for each circuit line in l in order to represent the signal transition (rising and falling) on each line l in the circuit.

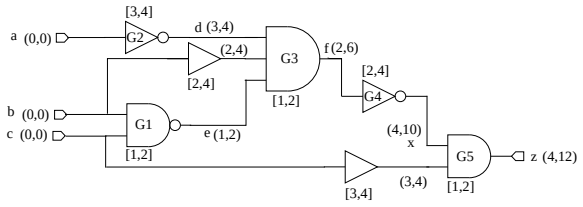

Fig. 1. Illustration of Non-robustly unsensitizable path elimination. (a) Circuit Under Test

In the proposed work we use the bounded delay-model to identify non-robustly unsensitizable paths using an implicit framework. As an example consider the circuit and bounded delay values specified in Fig 1. In Fig 1 at gate G3 path b_refxz is masked by the path a_fdfxz so all paths through b_refxz are non-robustly unsensitizable. Enumerating all the possible paths from the circuit into the ZBDD it is possible to remove the unsensitizable path implicitly using ZBDD operators. If a segment of path is identified as unsensitizable then all the paths through this segment are identified without path enumeration. The delay calculation done in the gate level and sums up the delays of all the fanins of the gate, as a result the minimum and maximum range of the delay values increases at each level of the circuit. Consider the example below where the delay values are updated with respect to each path. The timing of the above circuit is modified for the better explanation for the path oriented bounded delay calculation.

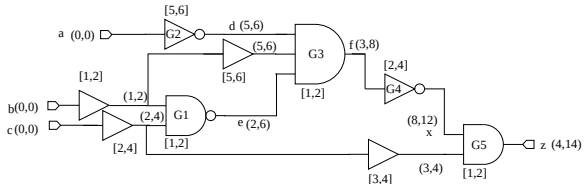

Fig. 2. Illustration of Non-robustly unsensitizable path.

To show the effectiveness of modeling the bounded delays within the ZBDD structure we consider Fig 2. Using the circuit based method, at gate $G3$ input b_refxz $[2, 6]$ is non-robustly sensitizable, but if we consider the path through the lines b_refxz it has a delay bound $[2, 4]$ which is nonrobustly unsensitizable. This can be identified by working on a path by path basis. This may be time consuming and will be an optional step of the proposed method.

3. Implicit Identification of Non-Robustly Unsensitizable Paths

This section describes the implicit identification of non-robustly unsensitizable paths using ZBDDs (ξ). Recently, the work proposed in [1] presented an implicit method to identify non-robustly unsensitizable paths based in the logic values that must be obeyed at each gate in the path. The method is [1] uses functions and is called ST method. We show how to identify additional unsensitizable paths using delays and bounded delay model.

We list below the conditions for removing a path as unsensitizable.For example, consider an AND gate g and let $f_1, f_2, ..., f_m$ be it fanins.

Condition 1: Under bounded delay, if there is rising transitions on $f_{1,2,..n}$ and falling transitions on $f_{n,n+1,...m}$ and if a path $MaxDelay(f_n) <$

$MinDelay(f_{1,2,..n})$, then the path f_n is non-robustly unsensitizable.

In this approach all the paths in the circuit are implicitly enumerated into a single ZBDD(ξ) then the delay values are calculated for the circuit. Let the circuit shown in Fig.1 be the circuit under test. The circuit contains ten paths and each line is assigned an variable with a subscript r $(similarly f)$ representing a rising transition on the line (similarly falling transition). Each line in the ZBDD (from the root node to the terminal node) corresponds to a path in the circuit. This ZBDD can be derived by a single topological traversal on the circuit as shown in Fig. 3(a). In the next phase the sensitization conditions are checked for each inputs of the gate. If a input fails to satisfy the condition *(condition 1)*then the corresponding paths are removed from the ZBDD(ξ). The proposed approach is explained with the following example.

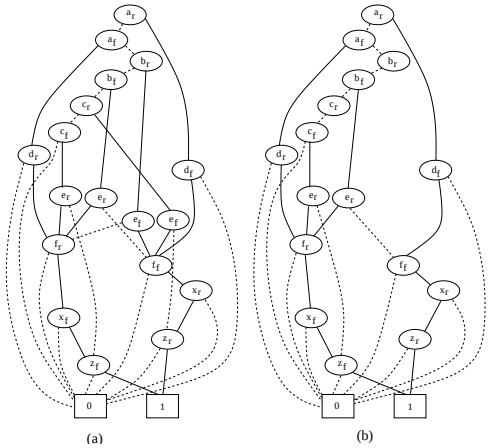

Fig. 3. Illustration of unsensitizable path elimination. (a) ZBDD representing all paths. (b) Reduced ZBDD.

In Fig.1, the delay values are calculated in the first phase considering some delay bounds for the gates and interconnects. At gate G3 when e=0 and if the other two fanins d and b settle in non controlling value then by condition 1 $max(e) < min(d)$ e is non-robustly unsensitizable so all the paths that go through $\downarrow e$ are eliminated from the ZBDD. According to condition 1 all paths containing variable e_f and f_f are non-robustly unsensitizable and can be eliminated from the ZBDD. Let $(S|_{v=1})$ denotes the subset operation, that identifies the subset of a set S whose element contains variable v. The unsensitizable paths are identified from ξ using this subset operation. The process of identifying the untestable paths is simply$(\xi|_{e_{f=1}})$. Fig. 3(b) represents set paths after the removal of paths through e_f and f_f.

Similar operations are carried on to eliminate non-robustly unsensitizable paths through set of lines or subpaths rather that a pair of lines. Further the the subset operations are invoked recursively if two or more variables are to be removed from the ZBDD. This check is done for each gate of the circuit resulting set of sensitizable paths in the ZBDD. The described algorithm is implicit and it is called delay based path sensitization at the gate level or simply, the DG algorithm.

Algorithm 1 Circuit Based NR Sensitization : The DG method

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1: Trace Bounded Delay for the Circuit C
2: Identify the set of all possible paths into ZBDD (ξ)
3: for all Gates G do
4:    for all Inputs i ∈ G do
5:       find inputs n that are Non-robustly Unsensitizable
6:       if maxdelay(i_ON) < mindelay(i_OFF) then
7:          Remove n_ON from (ξ)
8:       end if
9:    end for
10: end for
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Additional non-robustly unsensitizable paths can be identified by working on a path enumerative basis on the circuit structure as was explanined in Fig. 2 earlier. Any path that is found to be unsensitizable can be removed from the ZBDD structure. This optional step is called Delay calculation method at the Path level, or simply the DP algorithm.

4 Experimental Results

We implemented the proposed implicit DG algorithm as well as the path explicit DP algorithm in c language. Table 1 shows the impact of algorithm DG and DP on some ISCAS'85 combination benchmarks (whose name start with c) and the combinational core of some ISCAS'89 sequential benchmarks (whose name starts with s). Column 1 given the number of benchmark. Column 2 the total number of logical paths. Column 3 gives known results of non-robustly unsensitizable paths using the function based method in [1]. Column 4 gives additional paths that can be determined as functionally unsensitizable using the implicit DG algorithm. Column 5 shows how many additional path can be found to be non-robustly unsensitizable using the optional path enumerative algorithm DP. Finally, column 6 gives all the paths that have been found to

Circuit	Total Paths	Non-Robustly Unsensitizable Paths			
		ST Algorithm [1]	Extra paths identified by DG	Extra paths identified by DP	Total paths
C2670	1,359,920	939,750	143,230	148,986	1,231,966
C3540	57,353,342	45,977,048	3,247,805	4,691,682	53,916,535
C5315	2,682,610	1,975,992	191,766	330,401	2,498,159
C7552	1,452,988	945,334	138,177	140,794	12,243,055
S1196	6,196	1,682	400	813	2,895
S1269	79,140	5,384	7,563	178	13,125
S1423	89,452	30,150	14,670	17,888	62,708
S1512	6,972	2,033	609	18	2,660
S3384	39,582	1,180	10,590	13,624	25,394
S4863	2,636,114,122	14,348,196	362,726,520	1,798,425,820	2,175,500,536

Table 1. Non-Robustly Unsensitizable Paths by the proposed method

be non-robustly unsensitizable by all 3 methods combined.

5 Conclusion

This work presents a novel approach to implicitly identify the non-robustly unsensitizable paths. The proposed method is achieved using bounded delay values and the canonical data structure (ZBDD). The framework performs effectively even for large and path intensive circuits. Experimental results for ISCAS'85 and ISCAS'89 benchmark circuits witness that a significant portion of non-robustly sensitized paths were indeed unsensitizable.

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