RSFQ DC to SFQ Converter with Reduced Josephson Current Density

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Abstract: - In this paper we consider the Rapid Single-Flux Quantum (RSFQ) circuits with reduced Josephson current density and especially deal with one of the basic building blocks of these electronics - the DC to SFQ converter. For future promising RSFQ applications the critical current of the Josephson junctions should be reduced (by reduction of Josephson current density) to several μA, resulting into values of the interferometer's inductance of several hundreds of *pH*. Such large inductances cannot be efficiently realized and we utilize an approach for substitution of inductances by arrays of classical Josephson junctions operating in nonswitching mode. We investigate the classical DC to SFQ converter and based on the utilized approach we design a new schematic with reduced Josephson current density. The circuit is optimized with respect to yield and fabrication margins of the design parameters.

Key-Words: - Superconductivity, Rapid Single-Flux Quantum (RSFQ) electronics, Josephson junction, DC to SFQ converter.

1 Introduction

One of the basic applications of the superconductivity is the Low-Temperature Superconductive (LTS) Rapid Single Flux Quantum (RSFQ) electronics [1] based on the Josephson effect [2]. The switching element of the RSFQ electronics is the tunnel Josephson junction. It is a thin nonsuperconductive barrier separating two superconductors designated as S_1 and S_2 in Fig. 1.

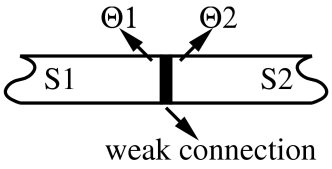

Fig. 1. Structure of the tunnel Josephson junction

Let Θ_1 and Θ_2 be the phases of the complex pair wave functions of the both superconductors and $\phi = \Theta_1 - \Theta_2$ be their difference. Let I_s be the lossless supercurrent flowing through the Josephson junction, I_c - its maximal value (also called critical current of the Josephson junction) and $U(t)$ - the voltage drop over the junction. Then:

$$I_s = I_c.\sin\phi \qquad (1)$$

and

$$\frac{d\phi}{dt} = \frac{2\pi U(t)}{\Phi_o} \quad , \qquad (2)$$

with $\Phi_o = 2{,}07.10^{-15}\ Vs$ - the single flux quantum.

These relations are first predicted by B. D. Josephson [2] and are popular as the *dc* (1) and *ac* (2) *Josephson effects*, respectively.

According to (1), the Josephson junction (Fig. 2) has equal equilibrium states if their superconductive phases differ with a multiple of 2π.

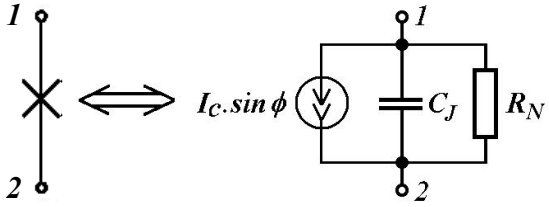

Fig. 2. Josephson junction - electrical symbol, and equivalent circuit

A transient process, during which a 2π change of the junction superconductive phase is performed, is called a switching of the junction. A voltage pulse is generated during such a switching. Its properties can be derived integrating (2)

$$\int_0^\infty U(t)dt = \Phi_0 \,, \qquad (3)$$

Due to the quantized area, this pulse is named Single Flux Quantum (SFQ) pulse. The SFQ pulses care the information bits of the RSFQ electronics.

Equations (1)-(3) demonstrate the internally digital nature of the RSFQ technique. Additionally should be pointed out, that the generation of the SFQ pulses causes an extremelly low power dissipation (of order of $2e^{-19}$ *J per switching*), which determines the attractiveness (with respect to the parasitic interactions and the energy levels to be communicated) of the RSFQ

electronics for future promising applications.
The basic building block of the RSFQ circuits is the superconductive interferometer containing two grounded Josephson junctions J_1 and J_2 having critical currents I_c and connected by a superconductive inductance L (Fig. 3). For optimal SFQ pulse propagation through this cell, the $\beta_L = L.I_c/\Phi_0$ parameter should be of order of 0.5. For optimal SFQ pulse storing, the β_L parameter should be of order of 1.5. Within the classical RSFQ applications, I_c is typically of order of $250\mu A$, i.e. the required inductances are of order of few pH, which can be easily realized as short pieces of microstrip line.

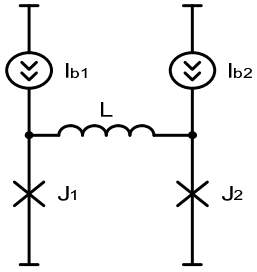

Fig. 3. The basic building block of the RSFQ circuits

The RSFQ technique is very attractive for future applications that require low energy electronics. Such a promising application is the quantum information processing. The ability to manipulate quantum information enables us to perform tasks that would be unachievable in a classical context, such as unconditionally secure transmission of information. For these promising applications, I_c should be reduced to several μA (at least by factor of 10), resulting into values of L of several hundreds of pH [3]. Such large inductances cannot be efficiently realized by microstrip lines (they will cover a lot of chip space, but will also generate even more difficulties due to the violation of the lumped element condition). These problems are one of the hardest constraints for the development of RSFQ digital circuits with reduced junctions' critical currents, and due to this, different solutions for the substitution of big inductances are intensively searched during the past years.
Up to now, the following solutions have been successfully reported in the literature:
a) substitution of the big inductances by π-junctions (see e.g. [4], [5]) - results into very compact and stable RSFQ circuits. Unfortunatelly, the fabrication of π-junctions with the currently available commercial RSFQ technologies is impossible;
b) substitution by arrays of classical Josephson junctions operating in nonswitching mode (see e.g. [6]) - this very new idea replaces the inductance L by an array of few unbiased Josepshon junctions. If an SFQ pulse is propagated through this array, it is unable to switch any of the junctions of the array and meets their Josephson inductance. Thus, an array of 2-3 junctions is able to provide the inductance necessary for optimal SFQ data propagation, and 8-10 junctions replace the inductance of a storing loop;
c) substitution by superconductive passive phase shifters (see e.g. [7], [8]) - in this case, a flux with a value of Φ_0 is frozen into a small passive superconductive loop, causing circulating supercurrents and superconductive phase droping in it. If such a loop is symmetrically connected to the basic RSFQ cell, it introduces the necessary disbalance of the junctions' bias levels, required to perform a successful SFQ data storing.
In this paper we utilize the second approach, namely substitution of inductances by arrays of classical Josephson junctions operating in nonswitching mode. We investigate the classical DC to SFQ [9] converter and based on the approach considered we design a new schematic with reduced Josephson current density. The circuit is optimized with respect to fabrication margins of global design parameters.
The paper is outlined as follows. In the next section we describe the approach [6] for substitution of superconductive inductances by arrays of classical Josephson junctions operating in nonswitching mode. In section 3 we describe the operational principle of the DC to SFQ converter and investigate a schematic with reduced Josephson current density. Then we also describe the new schematic where the inductances are replaced by arrays of classical Josephson junctions and present an optimized version of the schematic parameters with respect to fabrication margins and yield. Conclusion remarks are given in the last section.

2 Substitution of superconductive inductances by arrays of classical Josephson junctions operating in nonswitching mode

If we substitute the superconductive inductance L in the superconductive interferometer by array of n classical Josephson junctions $J_{L1}, J_{L2}, \ldots, J_{Ln}$ we get the RSFQ circuit shown in Fig. 4.
Here $L_{p1}, L_{p2}, \ldots, L_{pn+1}$ are the parasitic inductances that represent the interconnects between the junctions. Their values are very small and can be neglected. It should be noted that the junctions $J_{L1}, J_{L2}, \ldots, J_{Ln}$ have to work in nonswitching mode. Let's the critical currents for junctions J_1 and J_2 are equal to I_c and the junctions J_{L1}, $J_{L2}, \ldots, J_{Ln}$ have identical critical currents I_{cL}.
For tranzient currents less than I_{cL}, each junction in the array behaves as a nonlinear inductance with a value equal to its Josephson inductance $L_{JL}(\phi) = \Phi_0/(2\pi I_{cL}\cos\phi)$,

where ϕ is the superconductive phase drop over the junction.

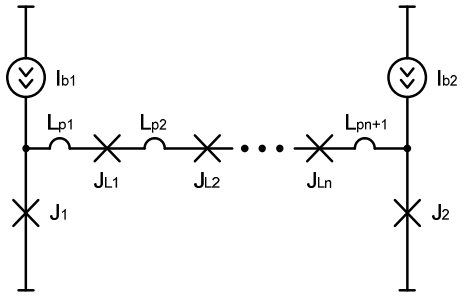

Fig. 4. The basic building block of the RSFQ circuits in which the inductance L is substituted by array of nonswitching Josephson junctions

Assuming that the bias currents Ib_1 and Ib_2 are identical, there is no redistribution current flowing through the array of junctions, i.e. they are not biased ($\phi = 0$ and $\cos\phi = 1$). In this case, $L_{JL}(0)=\Phi_0/(2\pi I_{cL})$ and if the value of the critical currents I_{cL} is of the same order as I_c then the junctions in the array will never switch, due to the switching of J_1 and J_2. If we use [6]

$$\beta_{L0} = \frac{L_{JL(o)} I_c}{\Phi_0}$$

and taking into account that $L_{JL}(0)=\Phi_0/(2\pi I_{cL})$ we get

$$\beta_{L0} = \frac{1}{2\pi}\frac{I_c}{I_{cL}} = 0.16\frac{I_c}{I_{cL}} \qquad (4)$$

i.e. the Josephson inductance of each junction in the array contributes with $0.16(I_c/I_{cL})$ to the β_L-parameter of the schematic in Fig. 4. In case of RSFQ circuits with reduced Josephson current densities, $L_{pi} << L_{JL}$, i.e. these parasitics can be neglected. Thus, the β_L-parameter of the RSFQ circuit considered becomes:

$$\beta_L = n\beta_{L0} = 0.16n\frac{I_c}{I_{cL}} \qquad (5)$$

The fabrication process of RSFQ chips is influenced by many factors, shifting all circuit parameters (and also all critical currents of the circuit) out of their expected nominal values. The global spread influence all circuits parameters on similar way, which can be modeled through multiplication of all nominal values by a certain constant. Because the pulse propagation and pulse storing in the interferometer from Fig. 4 depend on β_L and β_L depends on the ratio I_c/I_{cL}, the operation of the circuit from Fig. 4 is not influenced from the global spread of the fabrication parameters, which usually is the dominant spread within the established commercial fabrication technologies. The operation of the circuit is influenced only from the local spread of these parameters and utilizing the technique for substitution of superconductive inductances by arrays of nonswitching junctions do not require a complete redesign of the circuit. This is true, because the total inductance of the array is automatically scaled reciprocally to the Josephson current density [6], and changes should be done only in bias currents and shunt resistors.

3 New schematic of the RSFQ DC to SFQ Converter with reduced current density

The classical DC to SFQ converter is depicted in Fig. 5.

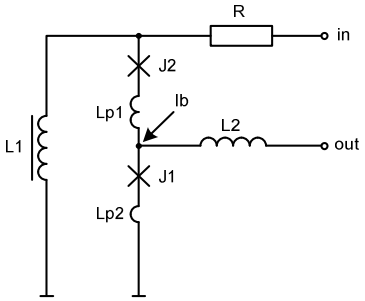

Fig. 5. Classical RSFQ DC to SFQ converter.

If an excitation signal (voltage or current) with a certain level is applied at the input *in*, it sums with the bias current *Ib* through *J1* and flips it. An SFQ pulse is generated at the output *out* and a supercurrent *Is* starts to circulate in the loop *Lp2-J1-Lp1-J2-L1*, because *L1* is chosen to be large enough to make the loop quantizing. Is and Ib flow through J2 in the opposite direction to the excitation current at *in*, so the total current through *J2* is not enough to flip it.

The circuit remains in this stable state until the excitation signal at *in* is switched off. In this case, only *Is* and *Ib* remain to flow through *J2*. They exceed its critical current and flip it, thus braking the superconductive loop *Lp2-J1-Lp1-J2-L1*. The circuit goes in its initial state. If an excitation signal is again applied at *in*, another SFQ pulse will be generated at *out*.

The design parameters of the DC to SFQ converter, optimized with respect to fabrication margins are taken form [9] *R=7.25Ω, J1=250μA, J2=225μA, L1=5.17pH, L2=3.3pH, Lp1=0.55pH, Lp2=1.44pH, Ib=255μA.*

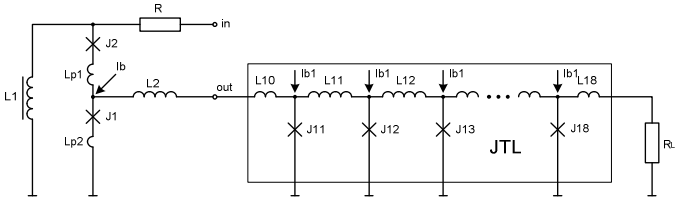

Fig. 6. Classical RSFQ DC to SFQ converter terminated by a JTL.

The behavior of the classical DC to SFQ converter is simulated by using DC voltage with level 2.6 mV applied at input *in*. The converter is terminated by a

Josephson Transmission Line (JTL), i.e. a JTL is connected at node *out* (Fig. 6) in order to shape the output impulse taken at the load resistor R_L=*1kΩ*. The nominal parameters of JTL are taken from [9]: *L10=L18=2pH, L11=L12=..=L17=4pH, Ib=175μA*, critical currents for Josephson junctions *J11=J12=...=J18=250μA*, and parasitic inductances to ground are set to *0.3pH*.
Simulation results are given in Fig. 7. As it can be observed in the framework of one DC excitation, the first pulse appear at the output node (*out*) of the DC to SFQ converter, whereas the second shaped pulse appear at the load resistor R_L.

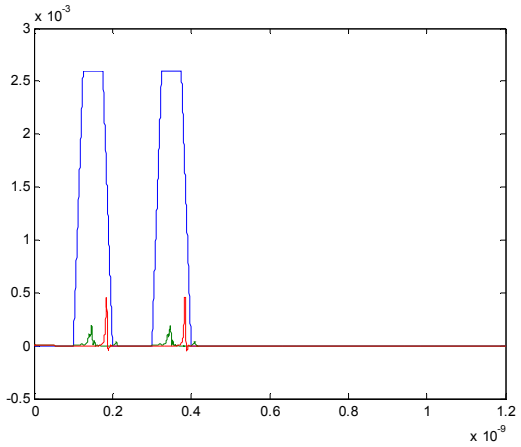

Fig. 7. Simulation results for the classical RSFQ DC to SFQ converter with nominal parameters terminated by a JTL.

In this paper we consider DC to SFQ converter with reduced by factor of *20* critical currents, i.e. multiplied by a coefficient *k=0.05*. This could be done by scaling the Josephson current density by the same factor and keeping the area of the nonsuperconductive barrier constant. For optimal SFQ pulse propagation these require that also all inductances are multiplied by *1/k*.

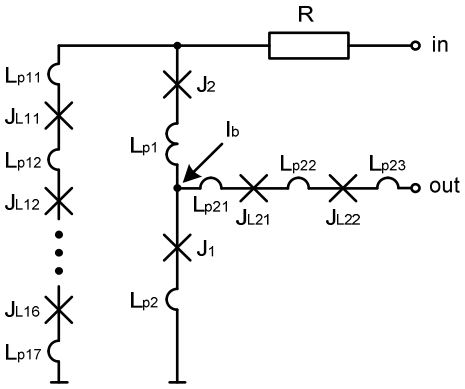

Fig. 8. RSFQ DC to SFQ converter with reduced current density (superconductive inductances substituted by array of classical Josephson junctions).

The result of this scaling is that the inductances *L1* and *L2* of the DC to SFQ converter from Fig. 5 become *L1=103.4 7pH, L2=66pH*, which are unacceptably large values for realization. Here we utilize the approach from [6] replacing inductance *L1* with 6 Josephson junctions J_{L11}, ..., J_{L16} and inductance *L2* with 2 Josephson junctions J_{L22}, J_{L23} operating in nonswitching mode, as it is shown in Fig. 8. These Josephson junctions are not biased and the critical currents I_{cL1} for the Josephson junctions that replace the inductance *L1* are chosen to be *k*400=20μA,* whereas the critical currents I_{cL2} for the Josephson junctions that replace *L2* are chosen to be *k*250=12.5μA*.
The behavior of the proposed schematic of the DC to SFQ converter is simulated by using the same DC voltage with level 2.6 mV applied at input *in*. The converter is terminated by a JTL, which capacitances, resistances and inductances are scaled on similar way (Fig. 9).

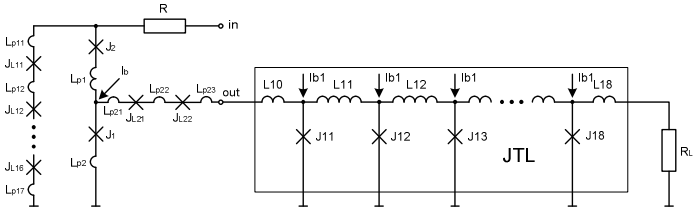

Fig. 9. RSFQ DC to SFQ converter with reduced current density terminated by a JTL.

Simulation results are given in Fig. 10. Similarly to the case of the original schematic from Fig. 6, terminated by a JTL, both pulses appear respectively at the output node (*out*) of the DC to SFQ converter and at the load resistor R_L.

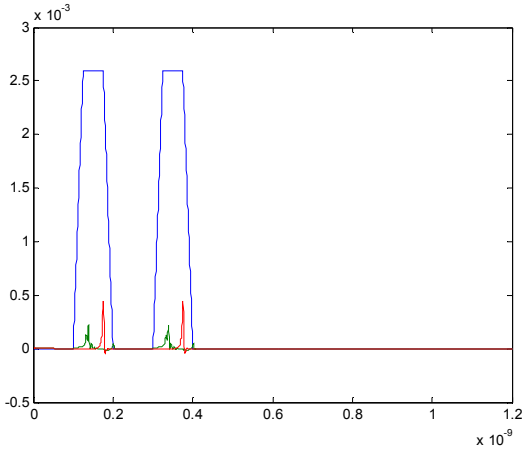

Fig. 10. Simulation results for the RSFQ DC to SFQ converter with reduced current density terminated by JTL.

The aim of our further investigation is to optimize the schematic with respect to margins and fabrication yield of four critical currents:

a) I_{c1} - the critical current of *J1*;

b) I_{c2} – the critical current of *J2*;
c) the critical currents I_{cL1} of the Josephson junctions $J_{L11}, \ldots, J_{L16}$;
d) the critical currents I_{cL2} of the Josephson junctions J_{L22}, J_{L23}.

Using the original values of the elements of the schematic from Fig. 8, the following margins of the considered critical currents are obtained:
[0.53125*I_{c1}, 1.078125*I_{c1}], [0.4609375*I_{c2}, 1.18*I_{c2}], [0.8046875*I_{cL1}, 1.1875*I_{cL1}], [0.5703125*I_{cL2}, 2*I_{cL2}].
We did this by simulations using the freeware simulation program JSIM for circuits using superconductive elements (Josephson junctions). In fact we used an extension [10] of this program for working with parameters and arithmetic expressions.
As one can observe, the nominal values of the critical currents considered are not well located in the margins interval. It has been stressed in [6], that if the original RSFQ circuit is optimized and if the substitution of superconductive inductances is done with array of nonswitching junctions, changes should be done only in the *dc* bias currents and shunt resistors. Thus, to improve the margin intervals, we can change the nominal value of the bias current *Ib* from 12.75 μA to 15.95 μA. In this case the obtained margins of the parameters are [0.738*I_{c1}, 1.28125*I_{c1}], [0.2*I_{c2}, 1.234375*I_{c2}], [0.796875* I_{cL1}, 1.65*I_{cL1}], [0.58*I_{cL2}, 2*I_{cL2}] and the nominal values of the critical currents considered are still not well located in the margins interval. This could not be improved by further change of bias current *Ib*. For further improvement of the margin intervals we changed the nominal value of critical current I_{c2} first to 10.125 μA and second to 7.875 μA. The margins that we have obtained in the last case are [0.74*I_{c1}, 1.25*I_{c1}], [0.285*I_{c2}, 1.77*I_{c2}], [0.795*I_{cL1}, 1.62*I_{cL1}], [0.58*I_{cL2}, 2*I_{cL2}]. For these circuits' parameters, the nominal values of the critical currents considered are better located in the margin interval and thus margins are better than the margins of the original scheme.

4 Conclusion

The future promising RSFQ applications require reduced critical currents of the Josephson junctions. This is realized by proportional scaling of the Josephson current density, keeping the area of nonsuperconductive barrier constant. The reduction of critical currents to several μA, is related to values of *L* of several hundreds of pH. Such large inductances cannot be efficiently realized and we utilize an approach [6] for substitution of inductances by arrays of classical Josephson junctions operating in nonswitching mode. We investigate the classical DC to SFQ converter and based on the utilized approach [6] we design a new schematic with reduced Josephson current density. The circuit is optimized with respect to yield and fabrication margins of the design parameters.

Acknowledgement

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