# A NEW APPROACH FOR AUTOMATED ANALOG DESIGN OPTIMISATION

L. LABRAK, T. TIXIER, Y. FELLAH and N. ABOUCHI
INL – CPE LYON – UMR 5270
43, Boulevard du 11 novembre 1918 – 69616 VILLEURBANNE CEDEX
FRANCE

*Abstract:* This paper presents a new method to improve analog design automation and thus design reuse. A top-down constraint driven methodology is applied to design complex analog system. This approach formulates the design problem as a multi objective optimization problem (MOOP). In the last decades optimization has been introduced in the field of analog design. Nevertheless, the knowledge needed to build an optimization problem dedicated to an analog circuit is still out of reach of designers. Our approach is a new efficient way to capture design performance metrics allowing an automatic optimization problem formulation. Based only on performance specifications (e.g., gain of 80dB) and preferences of the designers (i.e, maximize or minimize a given performance metric), a multi objective optimisation problem (MOOP) is built. An example using hybrid algorithm involving a pattern search based algorithm and a conjugate gradient based one to solve the MOOP for a CMOS two stage Opamp is given.

*Key–Words:* Optimization,Pareto Front, Analog IP, Design Reuse

## 1 Introduction

The so long and ever lasting analog part of sensor interfaces is the most critical phase in the development of mixed-signal designs. Typically, analog cells are characterized by a large number of possibly competing performance specifications that keep analog standard impossible. Thus, designing mixed signal or simply analog systems with changes in any of the specifications frequently involves a complete redesign of the system. A great effort on Computer-Aided Design (CAD) solution has been done during last decades to automate analog design and some industrial product have emerge [4]. Most of these emerging solution have left the earlier knowledge-based approach for the optimization-based ones. Nevertheless, optimization concept introduced to automate the analog design flow has introduced a new level of complexity. Designers have to set parameters of an optimization problem but don't have the keys to guarantee that the solution computed is really optimal. In the optimization method designers have to formulate a cost function to represent objective to be attained by the circuit. Then they must define preference to manage trade off between concurrent performances. Theses preferences and the cost function are fundamentals to ensure a efficient resolution of the optimization problem. In the following paper, we propose a hybrid approach for design and optimization of analog circuits. A new and efficient solution is proposed to build a multi objective optimization problem without requiring additional knowledge of the designer.

At first, a top-down design flow with applications from circuit sizing and automated behavioral modeling will be briefly described. Following, optimization issues and the solution we propose will be described. Finally, an application is proposed on a Sigma Delta ($\Sigma\Delta$) analog to digital converter (ADC).

## 2 HIERARCHICAL METHODOLOGY APPROACH

Top-down design is a design methodology that is useful when designing large complex systems. The aim is to design and verify the system at an abstract level before starting the detailed design of the individual blocks. Thus, we propose a top-down design methodology relying on a hierarchical, constraint driven system description [1]. The first step is obviously the topology selection. It is performed at the system level to choose for example between different types of data converters (mono-bit, single-loop,...) but also at the sub-block level to choose for example between different types of integrators. When a suitable topology is selected at the system level, the aim is then to propagate performance specifications from different lev-

els to enable independent circuit block design optimization. Indeed with top-down design, the individual blocks performance needed to meet the overall system performance requirements is carefully studied and understood before the blocs are developed. This reduces the need for over design in the individual blocks, but at the risk that the anticipated performance for one or more blocks is unachievable, which would require that the system design be revisited. To avoid such cases an optimization is performed at the system level to define performance specifications for all sub-blocks.

## 2.1 Constraint Propagation

Starting from the highest abstraction level of specification, a first optimization is carried out to define the performance to be obtained at each block level. This first optimization process is carried out with the flexible constraint programming method described in [2]. For each block of a system, a functional description of the design enables to formalize the optimization issue and therefore frame the block itself. This step is described in the next section of the paper. This methodology, depicted in Fig. 1 allows the design of analog system providing a virtual prototype with a high abstraction level. Further details can be found in [3].

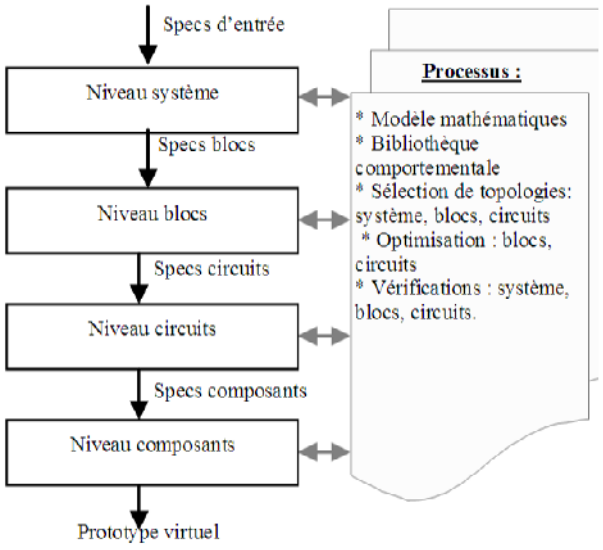


Figure 1: Top-Down design methodology

## 2.2 Hybrid Optimization

We consider in this part the design of a block of a system. Design of analog circuits in general requires a large number of parameters and intensive trade off analysis. In order to overcome the difficulty, building block sizing is undertaken using a multi objective optimization problem (MOOP). Instead of implementing heuristics has it was done in the first analog tools, optimization is used as it is an efficient way to automate analog design flow. Literature on the topic of automated analog circuit synthesis has broadly classified two categories of tools: 1) Equation-based; and 2) Simulation-based approaches [5]. Until today, it is quite difficult to define a most promising approach as none can guarantee both precision and reasonable time calculation. The time needed to formulate the equations is lengthy and is specific to a given circuit topology. On the other hand time computation is very short compared to the simulation based method which do not need a long setting time. Our approach try to take advantage of a formal description of the circuit block, to speed up computation time, but evaluate each solution candidate at the electrical level to guarantee a high level of precision.

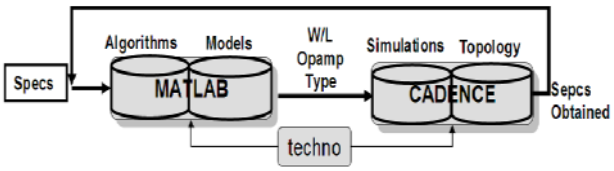


Figure 2: Hybrid Optimization and co-simulation

Fig. 2 shows that our hybrid approach relies on both the equation-based methodology by using a functional description of circuits and the simulation-based methodology by evaluating the performance results at electrical level. The functional description of circuit allows a fast calculation of performance metrics based on a simplified MOS model. Nevertheless, the MOS description is kept sufficiently accurate and capacitive effects are taken into account. Capacitance and transconductance equations have been implemented from $bsim3v3$ simulation model. When the optimization process is successful, a performance evaluation is carried out at the electrical level to ensure feasibility of the circuit. Then if some constraint are not satisfied, a new starting point is defined for the MOOP. The two different steps are managed with a dedicated framework. MATLAB© has been used to implement the MOOP formulation and resolution due to the handling of matrices of large sizes. Performance appraisal at the electrical level is automated with CADENCE© Spectre analog simulator. Co-simulation in real time is undergone by an automatic flow between the frameworks.

# 3 AUTOMATED MULTIOBJECTIVE OPTIMIZATION

## 3.1 Cost Function

Writing an optimization problem to design an analog chip is not an easy task. Designers have to define relationship between the variables and performances, and then, formulate a cost function that have to be minimized. Thus, the key factor in analog circuit optimization formulations is the cost function. It must formulate the exact needs of the analog designer and be able to provide many optimal Pareto points. Pareto points represent the best trade off between concurrent performances. Although the most common way to take into account all the performances trade off is the weighted sum method (equation 1), it does not present the cumulative number of points at the Pareto front and has the major inconvenience of considering the weight parameter on each objective.

$$U = \sum_{i=1}^{n} wi \cdot Fi(\vec{x}) \qquad (1)$$

Where $wi$ weight, $Fi$ objectives.

Even if the question of the weights is widely avoided in analog design literature, it is quite determinant in the resolution of a MOOP. Indeed, depending on weights values you can represent only a part of the Pareto Front of an optimization problem as points of non convex region are not computed. We propose in this work an efficient way to capture designer needs to automatically build the cost function. Based on the physical programming method [7], we implemented a tool that automatically constructs the MOOP of a given analog block. First, it is an optimization method that captures the designer's physical understanding of the desired design outcome in forming the aggregate objective function. On the other hand, it gives a more user friendly and more flexible use of the optimization concept. Instead of giving weights to formalize priority on objectives, designers provide a desired value (for each performance metric) that is used to form a class function. These class functions are designed to ensure convergence of the algorithm and to provide a complete set of Pareto points. The class function must have the following properties: 1) strictly positive 2) continuous first derivative 3) strictly positive second derivative. Three types of class function allow maximizing, minimizing or attaining a target value. The Fig. 3 illustrates the three class function generated for a desired value.

The set of values provided match up with tolerance limits on a target and help quantifying a good or bad result in a similar way to fuzzy logic. The aggregated cost function is of the form (equation 2).

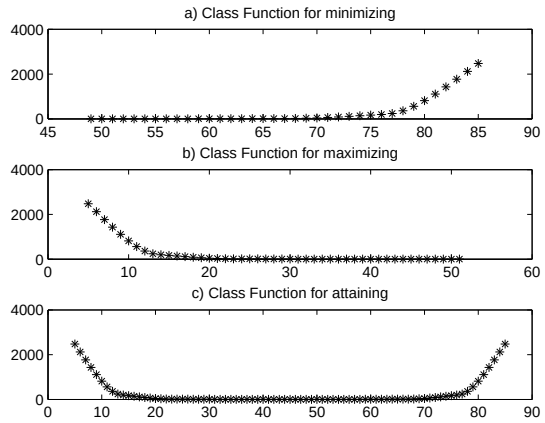


Figure 3: Different kind of class function

$$U = \log\left\{ \frac{1}{dm} \cdot \sum_{i=1}^{n} \bar{Fi}\left[Fi(\vec{x})\right] \right\} \qquad (2)$$

Where: $dm$ number of targets, $\bar{Fi}$ class, $Fi$ objectives.

This method has been implemented to automatically build the MOOP and particularly the objective function. As illustrated in Fig. 4 all informations expected from the designer are related to the circuit and no information such as weights are needed. Collected design performance metrics allow an automatic MOOP construction.

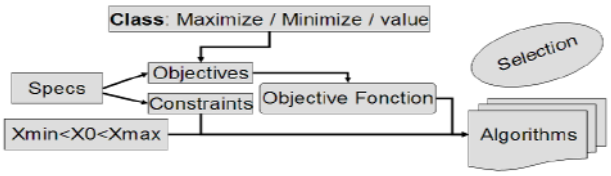


Figure 4: Automatic MOOP construction

## 3.2 Minimization Algorithms

Once the problem has been formulated, the cost function has to be minimized under constraints. Search methods for solving constraint problems can be broadly divided into two categories: global search and local search methods. Most of the studies on analog design automation process have focused on several minimization algorithms that have stressed on global search heuristics [8], [5]. A study has however proved that the simultaneous use of local and global search techniques improve considerably the performance in time calculation and accuracy of results [9]. Our method therefore, relies on both direct type algorithms

and algorithms with global search techniques. Two different methods are implemented. As shown Fig. 5 the first method uses first a global search method to find a minimum. Then if no solution is found a direct search algorithm is used. The other method illustrated Fig. 6 switch between two algorithms until a good solution is found.

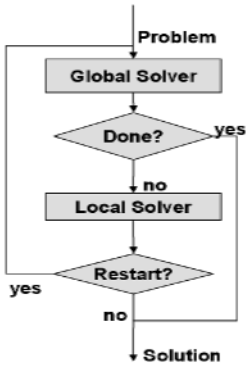


Figure 5: Hybrid method $(a)$ for MOOP solving

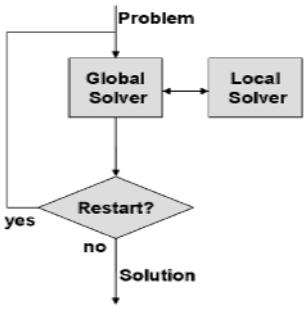


Figure 6: Hybrid method $(b)$ for MOOP solving

# 4 PRACTICAL EXAMPLE: DESIGN OF A $\Sigma\Delta$ (DT) ADC

The method is applied to the design of a $10\,bit$, low frequency ADC. The converter is designed with a $\Sigma\Delta$ modulator (Fig. 7) and digital filters. The technology being used is an AMS $0.35\,\mu$, with a $3.3\,V$ power supply.

Topology selection at the system level and calculation of performances for all sub-blocks is done automatically as described in [3]. The first calculation provides us with the block's performance (amplifier: gain, SR,...). It is based on flexible constraints programming outlined in [3]. After that, a MOOP is created for each sub-block. As an example, we outline below the results for a basic two stage CMOS Opamp with Miller compensation that is used as an integrator of the modulator. Each type of design objective

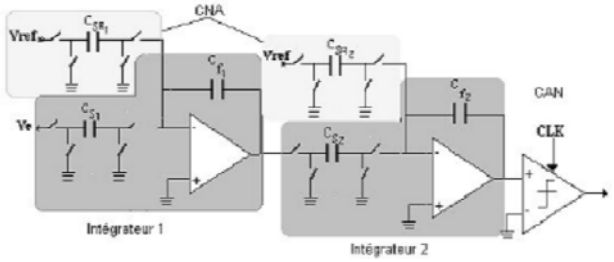


Figure 7: $\Sigma\Delta$ modulator architecture

(performance metrics) is first associated with a type of individual class function distinguished by a general form, such as a monotonically increasing, monotonically decreasing, or unimodal function. For instance, to specify the gain of the amplifier we define a class function that will maximize the value. No weights are to be allocated on each objective since a set of five values is automatically generated to fix tolerance limits. Fig. 8 illustrates a class function built to maximize gain with a $60\,dB$ specification.

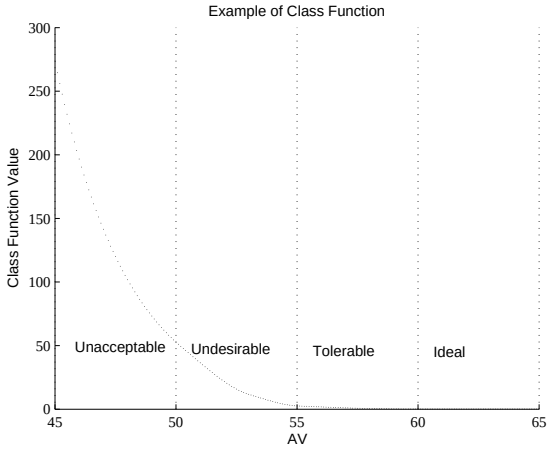


Figure 8: Example of class function

Five values generated to build a class function guarantee convergence of the algorithm and provide a complete set of Pareto points representing trade off between performance metrics. The resulting aggregated cost function is then minimized. As the aggregated cost function can be not derivative in some points, it can be necessary to switch from a direct search algorithm to a global search one. Table. 1 shows results obtained for the design of a two stage Miller Opamp. Performances are computed at the electrical level in a total computation time of $95\,s$.

The algorithm method used to solve this multi-objective optimization problem is the Fig. 5 one. The global search method is pattern search based and does not require any information about the gradient of the

Table 1: Opamp performance results

| **Performance Specification** | **SPEC** | **Simulated Spectre** | **Units** |
|---|---|---|---|
| SR | $\geq 10$ | 12.1 | $V/us$ |
| Gain | $\geq 60$ | 85.5 | $dB$ |
| Noise | $min$ | 60 | $nV/\sqrt{Hz}$ |
| GBW | $> 10$ | 12.6 | $MHz$ |
| Phase Margin | $> 50$ | 67.4 | $deg$ |

objective function. The advantage is that at least it converge in the neighboring of a global minimum and then allow a local search algorithm to easily find the best solution. Local search algorithm used are conjugate gradient based that handle non-linear constrained optimization problem.

# 5 Conclusion

A hybrid approach to optimize and synthesize analog architecture by co-simulation is described. The approach rely on a top down constraint driven methodology to achieve analog design reuse. It uses MATLAB© for functional simulation and CADENCE© Spectre simulator for electric simulation. It includes an efficient way to capture the targets for building and resolution of the MOOP. Mathematical knowledge such as weights of the cost function is eliminated but MOOP automatic formulation guarantee to obtain a good solution. Convergence is also guaranteed by a fast and innovative method that incorporates both local and global search algorithm techniques. This new optimization technique is associated to a top down methodology to allow fast redesign of analog circuits. The efficiency of the approach is proved with the synthesis of $\Sigma\Delta$ (DT) that targets the AMS $0.35\,\mu$ technology. Illustration is proposed on a two stage CMOS OpAmp.

*References:*


[1] Y. Fellah and N. Abouchi and T. Tixier and A. Aubert and L. Labrak, *"Top-down, constraint driven design: application to Sigma-Delta modulator"*, IEEE International Conference on Industrial Technology, pp. 59–72, December 2004.

[2] Chang, *"Top-Down, Constraint-Driven Design Methodology Based Generation of n-bit Interpolative Current Source D/A"*, In Proc. of the CICC San Diego CA, pp. 369-372, May 1994.

[3] Y. Fellah and L. Labrak and N. Abouchi and T. Tixier, *"Automatisation du flot de conception des systemes mixtes : Application au Convertisseur Sigma Delta"*, pp. 63-66, Taisa'06, 2006.

[4] Eckhard Hennig and Ralf Sommer and Lisa Charlak, *"An Automated Approach for Sizing Complex Analog Circuits in a Simulation-Based Flow"*, DATE'02 2002, Designer's forum.

[5] L. Richard Carley and Georges G. E. Gielen and Rob A. Rutenbar and Willy M. C. Sansen, *"Synthesis Tools for Mixed-Signal ICs: Progress on Frontend and Backend Strategies"*, Conference on Design Automation (DAC'96) pp. 298-303, 1996.

[6] RT Marler and J.S. Arora, *"Survey of multi-objective optimization and methods for engineering"*, Structural and Multidisciplinary Optimization, pp. 369-395, volume 26 , $n^\circ 6$, April 1996.

[7] A. Messac, *"Physical programming: Effective Optimization for Computational Design"*, AIAA journal , pp. 149-158, volume 34, $n^\circ 1$, January 1996.

[8] Michael Krasnicki and Rodney Phelps and Rob A. Rutenbar and L. Richard Carley, *"MAELSTROM: Efficient Simulation-Based Synthesis for Custom Analog Cells"*, Conference on Design Automation (DAC'99), pp. 945-951, 1999.

[9] Yi Shang and Yungchun Wan and Markus P.J. Fromherz and Lara S. Crawford, *"Toward Adaptive Cooperation between Global and Local Solvers for Continuous Constraint Problems"*, Workshop on Cooperative Solvers in Constraint Programming, December 2001.