Modification of the CBCM Method

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Abstract: This paper deals with a modification of the CBCM method for floating nonlinear device characterization. Closed form analytical formulae for the estimation of CBCM errors due to parasitic charge injection are presented. A test chip implementing the method was designed and manufactured in the 0.35µm CMOS process.

Key-Words: Charge-Based Capacitance Measurements, MOS characterization, Test Structures

1 Introduction

The CBCM method (Charge-Based Capacitance Measurements) has found extensive use for on-chip capacitor measurements [1]. The method is characterized by high resolution although it is based on equipment found in any average laboratory. Sub-femtofarad resolution has been reported [2]. CBCM was originally developed for linear interconnect measurements. This paper shows a modification of the method to nonlinear MOSCAP characterization. Closed form formulae for the estimation of measurement errors due to parasitic charge injection are presented. A test chip implementing the method was designed and manufactured in the 0.35µm CMOS process.

2 The CBCM method

Fig. 1 shows the principle of the classical version of CBCM method. The test structure consists of a pair of NMOS and PMOS transistors connected in a pseudo inverter configuration. The matched structure on the left is used as reference to increase the resolution. The left and right structures are both driven by two non-overlapping signals to ensure that only one of the two transistors on either the left or the right side is conducting current at any given time. When the PMOS transistor turns on, it will draw charge from V_{dd} to charge up the target capacitance C_x to be measured. This amount of charge will subsequently be discharged through the NMOS transistor into ground. The actual waveform of the charging current is not important - only its DC value needs to be measured [1]. The difference between the two DC currents is used to extract the measured target capacitance C_x as given by

$$I - I' = (Q - Q')\, f = V_{dd}\, C_x, \tag{1}$$

where $Q - Q' = V_{dd}\,((C_i + C_x) - C_i)$, f is the switching frequency, C_i is the intrinsic capacitance, and DC currents I and I' are introduced in Fig. 1.

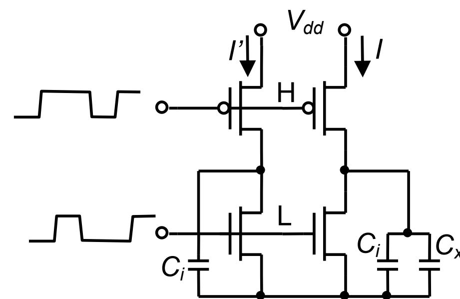

Fig. 1 Principle of the CBCM method.

The simple version of the method is not well suited for the characterization of nonlinear capacitors such as MOSFET gate capacitances. Nonlinear capacitors are characterized by the *C-v* or *Q-v* curves. The standard CBCM allows V_{dd} sweeping but for low voltages its resolution decreases and becomes unacceptable. This is especially critical for minimum-feature transistors, where it is desirable to use large swing to obtain a reasonable current.

The proposed modification is applicable to measurements of floating devices. Two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the device under test. One source is swept while the other is kept constant, and vice versa. For each point of the characteristic a minimal voltage swing and thereby a minimum DC current is guaranteed, Fig. 2.

One period of controlling signals can be divided into four non-overlapping phases, Fig. 3. During

phase 1 the measured capacitor is charged to a negative voltage (seen on its terminals) from the source V_{dd2} through the switches L and S. During phase 2, L is switched off and S remains switched on. Activating the switch H causes charging the capacitor to the voltage V_{dd1}-V_{dd2}. The charge drawn is counted by the ammeter. The voltage changes for V_{dd1}. During phase 3, S is switched off and the capacitor is charged to V_{dd1} through the switch D. The voltage changes for V_{dd2} and the charge drawn is again counted by the ammeter. During the last phase C_x is discharged.

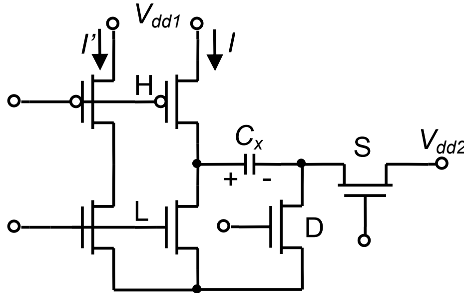

Fig. 2 Principal schematic of modified CBCM.

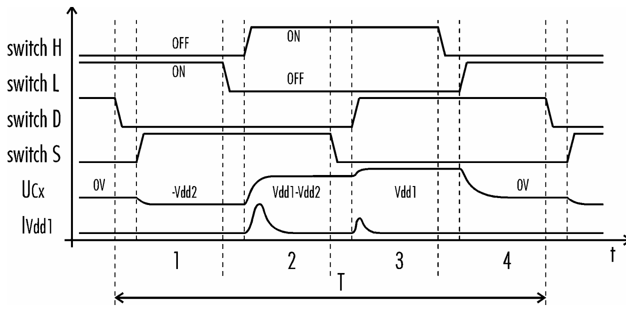

Fig. 3 Switching sequence.

The capacitor voltage varies during one period from $-V_{dd2}$ to V_{dd1} and the charge variation can be determined from the measured currents as

$$\Delta Q(V_{dd2},V_{dd1}) = \frac{I - I'}{f} = \int_{-Vdd2}^{Vdd1} C(v)dv \ . \qquad (2)$$

The dynamic capacitance $C(v)$ can be determined from the reconstructed Q-v characteristic. Formula (2) gives only the value of charge variance.

Let us start the reconstruction of Q-v characteristic for negative voltages from $V_{dd2} = 0$. The voltage variation is then V_{dd1} and the charge variation is $\Delta Q(0,V_{dd1})$. For zero voltage the charge must be zero too, i.e. $Q(0) = 0$. This gives a fixed point in the characteristic. The change of charge due to the sweeping of V_{dd2} is considered relative to this point. Finally we obtain

$$Q(-V_{dd2})_{Vdd1=const} = \Delta Q(0,V_{dd1}) - \Delta Q(V_{dd2},V_{dd1}) \qquad (3)$$

and similarly for the positive voltage

$$Q(V_{dd1})_{Vdd2=const} = \Delta Q(V_{dd2},V_{dd1}) - \Delta Q(V_{dd2},0) \ . \qquad (4)$$

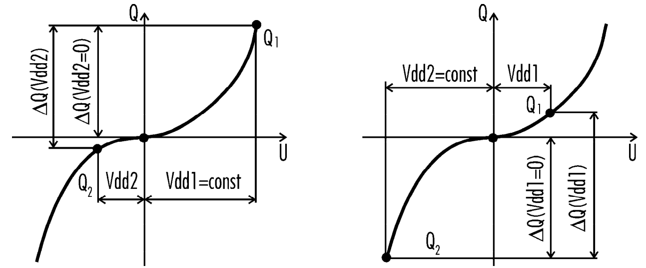

Fig. 4 Reconstruction of Q-v characteristic.

3 Systematic and Random Errors

The capacitance under test should be completely charged and discharged during one period. Fig. 5 shows the steady state voltage of C_x where t_{onH} and t_{onL} are the on-periods of high and low switches, respectively.

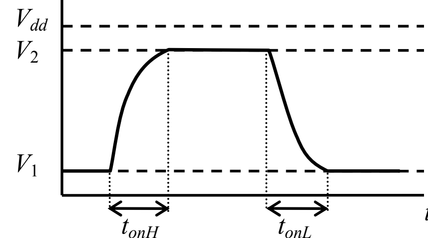

Fig. 5 Steady state of switching process.

In the simplified case of linear switches the steady-state voltage swing is

$$V_2 - V_1 = V_{dd} \frac{(1-k_L)(1-k_H)}{1-k_L k_H} \ , \qquad (5)$$

where $k_L = \exp(-t_{onL}/\tau_L)$ and $k_H = \exp(-t_{onH}/\tau_H)$, $\tau_H = R_{onH}(C_i + C_x)$, and $\tau_L = R_{onL}(C_i + C_x)$. The measurement error is then

$$\delta_\tau = \frac{C_{calc} - C_x}{C_x} = \frac{2k_L k_H - k_L - k_H}{1-k_L k_H} < 0 \ , \qquad (6)$$

where C_{calc} is the capacitance calculated using (1). For example, for $\delta_\tau = -1\%$ and identical switches we obtain $t_{on}/\tau > 5.3$.

Another source of error is the parasitic charge injection from driver circuitry to the device under test [3]. Fig. 6 shows schematically the waveforms of switching transients valid for both the left and the right structures in the basic configuration from Fig. 1.

The unwanted charge injection takes effect both

for L and H switches. At the start of switching cycle, V_{Cx} is zero. Charge injection during switching off of the L switch causes V_{Cx} to be negative. The total voltage swing of C_x is then greater than V_{dd}. Another parasitic injection occurs during switching off of the H switch causing a spike on I or I'.

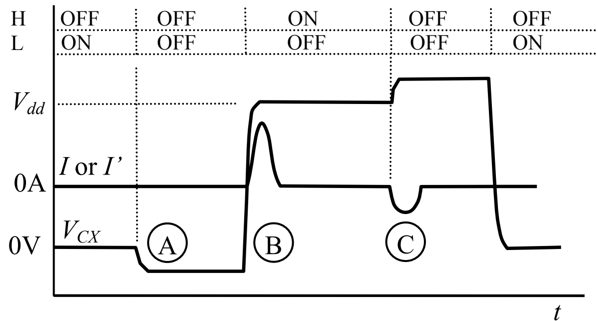

Fig. 6 Switching transients.

Let us consider a single pseudoinverter from Fig. 1 loaded by a capacitor C_L representing either C_i or C_x+C_i. The charge drawn from the V_{dd} source during one period can be expressed as

$$Q_{dd}(C_L) = Q_A(C_L) + Q_B(C_L) + Q_C(C_L) \ , \qquad (7)$$

where Q_A, Q_B, and Q_C are the contributions for transients A through C, Fig. 6. Since Q_{dd} is a nonlinear function of C_L, the parasitics of the left and the right structures cannot compensate as in (1) even in the case of perfect matching

$$Q - Q' = Q_{dd}(C_x + C_i) \text{-} Q_{dd}(C_i) \neq V_{dd}\, C_x \ . \qquad (8)$$

This represents the systematic error of CBCM. Moreover, the error is both process and matching sensitive.

The analysis of charge injection is based on a lumped switching model introduced in [4], which is simple enough to allow an analytical solution. The lumped model is valid if the gate voltage drops much slower than the intrinsic carrier transmit time in the transistor ($\tau_C = R_{on} C_{ox}/4$). For a submicron process τ_C is in the order of picoseconds for short transistors.

The transistor is characterized by the threshold voltage V_T, current factor $\beta = \mu C'_{ox} W_{eff} / L_{eff}$ and by the overlap capacitances C_{GDO} and C_{GSO}. The body effect need not be taken into account since V_{BS} is constant.

3.1 Transients A and C

The unwanted charge injection occurs during the switching off process. For transient times much larger than τ_C, the channel charge is initially split equally between the source and the drain. The redistribution of charge from the drain to the source is determined by their voltage difference and time constants [5].

Let us consider the basic configuration in Fig. 7. The initial capacitor voltage is zero. The capacitor voltage will be negative after the transient but small enough not to cause a significant current through the drain-bulk junction.

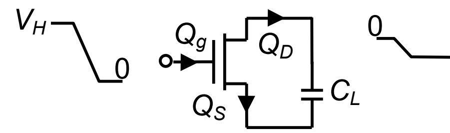

Fig. 7 Model for transients A and C.

The charge injection was studied, for example, in [4], [5]. If the gate voltage is a ramp function which begins to fall at time 0 from the high value V_H toward 0 at a falling rate U

$$V_G = V_H - U t \ , \qquad (9)$$

the charge injected to the drain terminal can be expressed in a closed form as

$$Q_D(C_L) = -\sqrt{\frac{\pi U}{2\beta}} \frac{C_L C_{GD}}{\sqrt{C_L + C_{GD}}} \operatorname{erf}\left(\frac{(V_H - V_T)\sqrt{\beta}}{\sqrt{2U(C_L + C_{GD})}} \right) - C_{GDO} V_T \qquad (10)$$

where $C_{GD} = C_{GDO} + C_{ox}/2$.

Using the charge-conservation principle, the charge injected to the source terminal will be

$$Q_S(C_L) = Q_G - Q_D(C_L) \ , \qquad (11)$$

where Q_G is the gate charge drawn from the driver

$$Q_G = -(V_H - V_T) C_{ox} - (C_{GDO} + C_{GSO}) V_H \ . \qquad (12)$$

The parasitic charges from (7) will be

$$Q_A(C_L) = -Q_D^N(C_L) \ , \qquad (13a)$$

$$Q_C(C_L) = Q_G^P - Q_D^P(C_L) \ . \qquad (13b)$$

Q_D^N and Q_D^P are determined from (10) and (11) using the NMOS or PMOS transistor parameters.

3.2 Transient B

Fig. 8 represents the equivalent circuit for transient B when L is switched on. The capacitor is charged from the initial voltage 0 to V_{dd}.

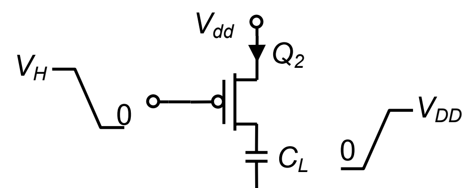

Fig. 8 Equivalent circuit for transient B.

Using the charge-conservation property, the

charge drawn from the V_{dd} source will be simply

$$Q_2(C_L) = C_L V_{dd} + C_{GSO} V_H + C_{GDO}(V_H + V_{dd}) + C_{ox}(V_{dd} - V_T) \quad (14)$$

In the case of ideal matching Q_2 can be compensated

$$Q_2(C_i + C_x) - Q_2(C_i) = C_L V_{dd} \; . \quad (15)$$

The injection induced error is then

$$\delta_i = \frac{C_{calc} - C_x}{C_x} = [Q_{dd}(C_x + C_i) - Q_{dd}(C_i)]\frac{f}{C_x V_{dd}} - 1 \, , \quad (16)$$

where C_{calc} is calculated using (1).

4 Test Chip

The test chip was manufactured in the AMIS 0.35µm technology, Fig. 9.

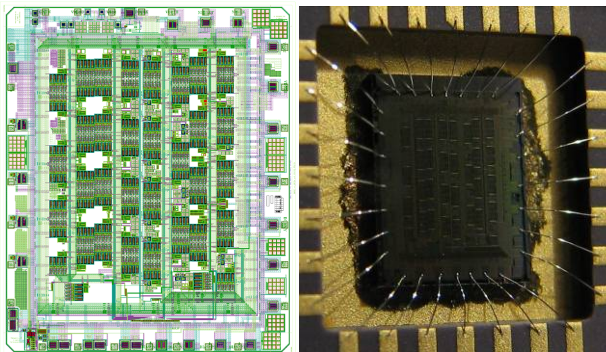

Fig. 9 Top layout and die photograph of test-chip.

The main purpose of developing the method was to characterize nonlinear MOS gate capacitors. Such capacitors provide a higher specific capacitance per unit area and do not require additional masks, but the nonlinearity must be carefully compensated. Fig. 10 shows measured *Q-v* and *C-v* characteristics of 1µm x 1µm NMOS transistor. The clock generator frequency was set to 10 MHz.

5 Conclusions

A modification of the CBCM method for nonlinear capacitance characterization was proposed. Just two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the measured object. Closed form formulae for measurement error have been derived. A test-chip implementing the method was designed and manufactured in the 0.35µm CMOS process. It was successfully used for MOSCAPs characterization in the full operating range.

6 Acknowledgements

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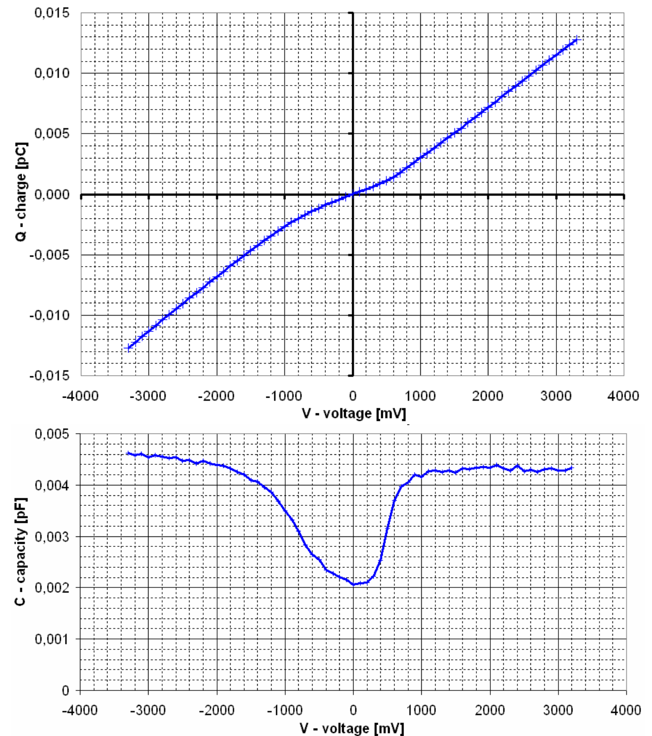

Fig. 10 Measured characteristics of MOS gate.

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