Floorplan considering interconnection between different clock domains

Linkai Wang, Xiaofang Zhou
ASIC & System State Key Lab
Fudan University
NO.825 Zhangheng Rd. Shanghai 201203
CHINA

Abstract: A further research on floorplanning considering multi clock domains is presented in this paper, which concentrates on interconnection between different clock domains. This contributes to simplification of clock tree and signal routing between different clock domains. Experimental results show that better floorplan can be obtained through our floorplanning proposed in this paper.

Key-Words: Floorplan Clock domain Interconnection Physical design

1 Introduction

As the complexity of SoCs is increasing, most chips contain multi clock domains rather than only one. To design this kind of complex chip, a common methodology is to design different blocks respectively and make sure that each block is driven only by one clock [1], and then use synchronizers such as FIFO (first in first out) module to connect each other of different clock domains. This presents another challenge in layout design，clock tree generation, and wire routing. In this paper we propose a floorplanning method considering this problem in higher level of physical design —floorplan.

In traditional design flow, clock tree routing problem is processed after all blocks and cells' location have been fixed. However this always makes the clock tree routing more difficult and the clock skew harder to reduce. To get faster design convergence, it is meaningful to consider the clock tree routing problem in higher design level.

And it is also necessary to consider the signal interconnection between different clock domains. This will contribute to a shorter wire-length routing.

Floorplanning is a key step in physical design. It decides the area, wire-length and performance of a chip to a certain extent. In this paper we model the interconnection between different clock domains and reach satisfying floorplanning result after considering this constraint in floorplanning step.

This paper is constructed as follows: we first explain why we should consider clock tree and wire routing in floorplanning step in section 2. Following is the representation and optimization algorithm used in this paper. In section 4, our floorplanning is introduced. The experimental results are listed in section 5 and we conclude the paper in section 6.

2 Problem formulation

For a design with multi clock domains, the floorplanning problem is always more complex. To design a chip with simpler clock routing, shorter wire length and better performance, we usually place all blocks with the same clock together, which has been considered in [2].

Another constraint should be considered is the interconnection between different clock domains. Modules that exchange signal or data between two clock domains should also be placed as near as possible.

That is because in multi clock IC design we use special module called synchronizer such as FIFO to communicate between different clock

* This research is supported by Shanghai Science and Technology committee and Shanghai N&S fund under granted number 06ZR14016

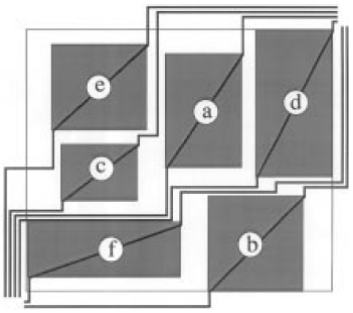
domains. It overcomes the meta-stability problem between different clock domains [1]. One point should be noticed is that each synchronizer block contains two clocks and more concentrated signal wires between two clock domains. To make the clock tree and wire routing easier, it is reasonable to place the sender module and the loader one together.

3 Preliminary

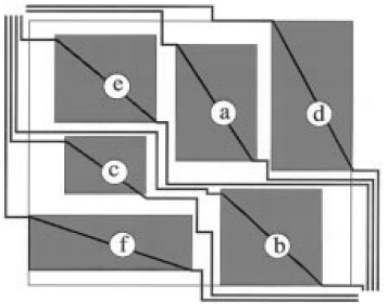
3.1 Sequence pair

In this paper, we adopt sequence pair [3] as the representation in our floorplan because it's facility in operation and less storage requirement. And the fast LCS algorithm proposed in [4] is used to decrease the time of transforming a sequence pair into floorplan. It decreases the time of evaluating a sequence pair from O(n^2) to O($n \log n$) after each operation.

Sequence pair is an elegant non-overlap representation that uses a pair of sequences to reflect the location relationship of the blocks as illustrated in figure 1:



Positive sequence: (e, c, a, d, f, b)



Negative sequence: (f, c, b, e, a, d)

Fig.1

The sequence pair operation used in this paper is listed as follows:

1): Rotate a block.
2): Swap two blocks within same clock domain in positive sequence.
3): Swap two blocks within same clock domain in negative sequence.
4): Swap two blocks within same clock domain in both sequences.
5): Swap all blocks of two clock domains in positive sequence
6): Swap all blocks of two clock domains in negative sequence.
7): Swap all blocks of two clock domains in positive both sequences.

The above operations which take clock domain into consideration make sure that all blocks with the same clock are placed together and also decrease the solution space [2].

3.2 Floorplanning algorithm: SA+LP

The floorplanning optimization problem is one of NP hard problems. Heuristic method is usually adopted to find optimal result. Simulated annealing (SA) method is one of those heuristic methods that are commonly used in floorplanning. The algorithm is something like greedy local search method, but the difference lies in that SA can accept an inferior result in a certain probability that determined by the current temperature and average delta cost as illustrated in formula (1).

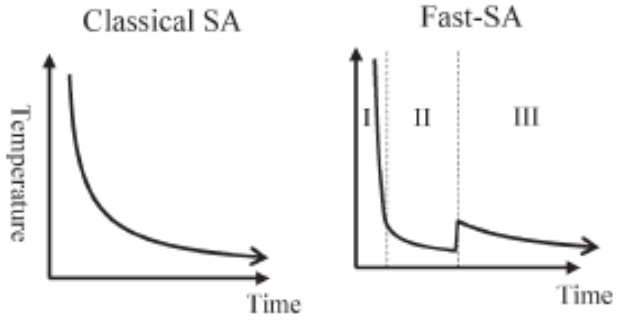
$$p = e^{-\Delta cost/T} \quad (1)$$

This avoids the searching process trapped in one sub optimal result.

Since SA alone always consumes long time to get satisfying results, we use two stages optimization. At the first stage, fast simulated annealing is used to get an initial floorplan and all soft modules are treated as hard ones. And at the second stage, the aspect ratio of soft modules is adjusted to minimize the area by very fast linear programming method. Because the relative

location will not be changed at the second stage, the wire length will be affected little.

We use modified recallable SA, which can store the best result that have been found so far. A new temperature dropping strategy is adopted that proposed in [5] as illustrated in Fig.2. By changing the temperature controlling process as depicted in figure 2, it accelerates the convergence of SA process. In the first part the temperature is set very high and random search is processed. And in the second part, pseudo local search is used. Then after increasing the temperature, normal SA is adopted in the third part



a b

Fig.2

After the SA processing stage, linear programming method proposed in [6] is adopted for the second stage optimization. The aspect ratio of soft modules is adjusted between a certain ranges.

Compared with SA alone optimizing process, the SA+LP method can get better floorplan result with less area and can distinctly decrease the optimization time in SA.

4 Floorplanning

Considering that the signal communication between different clock domains is always concentrated on one sender module in one clock domain and loader in the other, we take the sender block and corresponding loader block in deferent clock domains as inter- block pair.

Obviously, a system with *N* clock domains contains at least *N*-1 pairs of inter-blocks since there is no isolated clock domain in an integrated system. We need place each pair of inter-blocks as near as possible in the final floorplan, and this constraint should be considered in floorplanning.

Three algorithms are usually used in floorplanning to satisfy certain constraints: the first is floorplan repair [7], which is a method that modifies the constraint violation after optimization process. The second is transforming a constraint violated floorplan into a feasible one after each operation in SA [8]. And the third is adding penalty item in the cost function of SA [9]&[10].

Compared with the other two methods, the third one is more general and more robust which is adopted in this paper. The key point is constructing a suitable model and the penalty item in the cost function of SA.

In order to place the blocks of an inter-block pair in different clock domains together, the dummy connection distance between inter-block centers as illustrated in Fig.3 is calculated to form the penalty item according to formula (2).

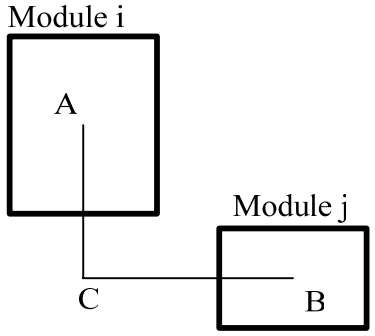


Fig.3

$$D = |AC| + |BC| \qquad (2)$$

To minimize the D in a non-overlap floorplan will make sure that the inter-blocks are placed as near as possible. And we use summation of dummy connection distance of all inter-block pairs as the penalty item in the cost function.

Now the final objective cost function is:

$$\begin{aligned} cost &= \alpha * area / norm\_area + \\ &\beta * wirelength / norm\_wirelenth + \\ &\gamma * \sum D / norm\_\sum D \end{aligned} \qquad (3)$$

α , β , γ are the weights of area, wire length and summation of dummy connection distance.

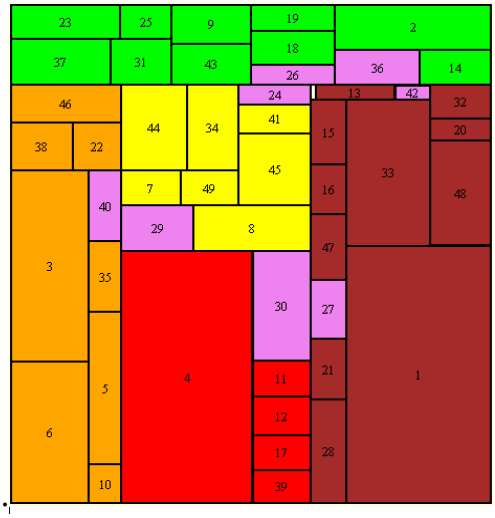
All items in the function are normalized by average value calculated in random search stage of SA for the sake of cost calculation.

5 Experimental results

We use MCNC benchmarks ami33 and ami49 as our test bench. A program is used to randomly endow each module with clock identity because there is no clock domain information in MCNC benchmarks. It determines the clock domain which the module belongs to and whether or not the module is inter-block. The random selection is not completely consistent with the signal net provided in the benchmarks，so the signal wire information given by MCNC is ignored in our experiments. But this will not affect verifying the validity and reliability of our floorplanning. We partition the test bench into five clock domains and choose four pairs of inter-blocks. And the weights of area and summation of D are 0.6 and 0.4 respectively at the first SA process stage.

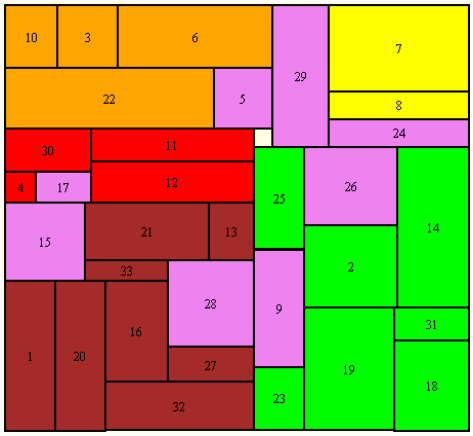
At the second LP stage, aspect ratio of soft module is adjusted and the area is optimized further, the aspect ratio range of soft modules is 0.2~5 in our experiment.

We implemented our experiments in C++ language on a 2.8G Dell PC with 256M memory. The floorplan and relevant data result are as follows:



Ami49

Fig.4 floorplan result of ami49



Ami33

Fig.5: floorplan result of ami33

We can see clearly in Fig.4 & Fig.5 that after our floorplan, not only module blocks within the same clock domain were placed together, but also those inter-blocks which we endowed with violet color in the figure were placed together, such as block 28 and block 9 in Ami 33，block 30 and block 27 in Ami49.

Table.1 lists average results of ten times and the best result in our experiments.

Table.1:

Test bench	Ami 33	Ami49
Average area(mm^2)	1.18	36.32
Best result(mm^2)	1.17	35.83
Average Time(s)	136	247
Dead Space	1.7%	2.4%

Comparing with the results presented in [2], we implemented new constraint considering interconnection between clock domains and the area is improved further both in best and average results as listed in table 2.

Table.2:

Test bench	best(mm^2)		average(mm^2)	
	Zhao	Ours	Zhao	Ours
Ami49	36.58	35.83	37.38	36.32

Since new constraint added in SA, the time consumption increased naturally. Our floorplan is sill a competitive one as far as the area and constraint satisfied are concerned.

6 Conclusion

This paper presents a kind of floorplanning considering interconnection between different clock domains. Experimental results show that we can get better floorplan result considering clock domain and signal routing which is more practical in multi clock IC design than just considering area and wire length.

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