Direct Digital Synthesizer Architecture Based on Amplitude Sequencing

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Abstract: - The paper introduces an architecture for a direct digital synthesizer based on algorithmic direct amplitude generation. The circuit implementing the algorithm has a gate count proportional to digital precision length and in its simplest form includes one compare, one addition and several increments per iteration step. A phase compensation method is described to eliminate the nonuniformity in timing of the samples inherent to the algorithm. The paper also presents an analysis of the proposed architecture focusing on the amplitude samples timing accuracy versus generated signal frequency. A FPGA implementation of the architecture was simulated using a VHDL description to validate the solution as proposed .

Key-Words: - DDS amplitude centered architecture, Jordan's nonparametric curve generator, signal generation solutions in FPGA.

1 Introduction.

Digital implementation is one of the trends in the design of electronic systems recently. The direct digital synthesis (DDS) is such a example. The analog solution of sinusoidal signal generation using PLL's was replaced by DDS based solutions [1][2].

The major problem of the DDS architecture is the necessity to do phase truncation to end up with a reasonable amount of ROM on the chip although solutions have been proposed to contain the problem [3][4]. Original solutions for dealing with ROM size or using methods to replace the ROM part have been reported with ought closing the issue successfully [5] [6] [11].

The proposed new architecture's main idea is the replacement of the look up table (LUT) module implementing phase to sine translation with direct amplitude values calculated algorithmically. The amplitude values are obtained from a extended variant of the Jordan's nonparametric circle generator algorithm. The values are the coordinates of a generic approximating point that tracks the circle following a rectangular grid according to a distance minimization criterion [7].

The algorithm provides values for the amplitude of sine and cosine functions with a linear relation from word length to the circuit gate count.

The phase truncation problem of the DDS architecture does not exist in the new proposed architecture.

Part 2 of the paper presents a method to compensate the phase nonuniformity error inherent to the algorithm. The compensation results in a decrease of the maximum possible generated frequency. Amplitude value need to be distributed nonuniformly requiring a minimum period in between samples to accommodate precise adjustments.

Part 3 presents the main elements of the proposed architecture and characteristics showing that the main advantages of the DDS architecture are preserved.

Part 4 presents conclusions and further work outline.

2 Compensation of sample timing

According to the original Jordan's algorithm the coordinates of the tip of the rotating vector are determined sequentially as increments on one or the other axis as to minimize the distance to the implicit function describing the circle. The increments are determined comparing the implicit circle representing function directional derivatives signs and implicit function value for deciding the next increment direction.

The algorithm is described by the equations and block diagram of its hardware implementation presented below. The coordinates of the points

approximating the circle are obtained by successive increments based on the minimal distance to the circle constraint.

Deltax and deltay take the values {1,-1} if selected for a move along respective axis and zero if not selected. PDF variables stand for directional derivative values and Next and Last for implicit function variables values at each iteration.

$$PDFx = PDFx + 2\ deltax \quad (1)$$

$$PDFy = PDFy + 2\ deltay \quad (2)$$

$$NextFx = LastF + PDFx\ deltax + 1 \quad (3)$$

$$NextFy = LastF + PDFy\ deltay + 1 \quad (4)$$

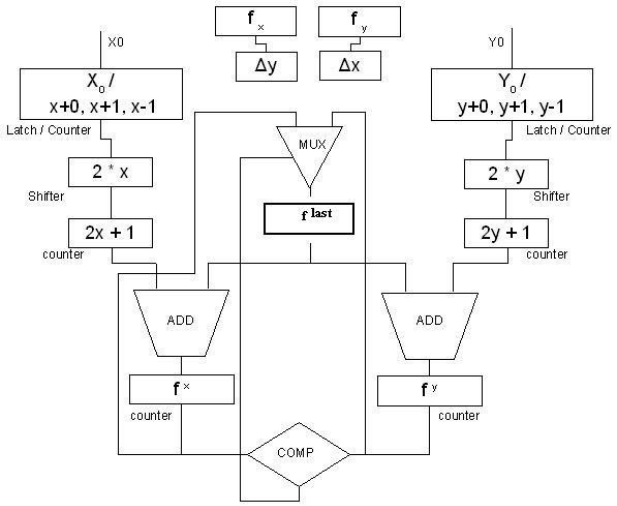

Fig. 4 Block diagram of the hardware implementation of the generator algorithm.

The major drawback of using Jordan's curve generating algorithm for determining trigonometric function sequences is that the approximating point tracking the circle does not move at a constant speed .

The nonuniformity is given by the following formula as indicated in the original paper:

$$Ni/R=1+\sin(sigma(t))-\cos(sigma(t)) \quad (5)$$

where Ni is the i-th approximation, R is phase vector length and sigma the phase.

The direct immediate use of the determined values for the generation of sine and cosine functions results in phase distortions as presented in Fig. 3.

In applications using sequences of trigonometric functions where the uniform sampling is not a hard requirement the algorithm can be used successfully if the sample timing is compensated.

The solution proposed for no phase distortions is the distribution in time of each sample according to the corresponding phase as it was determined.

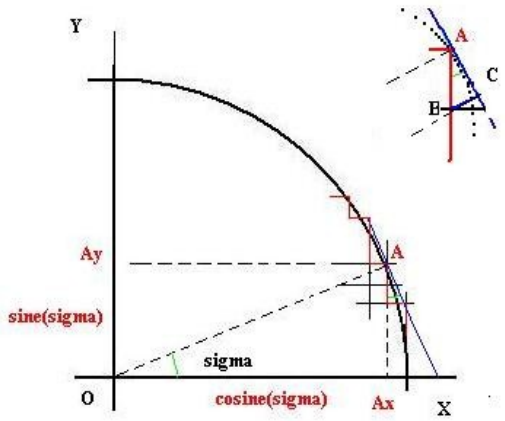

Fig.2 Presentation of the geometrical argument for the phase error correction proposed method .

For the determination of the correct time distribution of samples we propose a method based on an observation based on formula (1). The phase angle advanced at each step of the algorithm along one axis is proportional to the sine or the cosine value at the corresponding phase of the approximating step on the circle.

A method to calculate the sample time delay for a step is indicated in Fig. 2. The phase advancement at each step can be approximated by the step length projection on the tangent to the circle (segment AC):

$$AC = AB \cos(sigma) \quad (6)$$

$$\cos(sigma) = Ax/R \quad (7)$$

$$AC \sim Ax \quad (8)$$

There fore the current calculated value Ax for the coordinates of the approximated point can be used to time a approximate delay for the sample when used to generate the sine and cosine signals.

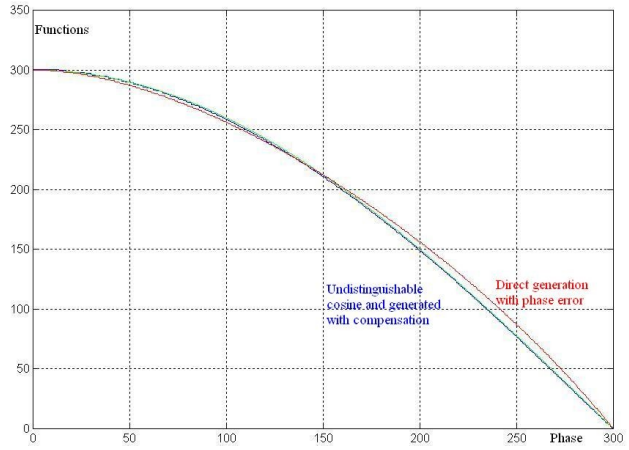

Fig 3. A compensated in time non uniform distribution is not distinguishable from a calculated cosine function simulated in MathLab.

3 Amplitude core DDS Architecture

The work reported in the paper proposes a new class of DDS architectures using the trigonometric function generating algorithm as the core module. The main characteristic of the new class is the absence of the phase to sine look up table translator module. The phase to frequency transfer function core is replaced by a direct algorithmic amplitude generated core.

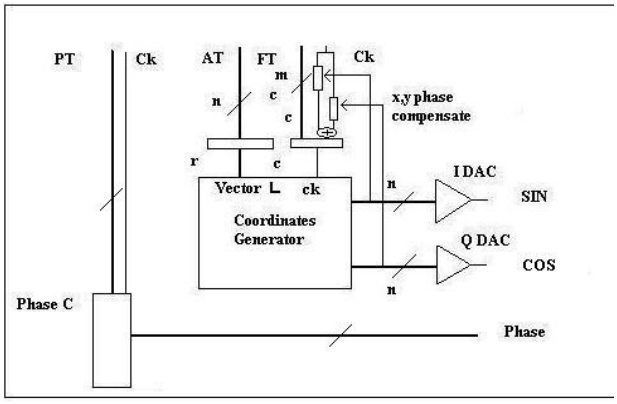

Fig.2 Amplitude based DDS architecture block diagram illustrating the principle.

The block diagram in Fig.2 presents the main modules of the proposed DDS architecture.

Frequency tuning is implemented by a loadable counter. The upper frequency limit of operation is given by the maximum clock frequency available in the target technology scaled down by the phase compensation counters length depending on the desired phase accuracy. The frequency tunning word can change at any moment during the cycle with ought any loss of precision in the generated signals and preserving the phase accuracy .

A phase counter can be included in the circuit as a parallel reference for use in applications that rely on phase.

The main advantage of the proposed architecture is that the accuracy of the signal at output is only limited by the rank of the DAC converter and the generation of very pure signals is feasible with minimal resources [8]. The cost of implementing long word length is linear with the word length.

The output spur frequencies due to phase truncation problem of DDS is not present in the new architecture.

The phase compensation is implemented by the two clock delays counters using the current coordinate values to determine the sample time delays.

A trade off must be made between accuracy of delay timing and maximum output signal frequency. Truncation of the time delay to raise the maximum frequency results in an increase of ripples in the output waveform. Fig 5. presents a MathLab simulation of generated signal with a truncated delay.

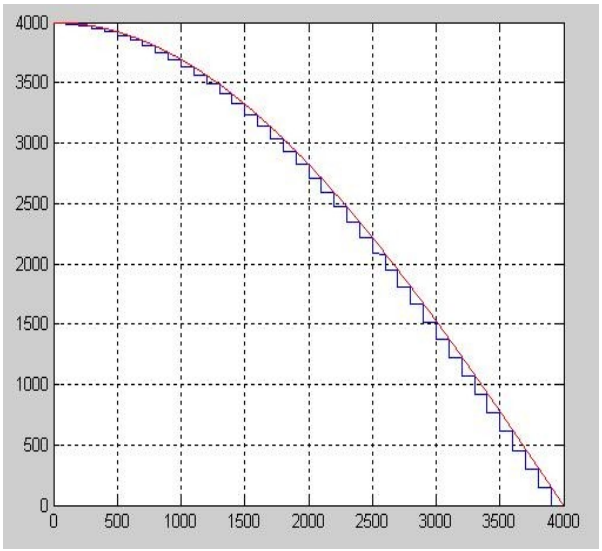

Fig. 5 Simulated delay timing truncated as a trade off between minimal phase error and maximum output frequency.

The very high match of the quadrature output inherent to DDS is preserved since the algorithm determines both sine and cosine values simultaneously.

The very accurate and versatile FSK capability of the DDS architecture is preserved with frequency hopping speed dependent on counter loading latency only.

The amplitude tunning values are frequency dependent and can be correlated by external calculus.

The simulation of the implementation of the architecture in Xilinx FPGA was made in order to validate the characteristics of the architecture as proposed. Fig. 6 presents a result of the simulation.

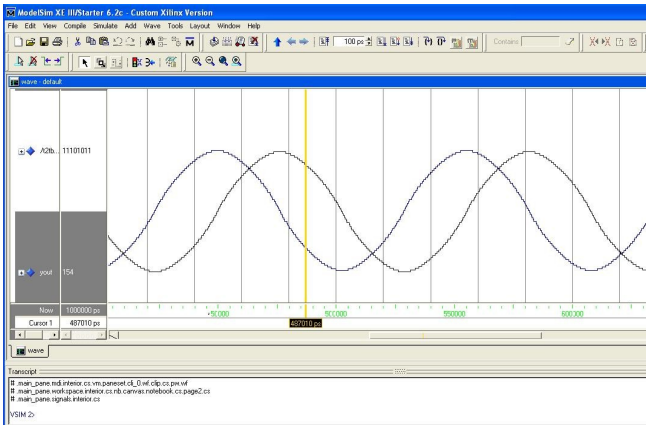

Fig.6 A VHDL structural simulation of a implementation of the DDS architecture as proposed on Xilix Virtex Pro II .

4 Conclusions

A novel DDS architecture is proposed based on direct algorithm generated amplitudes. The new architecture is analyzed in its capacity to generate accurate and high speed sine/cosine signals. A method to compensate the phase error inherent to the amplitude generating algorithm is presented.

It is shown that most advantages of DDS architecture are preserved. The phase truncation problem inherent to DDS architecture is eliminated [9] [10].

Numerical results of the simulations indicate that using the proposed architecture in present FPGA's or ASIC implementation can generate high accuracy and low harmonic signals up to frequencies in the Mhz range .

Future work need to focus on determining the robustness of the new architecture in practical applications like PSK in comparison with classical DDS architectures.

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