Common Mode Problematic of Solar Inverter Systems

K. H. EDELMOSER
Institute of Electrical Drives and Machines
Technical University Vienna
Gusshausstr. 27-29, A-1040 Wien
AUSTRIA

Abstract: - In the medium and high power range (starting from about 5kW) mostly three-phase Solar inverter systems are used. The PWM-systems reduce the harmonics of the mains current but insert a high frequency voltage between the DC-link and the neutral point of the AC-side, which is called common mode disturbance voltage here. This voltage is shown to be a four-level signal whose amplitude is in the range of the DC-link voltage. Its frequency is at least switching frequency and its rate of rise depends on the switching speed of the power semiconductors used. The required switching frequency for low distortion input currents and the resulting switching speed of modern semiconductors lead to excessive earth currents. Especially big solar fields show a considerable ground (earth) capacitance leading to problematic leakage current in DC-slink side. Both countermeasures, the reduction and the short connection of the parasitic earth capacitances (as well as the insertion of a differential inductor in both cases) lead to non trivial resonance problems. The problems are described in detail and a solution is proposed.

Key-Words: - Common Mode Disturbances , Solar Inverter, PWM Inverter

1 Introduction

The traditional B6 inverter system shown in Fig. 1 is investigated exemplarily [1]. The common mode disturbance voltage u_{CM} consists of four levels depending on the switching state only. When all low-side switches conduct, the negative terminal of the DC-bus has ground potential, therefore the voltage u_{CM} becomes + $U_{ZK}/2$. In the opposite case, where all switches conduct to the positive bus, u_{CM} becomes - $U_{ZK}/2$. The source impedance in these cases is obviously given by $Z_I = (R_I + \omega L_I)/3$. Figure 2.a. shows the current path for another case, where two high-side switches and one low-side switch conduct. From the equivalent circuit Figure 2.b. the voltage u_{CM} and its source impedance Z_I are derived.

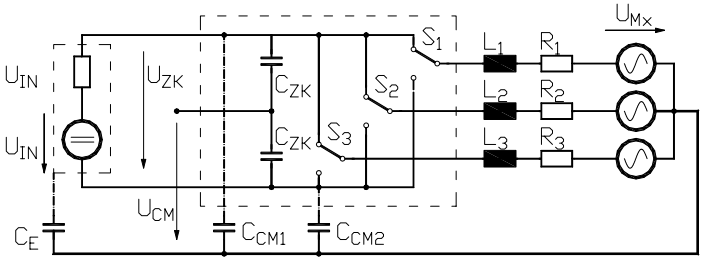

Fig.1. B6 bidirectional FCR system

The DC-link capacitors are taken into consideration with the voltage sources $U_{ZK}/2$ in Fig.2.b. This approach is valid for the switching frequency and higher frequencies. The parallel connected sources u_{M1} and u_{M2} with the source impedances R_I, L_I are replaced by the voltage source $(u_{M1}+u_{M2})/2$ with the source impedance $R_I/2$, $L_I/2$.

According to Fig.2.b. in loop 1 the voltage across the inductor L_I can be calculated to

$$L_I \cdot \frac{di_3}{dt} = \frac{2}{3} \cdot \left(u_{M3} + U_{ZK} - \frac{u_1 + u_2}{2} - i_3 \cdot \frac{3}{2} \cdot R_I \right) \qquad (1)$$

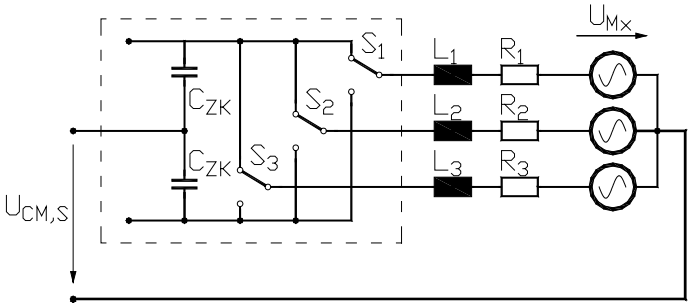

Fig.2.a. Current path for system state 2

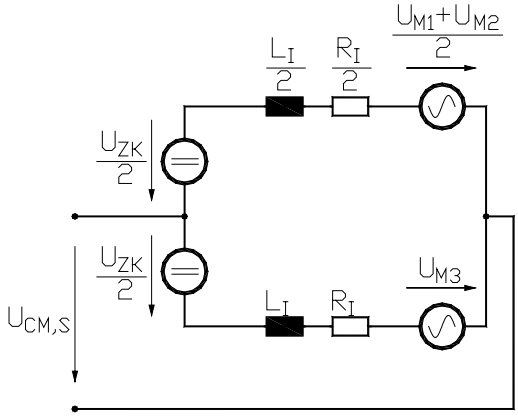

Fig.2.b. equivalent circuit for calculation of $u_{CM,S}$

The disturbance voltage $u_{CM,S}$ is calculated out of the sum of the voltage drops in loop 2.

$$u_{CM,S} = u_3 - R_I \cdot i_3 - L_I \cdot \frac{di_3}{dt} + \frac{U_{ZK}}{2} \tag{2}$$

With (1) the common mode disturbance voltage $u_{CM,S}$ is given by

$$u_{CM,S} = -\frac{U_{ZK}}{6}. \tag{3}$$

The equivalent source impedance in this case also becomes

$$Z_{CM} = \frac{R_I + j\omega \cdot L_I}{3}. \tag{4}$$

Therefore, the source impedance Z_{CM} of the common mode disturbance voltage $u_{CM,S}$ is independent of the switching stages of the inverter. On the other hand, when one high-side switch and two low-side switches conduct, the voltage $u_{CM,S}$ is calculated to

$$u_{CM,S} = +\frac{U_{ZK}}{6}. \tag{5}$$

The switching states of the inverter and the corresponding voltage levels of $u_{CM,S}$ are summarized in table I and visualized in Fig.3.

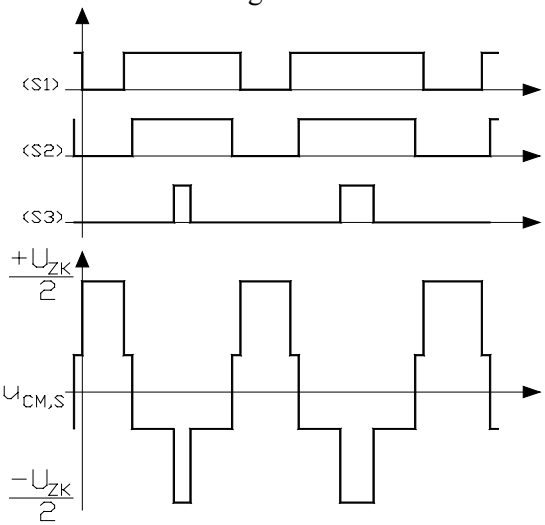

Fig. 3.a. Switching control signals, b. resulting common mode voltage $u_{CM,S}$.

In the inverter-system each switch can either connect the phase inductor to the positive rail (logic 1) or to the negative rail (logic 0). In table I the switching state of the whole system is represented by a line matrix with three columns.

1. $\begin{bmatrix}0 & 0 & 0\end{bmatrix}$ $\quad u_{CM,S} = +\frac{U_{ZK}}{2}$, (6)

2. $\begin{bmatrix}1 & 0 & 0\end{bmatrix}$ $\begin{bmatrix}0 & 1 & 0\end{bmatrix}$ $\begin{bmatrix}0 & 0 & 1\end{bmatrix}$ $\quad u_{CM,S} = +\frac{U_{ZK}}{6}$, (7)

3. $\begin{bmatrix}1 & 1 & 0\end{bmatrix}$ $\begin{bmatrix}1 & 0 & 1\end{bmatrix}$ $\begin{bmatrix}0 & 1 & 1\end{bmatrix}$ $\quad u_{CM,S} = -\frac{U_{ZK}}{6}$, (8)

4. $\begin{bmatrix}1 & 1 & 1\end{bmatrix}$ $\quad u_{CM,S} = -\frac{U_{ZK}}{2}$. (9)

Table I. System states, resulting common mode disturbance voltage

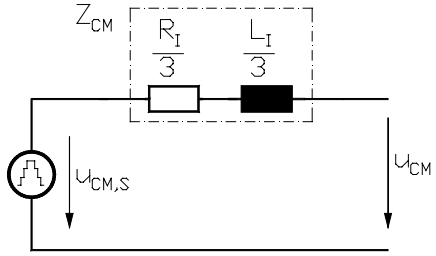

Fig. 4. Resulting equivalent circuit of the inverter ground loop with the common mode disturbance voltage $u_{CM,S}$ and its source impedance Z_{CM}; across the parasitic earth capacitances appears the voltage u_{CM} (floating DC-link); when the DC-link center point is connected to ground (the high frequency harmonics of u_{CM} are shorted and appeared across the line inductors) the low frequency harmonics of u_{CM} appear across the DC-link capacitance 2 * C_{ZK} on the DC-link center point.

1.1. Floating DC-Link Center

In Fig.4, the inverter is reduced to the common mode disturbance source $u_{CM,S}$ with the source impedance Z_{CM}. It can be seen that in the case of floating DC-link the inverter stimulates a series resonant circuit consisting of Z_{CM} and the parasitic earth capacitances. The insertion of an additional differential inductor into the positive and negative bus of the DC-link increases the reactive component $L_I/3$. For a substantial increase of the reactive component of ZCM to reduce the earth current a very large differential inductor is required [3].

Moreover, resonant overshoot is transferred to lower frequencies and lower damping rates of the system result. (In [2], where the problem of the common mode disturbance voltage is addressed, a system with low switching frequency is proposed.)

The voltage u_{CM} contains high switching frequency harmonics in addition to a resonant overshoot. The

additional voltage stress requires high isolation of the converter and the solar array. Therefore in most cases of DC-to-AC inverter topologies (e.g., solar and wind generators), an additional DC-to-DC converter is required for DC isolation and elimination of parasitic earth current. Also, in drive applications [3, 4 & 6] the higher voltage stress leads to higher isolation costs and larger machine sizes. Big solar plants of several kilowatt electrical power, which must be grounded in the center of the DC-link due to isolation problems and their big earth capacitance require a mains coupling transformer with low parasitic capacitances, to eliminate the resonant overshoot. In case of the usage of an active compensation (as shown in this paper), the non trivial resonant problems in conjunction with passive filters and/or ground connection of the DC-link center are avoided. Moreover, in many cases the cost intensive mains transformer can be eliminated.

1.2. Grounded DC-Link Center

If the center of the DC-link is connected to ground, the high frequency harmonics of $u_{CM,S}$ appear additionally on the line inductors. The ripples of the line inductors rise proportionally. The series resonant circuit consists of Z_{CM} and the DC-link capacitance $2*C_{ZK}$ (cf. Figs. 2,4,5) and thus leads to a system with very low resonant frequency.

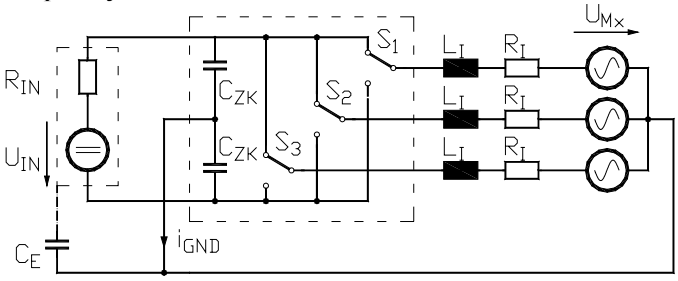

Fig. 5. B6 system with grounded DC-link

Because in this case low frequency stimulations are critical, the DC portion of $u_{CM,S}$ within one period of the switching frequency is calculated. With the equations (6)-(9) and the duty cycles (1, 2 and 3 it is given by

$$\overline{u_{CM,S}} = U_{ZK}\left[\frac{1}{2} - \frac{1}{3}\cdot\left(\alpha_1 + \alpha_2 + \alpha_3\right)\right]. \quad (10)$$

When the modulation

$$\alpha_1 = \frac{1}{2}\cdot\left(1 + \sin(\omega t)\right) \quad (11)$$

$$\alpha_2 = \frac{1}{2}\cdot\left(1 + \sin\left(\omega\cdot t + \frac{2\pi}{3}\right)\right) \quad (12)$$

$$\alpha_3 = \frac{1}{2}\cdot\left(1 + \sin\left(\omega\cdot t + \frac{4\pi}{3}\right)\right) \quad (13)$$

is used, which is depicted in Fig.2a, the DC portion of $u_{CM,S}$ becomes zero. Low frequency harmonics in the power grid may occur [4] due to its high quality Q = Z/R of the resonant earth loop (Z_{CM}, $2C_{ZK}$) and pulse distortions.

In the bought inverter of the laboratory arrangement a different modulation is applied. In order to reduce the switching losses only two branches are switching. The current of the third branch, which remains in the logic 0 or logic 1 position during 60° of the output frequency (cf. Fig.6),is determined by the sum of the phase currents of the switched branches. From Fig.6. one can see, that the not switching branches remain alternatively in the logic 0 or logic 1 position. When it is switched to the negative rail (logic 0) the voltage level $+U_{ZK}/2$ of $u_{CM,S}$ does not appear. Otherwise (not switching branch remains in logic 1 position), $u_{CM,S}$ does not show the voltage level of $-U_{ZK}/2$ (cf. Fig.10.). In this case the resonant circuit is stimulated with only three times the line frequency (active front end) or the output frequency, respectively.

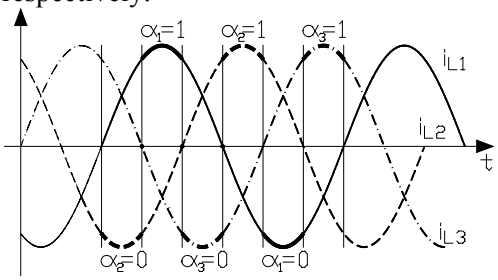

Fig. 6. phase currents and time intervals (fat) of the corresponding non switching branch

It is very important to see, that the low frequency harmonics are not damped or even effected by the regulation of the DC-voltage.

2 A Possible Solution

So far it is shown that the inverter introduces the common mode disturbance voltage $u_{CM,S}$.
In the case of floating DC-link the common mode voltage $u_{CM,S}$ stimulates the high frequency series resonance tank formed by the source impedance and the ground capacitor, in the case of DC-link center shorted to ground a low frequency resonance tank is formed by the source impedance and the DC-link capacitors. conventional output filters have to be dimensioned very carefully and still could lead to additional resonance problems [6]. A possible solution to eliminate the shown resonance problems is the compensation of u_{CM} with the active circuit shown in Fig.7.

The required compensation transformer core has to be designed to operate at switching frequency. On the primary side only the magnetizing and the remaining

ground leakage current (generated by C_{CM1}) have to be taken into consideration. On the secondary side, a wiring for full DC-load current is required. The windings on the secondary are current compensated. The maximum voltage across the secondary windings of the transformer is half the DC-link voltage. This leads to a smaller compensation equipment in relation to output filters.

3 Laboratory Arrangement

The effectiveness of the solution is shown with an AC-Drive system consisting of a 440V DC-source plus external capacitors C_{ZK1} to form the DC-link center point, a bought 1kW inverter with the DC-link capacitors C_{ZK2} and an 2kW load (cf. Fig. 7.).
The earth-capacitance of the motor amounts about 8.4nF. The DC-link center point is connected to ground. The inverter has to be operated with floating engine windings only (see 1.b and floating DC-link when it is supplied from the mains). The output frequency of the inverter was 50Hz and its switching frequency 5kHz. Fig. 8 shows the voltage u_{CM} (channel 1) and the resulting earth current (channel 4). The voltage u_{CM} has a high low-frequency component at three times the output frequency of the inverter due to the change of the switching-state every p/3 of the inactive branch. Fig's. 9. and 10. show the waveforms in between two changes and during one change of the switching state described before.
In Fig. 7. the compensation transformer is put in between the DC-source (C_{ZK1}) and the DC-link of the inverter (C_{ZK2}). Because the inverter starts with an output-frequency near 0Hz, a decoupling capacitor C_M has to be inserted in series to the measurement transformer T_M. Fig. 11. again shows the voltage at the star-point (channel 1), the voltage at the center of the DC-link of the inverter (channel 3) which is not zero yet, and the significantly reduced earth current (channel 4). The difference between channel 1 and channel 3 is the well known voltage u_{CM} shown in Fig's 8.-10. In Fig. 12. the compensation action is clearly visible on channel 3.
The potential on the star-point of the engine (channel 1) does not jump any more due to the inverter switching actions. The superimposed ringing is a result of the series connection of the decoupling capacitor C_M to the measurement transformer T_M.

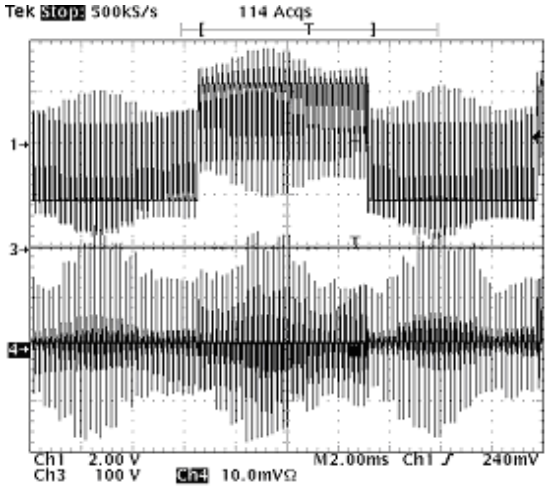

Fig. 8. Uncompensated system; channel 1,3: 200V/div; channel 4: 0.2A/div

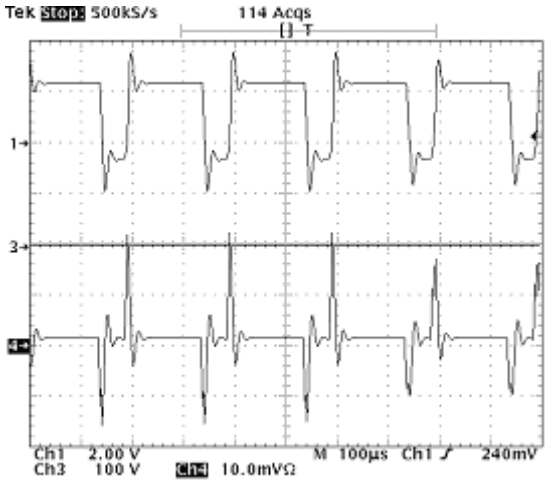

Fig. 9. Uncompensated system, detail; channel 1,3: 200V/div; channel 4: 0.2A/div

When the modulation strategy of equations 11-13 is used, no longer the output frequency of the inverter but its switching frequency only is relevant for the dimensioning of the measurement transformer and the

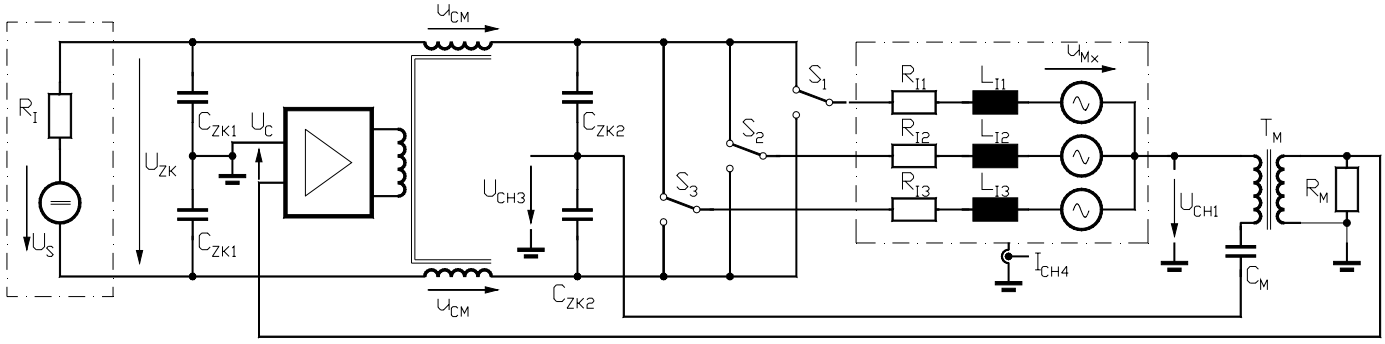

Fig. 7. Laboratory AC-Inverter with compensation circuitry

decoupling capacitor. In this case the decoupling capacitor is theoretically not necessary.

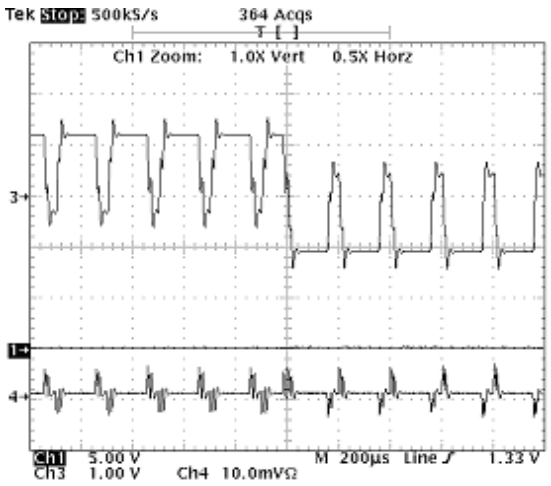

Fig. 10. Uncompensated system; ch. 1: 200V/div; channel 3: 200V/div; channel 4: 0.5A/div

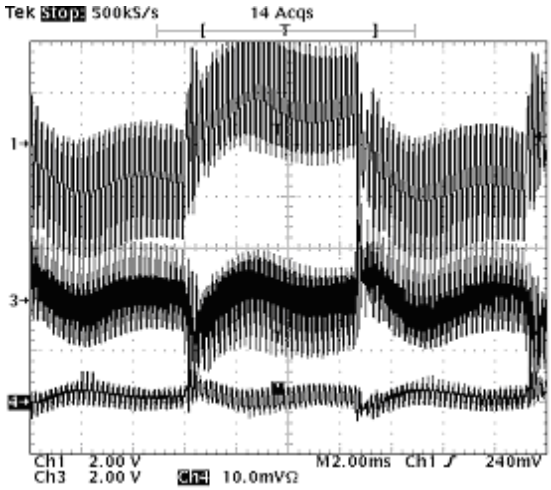

Fig. 11. Compensated system; channel 1,3: 200V/div; channel 4: 0.2A/div

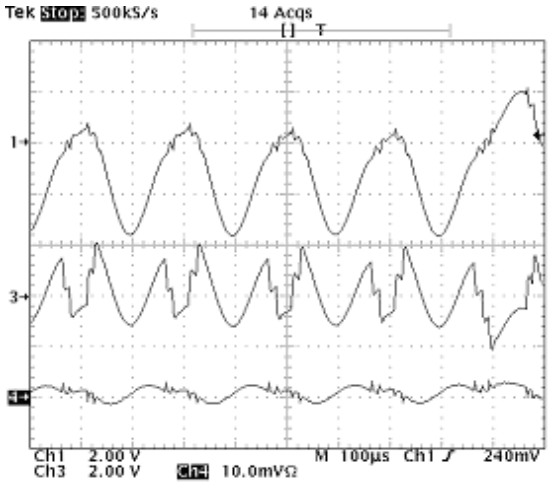

Fig. 12. Compensated system, detail; channel 1,3: 200V/div; channel 4: 0.2A/div

4 Conclusion

Especially in the case of solar and wind energy generation, as well as in AC-motor applications, the high common mode disturbance voltage of conventional systems leads to resonance problems. In the case of the often required floating DC-link center, common mode filtering and high isolation requirements lead to considerable system costs [5]. In many applications, e.g., solar power plants, where the DC-link center is grounded, an additional isolation transformer for the mains connection is required, in order to interrupt the ground current loop. The resulting higher system costs can be avoided by the compensation of the common mode disturbance voltage. The proposed compensation of the common mode disturbance voltage reduces considerably the system costs due to the resonance problems and isolation requirements. Compensation power is required only for covering losses due to nonideal circuit components. It amounts to about one percent of the inverter rating, independent of the output earth capacitance. Especially, Fig's 8. and 12. shows the result of the method proposed here. The earth current is reduced to a fraction of the original value. Furthermore, it should be noted that for idealized components and especially for such modulation of the switching branches where no DC-portion of the common mode disturbance voltage occurs the resulting output noise would be ideally zero.

References:

[1] Y. Chen, K. Smedley, J. Brouwer: "A Cost-effective Three-phase Grid-connected Inverter with Maximum Power Point Tracking" Conference Record of the Forty-First IAS Annual IEEE Industry Applications Conference, Oct. 2006, Volume 2, pp.: 995-1000.

[2] E.L.M. Mehl, I. Barbi: An Improver High Power Factor and Low-Cost Three-Phase Rectifier. IEEE Transactions on Industry Applications, Vol. 33, No. 2, March/April 1997, pp. 485-492

[3] A.H. Bonnet: Available Insulation Systems for PWM Inverter-Fed Motors. IEEE Industry Applications, Vol. 4, No. 1, Jan./Feb. 1998, pp15-26

[4] C.L. Poh, D.G. Holmes, T.A. Lipo: "Implementation and Control of Distributed PWM Cascaded Multilevel Inverters with Minimal Marmonic Distortion and Common-Mode Voltage" IEEE Transactions on Power Electronics, Vol. 20, Issue 1, Jan. 2005, pp.: 90 - 99.

[5] H. Akagi,H. Hasegawa, T. Doumoto: "Design and Performance of a Passive EMI Filter for use with a Voltage-Source PWM Inverter having Sinusoidal Output Voltage and Zero Common-Mode Voltage", IEEE Transactions on Power Electronics, Vol. 19, Issue 4, July 2004, pp.: 1069 - 1076.