Computer-Based Design of Analog Integrated CMOS-Circuits

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Abstract: - In this paper a software design tool is presented that supports the designer in the development process of integrated MOS circuits. Here the general difficulty to find out the right parameter set of all devices in the circuit is split into small device-level tasks, so the designer is able to interactively compute proper *W* & *L* geometries of each single MOS-device. Starting with the common dilemma in the design of integrated analog MOS-circuits with conventional design software, the approach is described to find out the right parameters at transistor-level. Operating point determinations expose some parasitic effects of modern MOS-devices, which complicate the process of design. Using the presented computer-program the designer directly experiences the dependencies of the transistor-parameters and their couplings among each other by interactive modifications of the design variables.

Key-Words: - computer aided design, CAD, electronic design automation, EDA, analog CMOS-circuits, dimensioning, target-oriented design

1 Introduction

Integrated MOS-circuits are composed out of N-MOS and P-MOS transistors. The basic property of a circuit is specified from the interconnection of the MOS-devices themselves. In the next step the channel geometries of all MOS-devices have to be determined to create the concrete circuit function as defined in the circuit specifications. This leads to the electrical properties such as node voltages and branch currents inside the circuitry which generate the designated output value(s) since the circuit has to fulfill its assigned function. Practically every analog MOS-circuit can only be developed by admitting several compromises among conflicting circuit aims such as high precision vs. low power consumption et cetera.

For dimensioning of integrated analog MOS-circuits it is assumed that - if not explicit mentioned - all devices operate in saturation region to ensure correct functioning of the stage. Even if one device is going from saturation to triode or cut-off region, the whole stage no longer acts like a linear circuitry and in the majority of cases it does not function as assumed anymore. E.g. this can occur because of too large signal operation.

Preferable to considering all possible conditions of each device in the stage is to design the dimensions of the channel widths *W* and the channel lengths *L* of the MOS-transistors with high accuracy. Universal approaches for a total automatic design of analog MOS-circuits [1] could not become accepted because of the complexity of this design task. Therefore the approach presented here does not attempt to take over the process of dimensioning the stage on its own, but to support the analog designer best possible in his job to find out the right transistor parameters.

Conventional circuit simulators or IC-development environments indeed provide the design of MOS-circuits at transistor level in a common form indeed, but they do not offer a target-oriented support nor guide the designer in the development process especially of analog circuits e.g. with software assistants.

2 Calculations at device-level

To define the concrete behavior of a MOS-stage the first step is to carry out a sensible planning of the node voltages and branch currents. As long as there are no boundaries specified for node potentials, currents or signal amplitudes, the designer just should aim at certain demands which can be low currents (as possible) or low voltage drops (as possible) on specific significant devices.

On the basis of device-level simulations the designer is able to find out - in respect of the target settings - which aim generally can be reached regarding the applied technology line. For this purpose single electrical or geometrical device parameters have to be set at certain aims whereas in a single simulation step only one selectable parameter is allowed to be changed: via repeated simulation runs the design software tries to iteratively attain the goal or to approach it as far as

possible. In certain circumstances it could even happen that the iteration loop does not end up at its destination, e.g. if the actual design parameter reaches its allowed limits.

The dimensioning has to be done at a single device for its intended operating point. Therefore the program constrains the designer to make serious considerations about important values such as node potentials, currents, voltage limits, conductance, geometries as well as parasitic effects. At the same time it should be checked how far signal amplitudes are limited by the actual dimensioning, e.g. due to channel length modulation. This step is used to maintaining the allowed parameter range of the specified input amplitude in terms of the available voltage drop of the device. Due to this, possible failures which can be caused by the device in later simulations as a part of the total circuitry will be avoided at an early design stage.

After determining all channel widths and lengths with support of the program, typical simulations of the total stage have to be carried out with conventional circuit simulators based on netlists or – more modern – with IC-development environments. As an intermediate step it is often advisable to simulate single branches of the stage first. On this account the simulation results of the total circuitry should be very close to the specifications. Small optimizations can be done with conventional tools if necessary at all. Following this way for the dimensioning of integrated analog MOS-circuits you will get adequate transistor geometries and operating points with even high probability instead of simple setup, repeated simulations, changing parameters and re-simulations for the total stage. In addition to the design procedure described, the possibilities of the applied technology line can be exploited even more.

The geometrical design parameters for the channel width W and the channel length L of a MOS-transistor not only define its electrical properties but rather have an impact on the behavior of the variations in mass-production [2] (cp. section 5). At the moment these dependencies are not covered by the program but will be considered in future versions as long as it makes practical sense. To keep in mind the share of mismatch of a single device is not the same share for all devices relating to the total stage. Every device affects the total output mismatch in a different way which for the most part depends on the internal structure of the circuit. Thus the designer has to decide on his own on which transistor he needs to spend more considerations in terms of mismatch. This property only appears from the context of the circuit. To get a coarse hint about the mismatch behavior of a single transistor with short computation times, sensitivities of its parameters have to be calculated.

3 Parasitic Effects of MOS-Transistors

As a consequence of progressive shrinking the geometrical dimensions of modern MOS-devices the designer has to cope with more and more difficulties to develop integrated circuits. The characteristic curves of current MOS-models show major differences to ideal MOS-characteristics due to highly cumulative parasitic effects. Not only so-called short-channel-effects but also fundamental parameter dependencies let the design of integrated analog MOS-circuits become confusing. In the following sections some of the significant effects are discussed which make the characteristic curves differ from the ideal MOS-model.

3.1 Channel Length Modulation

While an ideal MOS-output-characteristic in saturation region does not exhibit a dependence of the drain current I_D on the drain-source voltage V_{DS}, this has changed with decreasing minimum feature sizes to a noticeable and non-linear current-boost: $I_D = f(V_{DS})$ (Fig. 1).

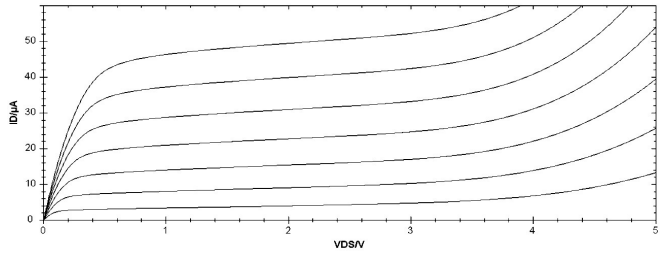

Fig. 1: typical N-MOS-output-characteristic

Measured characteristic curves of ultra-modern MOS-devices with feature sizes in the deep nanometer region [3] show such big differences to the ideal characteristics that a saturation region almost cannot be identified in their output-curves.

3.2 Threshold Voltage Displacement

The threshold voltage V_{Th} of MOS-transistors is not a constant value but a function of the source-bulk voltage V_{SB} which varies under operating conditions. Additionally, there is a dependence of V_{Th} on the ambient temperature T and the drain-source voltage V_{DS}. Values of the zero-field-threshold voltage V_{T0} can be taken from the design rules for the available types of transistors. From this the effective threshold voltage V_{Th} can be calculated in dependence of the parameters mentioned above. Often it is not noted which method was used when acquiring the zero-field-threshold voltage V_{T0}. It is often vague as well for which operation region of the MOS-device – triode region or saturation – the declared voltage is intended.

When a transistor is dimensioned with the help of a circuit simulator the designer does not need to take into consideration the exact value for the displacement of V_{Th}, because the simulator computes the effective threshold voltage V_{Th} on the basis of the underlying transistor-model and the specified operation point potentials. Nowadays the BSIM3V3-model is used in the majority of cases in CMOS-technology. Its complexity can be quoted by the equation for the calculation of the threshold voltage V_{Th} which is an expression of several lines [4]. In the graphical user interface of the proposed program the current value of V_{Th} is updated on every change of other parameters, therefore the designer can react to changes of V_{Th} when he is gathering for the right W & L values. Mostly this occurs after changing the substrate voltage V_{SB} which has the biggest impact on the displacement of V_{Th} but also when dimensioning simple MOS-stages like level shifters.

In conjunction with the threshold voltage V_{Th} the effective-gate voltage V_{Geff} is a very important parameter for the operating point when designing analog MOS-circuits: $V_{Geff} = V_{GS} - V_{Th}$. This value is also updated in the user interface of the program on every change, because it represents the effective condition of the channel. Fig. 3 shows an editable value for V_{Geff} as it can be calculated directly from the gate-source voltage V_{GS} via V_{Th}. Thus the designer only needs to consider V_{Geff} whereas the program makes the required modifications on V_{GS} in dependence on the current value for V_{Th}.

3.3 Drain Induced Barrier Lowering

Drain-induced barrier-lowering is a synonym used for the parasitic effect of the dependence of the threshold voltage V_{Th} on the drain-source voltage V_{DS}. This interconnection is taken into account in current MOS-models like BSIM3V3 [4].

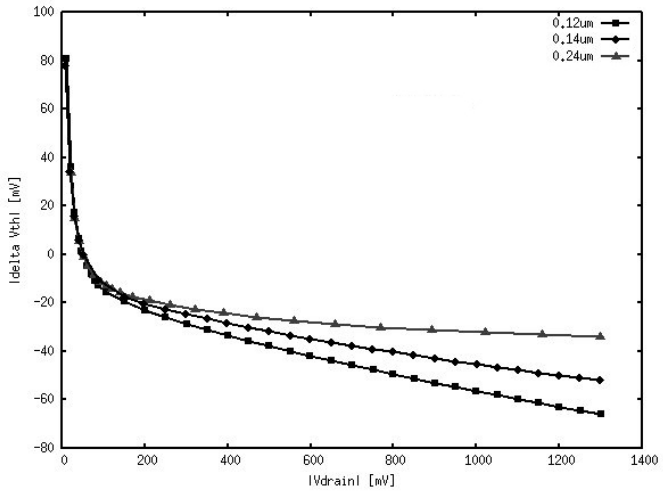

Fig. 2: dependence of V_{Th} on V_{DS} [5]

Analyses of this effect on MOS-transistors with different channel lengths [5] show an additional dependence of the threshold voltage V_{Th} on the channel length L (Fig. 2). In the presented software tool this effect is also transparent to the designer since it is resolved by an appropriate MOS-model.

3.4 Temperature Range

In the specifications of an integrated analog circuit mostly a safe operating area is set which defines the lowest and highest ambient temperature of the chip. At room temperature simulations of conventional designed MOS-circuits often show still adequate signal properties, but with temperature increasing to the specified edge some of the output signals already drifted out of their intended range. In detail particularly the threshold voltage V_{Th}, the drain current I_D as well as the saturation voltage V_{Dsat} exhibit a strong dependence on the operating temperature for MOS-transistors. However, dimensioning a single MOS-device with support of the proposed design tool parameter drifts of highly temperature sensible elements can be identified at early development stage via quick interactive temperature variations.

3.5 Saturation

Most of analog MOS-circuits are based on the independence of the drain current I_D on the drain-source voltage V_{DS} for each of its elements, which means that the drain current does not change on variations of V_{DS}. This is the ideal behavior of a MOS-transistor when it is driven in saturation region. In this mode I_D primarily is a function of the gate-source voltage V_{GS}, thus the transistor has the purpose of a voltage controlled current source. For this operating mode it is required that $V_{DS} > V_{GS} - V_{Th}$ (saturation constraint). In a linear circuit all components have to accomplish this constraint. Even if a single transistor is leaving its intended saturation region the total stage can show unintended signal behavior. Therefore it is very important to consider the entire voltage amplitude of each transistor already at early stage of design.

Circuit simulators such as SPICE and its modern derivates can compute the saturation voltage V_{Dsat} of a MOS-device much more precise than the saturation constraint mentioned before. Just like other parameters the current value for V_{Dsat} is updated on every user activity in the proposed program (Fig. 3). Here a red marked V_{Dsat} value signals that the transistor is currently not in saturation region. Additionally, a vertical line in the output characteristic graphically shows this value as well as the current value for V_{DS} which is marked with a big dot on the output curve. At a glance the designer can see if his changes break the saturation constraint.

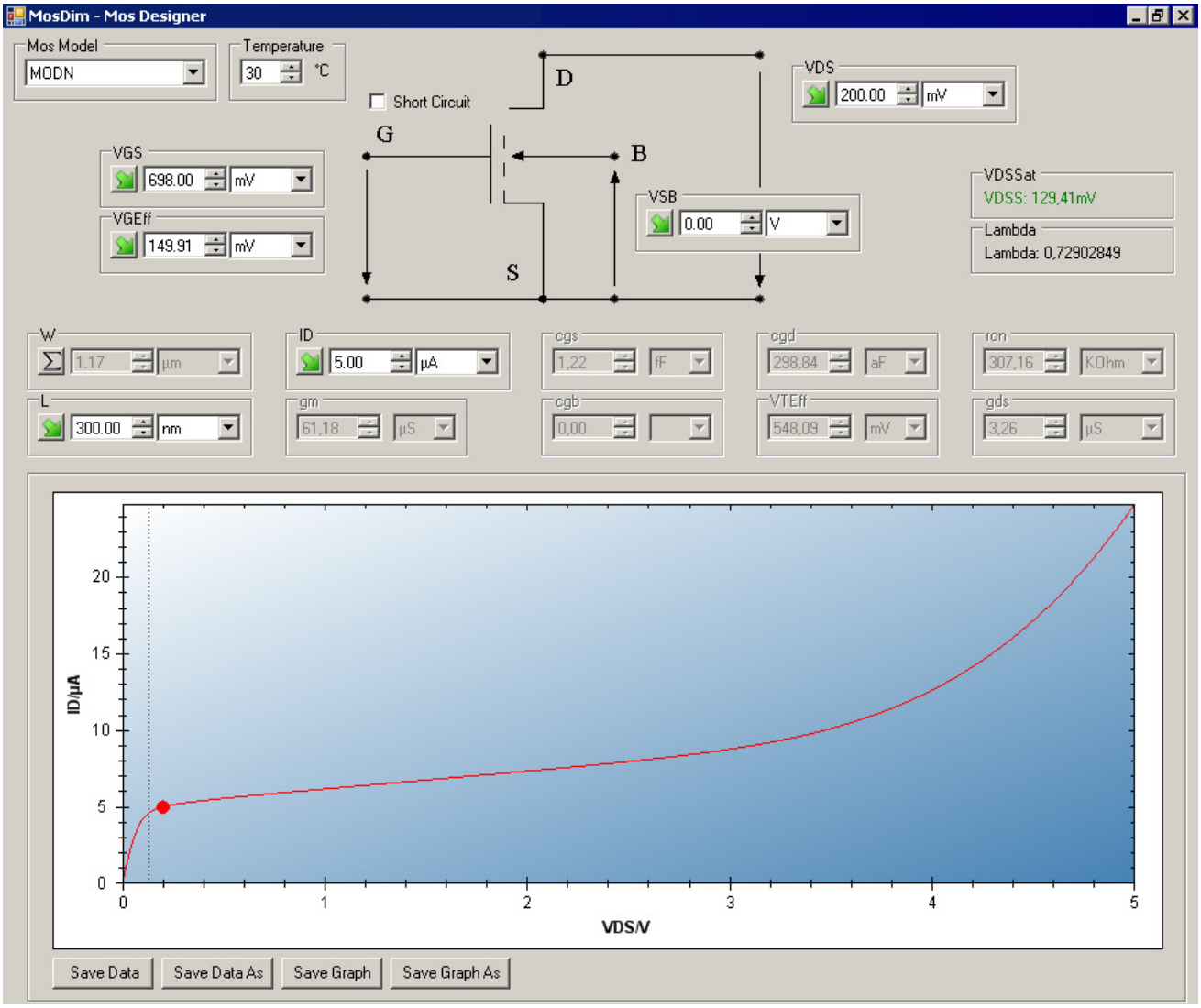

Fig. 3: user interface of the main window for interactive calculations of single MOS-transistors

As this is one of the most important demands in analog MOS-design, the program offers a value-based and a graphic-based possibility to check the operating condition of the current MOS-device. Since the saturation voltage V_{Dsat} is not a constant value, the position of its line is updated on every user action as well, e.g. by changing the gate-source voltage V_{GS}, the drain-source voltage V_{DS}, the channel length L, the temperature T or indirectly by changing the threshold voltage V_{Th}.

4 User Interface of the Design Tool

As mentioned in section 3, multiple couplings of the transistor parameters among each other should emphasize the complexity of the design of integrated analog MOS-circuits. Using conventional development software the designer is asked for a high level of experience to pre-estimate all of the parameters and afterwards optimize them. On the other hand the dimensioning of a single transistor with conventional software needs very circumstantially and tedious inputs. To put things right the graphical design tool shown in Fig. 3 was developed for accurate dimensioning of a single MOS-transistor or MOS-diode (gate-drain short-circuited MOS-transistor). It creates a user interface between the designer and input/output of the text-based circuit simulator. It is intended to be invoked from the schematic view of an IC-development environment as it needs the parameter set. At the moment the design tool still is a stand-alone program, thus the parameter set, the underlying simulator, default values for transistors and other configuration parameters have to be set in its configuration setup window (Fig. 4).

The interactive user interface provides a comfortable and target-oriented way to find out the right dimensions of MOS-transistors for their intended role inside the stage. Important parameter values like V_{Th} or V_{Dsat} are computed via an appropriate simulator in the background, then displayed instantaneously, and hence can be considered by the designer to interactively dimension

the device. At this the allowed geometrical resolution for W & L is comprised automatically. On modern computer systems the calculation time of a single MOS-device is negligibly short, so the feedback regarding input changes can be displayed almost in real-time (iterative approximations can entail several simulator calls depending on the current design task).

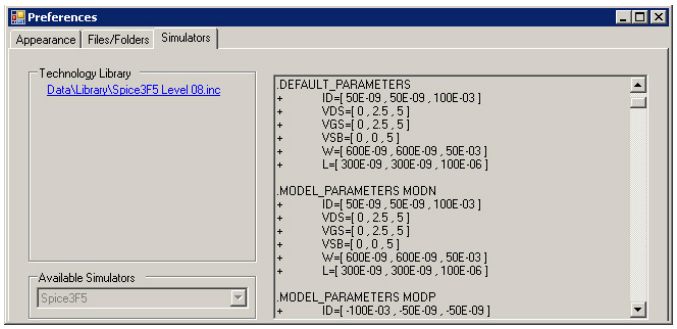

Fig. 4: general configuration, selection of parameter set and simulator

The program code was constructed to be as flexible as possible for almost all combinations of parameter sets and their intended circuit simulator. So no changes on the code of the program are required on most of available circuit simulators. Through this it is also ensured that calculations of the program fit to subsequent simulations of the total stage, since all calculations are executed with the same simulator and with the same parameter set or technology line respectively. For this reason operating point data obtained from the proposed design tool are a good origin for minor optimizations in conventional simulations of the total circuit.

As it appears from Fig. 3 the designer can directly modify the following values: the gate-source voltage V_{GS}, the effective gate voltage V_{Geff}, the drain-source voltage V_{DS}, the substrate voltage V_{SB}, the channel width W, the channel length L, the drain current I_D, the operating temperature T and the type of MOS-transistor (e.g. N-MOS, P-MOS, with thin or thick gate-oxide according to the available devices in the parameter set). Additionally, all of the non-directly adjustable values are updated on every parameter change like: the saturation voltage V_{Dsat}, the channel-length-modulation factor λ, the effective threshold voltage V_{Th}, the transconductance g_m, the channel conductance g_{ds}, the on-resistance r_{ON}, the gate-source capacitance C_{GS}, the gate-drain capacitance C_{GD} and the gate-substrate capacitance C_{GB}.

In the diagram of Fig. 3 a simulated curve of the output characteristic is shown depending on the current transistor parameters. The current values for V_{DS} (marked on the curve), V_{Dsat} (shown as a vertical line) and the unwanted increase of the drain current due to channel-length-modulation are displayed as well.
One single parameter of the adjustable values can be selected as the one to be computed depending on the current values of the other parameter. Its symbol then is changed to a sigma sign and its input box turns to light gray (as in Fig. 3 the channel width W) whereas the other tunable parameters are depicted with an arrow for reasons of better overview. If an adjustable parameter is changed per increase, decrease or via direct input of its value, the program determines the unknown value via iterations in the background and displays the new values for all parameters. Through this the designer is able to keep track of them all. If a MOS-diode (built out of a gate-drain short-circuited transistor) has to be calculated, the check-button "short circuit" has to be selected (which results in a slightly different input form).

5 Conclusion

The design of integrated analog MOS-circuits is an exhausting process using conventional IC-development environments. The design tool presented in this article changes the direction of how parameters have to be determined, so that, via its graphical user interface, it is possible to directly modify any value and keep track of its impact on other parameters. This is displayed both as data and by a diagram which facilitates and accelerates the dimensioning process in all.

For the design of current and upcoming nanometer devices it is important to resolve any parameter dependencies and parasitic effects, since by scaling down channel geometries these parasitic effects will increase above average - most notably channel-length-modulation. It is obvious that the impact on the relative changes of the transistor's channel-lengths related to its absolute size has a strong and growing influence in each step of scaling down geometries.

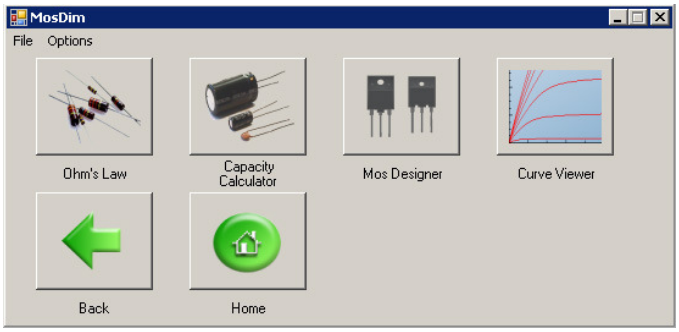

Fig. 5: selectable calculators for different device types

This design tool can be compared to an electronic calculator for MOS-transistors. Beyond this it also offers

interface forms for other design tasks like calculating capacitances or just resistors (Fig. 5).

There are further dependencies in the design of modern MOS-circuits that are currently not supported by the program but nevertheless are important to be considered like examinations of frequency behaviour, parameter sensitivities, noise or statistical parameter variations due to manufacturing process [2]. However, in future versions of the program not only operating point calculations are to be accomplished but also estimations about the expected yield of the manufactured circuit.

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