Worst Case Analysis of the Analog Circuits

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Abstract: - An approach of the worst case analysis of the analog electronic circuits based on the circuit description in parameter space is proposed. A DC, AC or transient worst-case analysis can be performed only testing the circuit for the vertices of a polytope in conjunction with a circuit simulator or computational environment. In order to validate and show the effectiveness of this approach, DC worst-case analyses of analog electronic circuits with symmetrical and asymmetrical tolerances in conjunction with a general-purpose circuit simulator are presented and discussed.

Key-Words: - Tolerance, Analog electronic circuit, Worst case analysis.

1 Introduction

The behaviour of a circuit is affected when certain parameters in specific components change. Circuit simulators like SPICE can perform many analyses of the analog and digital circuits that highlight the change effects of the parameter values on the circuit performance. The worst case analysis lets us explore the worst possible effects of variations in component parameters on the performance of a circuit. Simulators like SPICE perform the Worst Case Analysis in conjunction with a DC or AC analysis. The worst case analysis results refer to the worst case values at the circuit outputs and performance specifications produced when a circuit component or device model change its parameter value [1]-[3]. Such an analysis is based on the sensitivity analysis [4]. Some circuit simulators perform the sensitivity analysis for the model parameters of the active devices such as BTJs, FETs and integrated amplifiers meanwhile others do not.

Automated fault detection for analog circuits is subject to specific problems, such as the unknown deviation in tolerances of nonfaulty component values, the location of soft faults and the presence of noise. The techniques for soft fault diagnosis in analog electronic circuits are based on the simulation before test, approach where a fault dictionary is a priori generated by collecting signatures of different fault conditions [5]-[8]. Worst case analysis can be considered as a step in the stress analysis or in the soft-fault diagnosis allowing us to find out the bound outputs or performance specifications of a circuit.

A method for studying the worst case of the outputs and performance specifications of the analog circuits that is not based on sensitivity analysis can be derived utilizing the circuit description in parameter space.

The paper is organized as follows. The analog circuit description in the parameter space by a polytope is given in Section 2. In Section 3, the problem formulation of the worst-case analysis based on aforementioned circuit description is presented. Then, in Section 4, we show how to implement and validate the proposed procedure using a circuit simulator where the sensitivity analysis for the model parameters of the active devices is not available. Two case studies are presented and discussed using a small-signal amplifier with JFET as example, in order to illustrate the proposed procedure and to demonstrate its effectiveness. Section 5 concludes the paper.

2 Circuit Description

2.1 Circuits with symmetrical tolerances

The concept of the circuit design approach and tolerance selection, based on the floating and expanding polytope, has been proposed by Bandler for an optimal design of the nominal parameter values of the circuit and tolerances [9]. This concept is appliable to the circuits with symmetrical tolerances such as those of the passive components [8].

Briefly, we resume this theorem looking for the circuit description as follows. Let us consider $\mathbf{\Phi} = [\Phi_1 \ \Phi_2 \ \ldots \ \Phi_k]^T$ a vector with k elements that

correspond to the parameter circuit values. This vector has a correspondent point $\boldsymbol{P}(\Phi_1\ \Phi_2\ ...\ \Phi_k)$ in the k-dimensional space of parameters. The nominal point $\boldsymbol{P^0}=\left(\Phi_1^0\ \ \Phi_2^0\ ..\ \Phi_k^0\right)$ corresponds to $\Phi^0=\left[\Phi_1^0\ \ \Phi_2^0\ ..\ \Phi_k^0\right]^T$ the vector of the parameter nominal values) and is associated with a non-negative tolerance set $\varepsilon=\left[\varepsilon_1\ \ \varepsilon_2\ ..\ \varepsilon_k\right]^T$. The tolerance region $\Re_t$, in the parameter space, is given as

$$\Re_t=\left\{P\middle|\Phi_i^0-\varepsilon_i\le\Phi_i\le\Phi_i^0+\varepsilon_i, i\in I_\Phi\right\} \quad (1)$$

where $I_\Phi=\{1,2,...k\}$.

The tolerance region $\Re_t$ is a k-dimensional convex regular polytope, centered at P^0, in the k-dimensional space of parameters, and $2\varepsilon_i$, $i\in I_\Phi$, is the length of the i side of this polytope. The polytope has 2^k vertices, which are the extreme points of $\Re_t$. Then, the set of vertices can be defined as

$$\Re_v=\left\{P\middle|\Phi_i=\Phi_i^0+\varepsilon_i\mu_i, \mu_i=\pm1, i\in I_\Phi\right\}. \quad (2)$$

The number of points contained by $\Re_v$ is 2^k: $\Re_v=\left\{P^1\ \ P^2\ \ ..\ \ P^{2^k}\right\}$. These points are indexed by P^i, $i\in I_v$, $I_v=\left\{1,2,...,2^k\right\}$. Looking for an optimal design of circuit, an accepted region $\Re_a$ is defined and it is demonstrated that if $\Re_v\subseteq\Re_a$, then $\Re_t\subseteq\Re_a$. According to this theorem, only the polytope vertices must be tested to be sure that $\Re_t\subseteq\Re_a$.

1.2 Circuits with asymmetrical tolerances

The operating characteristics of active devices and analog integrated circuits are often unpredictable because of their internal geometric dependence. We can create component models that more closely represent actual real world devices by converting measurement or catalog data into model parameters by means of various tools type parameter extractor. Usually, the model parameter range of a device lot is not centered at nominal values of the model parameters of a given device sample. The spread of the parameter values due to the manufacturing process and temperature effects are generating sources of asymmetrical tolerances of the parameters. Also, the deviations of the supply voltages can be asymmetrical with rapport to their nominal values.

This problem of the analog circuits with asymmetrical tolerances becomes easy to solve if the asymmetrical tolerance case can be reduced to that of the symmetrical tolerance case. In order to solve this kind problem, the polytope with averaged-nominal point was defined and its equivalence with the polytope with symmetrical tolerance was demonstrated [10].

We supposed that the nominal point is $\{\Phi_{0i}\}$ with $i\in I_\Phi$, the positive tolerances ε_{pi} and ε_{ni} are lop-sided, i.e. there is $i_0\in I_\Phi$ for which $\varepsilon_{pi_0}\ne\varepsilon_{pi_0}$. Some tolerances can be symmetrical. Now, the tolerance region is

$$\Re_t=\left\{P\middle|\Phi_{0i}-\varepsilon_{ni}\le\Phi_i\le\Phi_{0i}+\varepsilon_{pi}, i\in I_\Phi\right\}. \quad (3)$$

The tolerance region $\Re_t$ is a k-dimensional polytope with side i of $(\varepsilon_{pi}+\varepsilon_{ni})$ length, $i\in I_\Phi$, and with 2^k vertices. We replaced the nominal point Φ_i^0 of the polytope $\Re_t$ with the averaged-nominal point Φ_{mi}^0, where

$$\Phi_{mi}^0=\Phi_{0i}+\frac{\varepsilon_{pi}-\varepsilon_{ni}}{2}, \quad (4)$$

and we denote the mean values of tolerances, i.e. the symmetrical tolerances,

$$\varepsilon_{mi}=\frac{\varepsilon_{pi}+\varepsilon_{ni}}{2}\ \text{ for all } i\in I_\Phi. \quad (5)$$

Then, we demonstrated

$$\Re_{mt}=\left\{\begin{matrix}P\middle|\Phi_{mi}^0-\varepsilon_{mi}\le\Phi_i\le\Phi_{mi}^0+\varepsilon_{mi},\\ for\quad all\quad i\in I_\Phi\end{matrix}\right\}=\Re_t. \quad (6)$$

Replacing the polytope with asymmetrical tolerances with its equivalent polytope with symmetrical tolerances allows us to apply the Bandler's theorem to an analog circuit with asymmetrical tolerances.

3 Worst Case Analysis

An analog circuit can be described in the parameter space by a polytope, i.e. $\Re_t$ or $\Re_{mt}$, of which vertices represent the extreme values of parameters. A DC, AC or transient analysis performed for the vertices of the polytope $\Re_t$ will produce corresponding value bands of the circuit outputs or performance specifications. The bounds of these value bands represent the worst case values of the circuit outputs or performance specifications.

Consider a circuit of k parameters, $\boldsymbol{P}$ = [p_1, p_2, ...,p_k], where p_i may be the resistance of a resistor, the capacitance of a capacitor, the β transconductance parameter or W/L ratio of a FET, the V_{th} threshold voltage, the λ channel length

modulation coefficient etc. The circuit parameters have the nominal values $\boldsymbol{P_0} = [p_{01}, p_{02}, ..., p_{0k}]$ and the tolerances $\varepsilon = [\varepsilon_{p1}, \varepsilon_{n1}, \varepsilon_{p2}, \varepsilon_{n2}, \ldots \varepsilon_{pk}, \varepsilon_{nk}]$. Some tolerances can be symmetrical, i.e. $\varepsilon_{pj} = \varepsilon_{nj} = \varepsilon_j$.

Let be the polytope $\Re_{\text{mt}}$ with the averaged nominal point

$$P_{mi}^0 = p_{0i} + \left(\varepsilon_{pi} - \varepsilon_{ni}\right)/2 \quad (7)$$

and the tolerances

$$\varepsilon_{mi} = \left(\varepsilon_{pi} + \varepsilon_{ni}\right)/2 \text{, with } i = 1,\ldots, k. \quad (8)$$

The vertices of the set $\Re_{mt} = \left\{P_m^l\right\}$, where $l = 1,., 2^k$, are denoted as follows:

$$P_m^1 = \begin{bmatrix} p_{m1}^0 - \varepsilon_{m1} \\ p_{m2}^0 - \varepsilon_{m2} \\ .... \\ p_{mk}^0 - \varepsilon_{mk} \end{bmatrix}, \; P_m^2 = \begin{bmatrix} p_{m1}^0 + \varepsilon_{m1} \\ p_{m2}^0 - \varepsilon_{m2} \\ .... \\ p_{mk}^0 - \varepsilon_{mk} \end{bmatrix},$$

$$P_m^3 = \begin{bmatrix} p_{m1}^0 - \varepsilon_{m1} \\ p_{m2}^0 + \varepsilon_{m2} \\ .... \\ p_{mk}^0 - \varepsilon_{mk} \end{bmatrix}, .., P_m^{2^k} = \begin{bmatrix} p_{m1}^0 + \varepsilon_{m1} \\ p_{m2}^0 + \varepsilon_{m2} \\ .... \\ p_{mk}^0 + \varepsilon_{mk} \end{bmatrix}. \quad (9)$$

We suppose that the behaviour of the circuit is characterized by m circuit outputs $\boldsymbol{y} = [y_1, y_2, \ldots, y_m]$ and n performance specifications, $\boldsymbol{S} = [s_1, s_2, \ldots, s_n]$. The circuit DC outputs $\boldsymbol{Y} = [Y_1, Y_2, \ldots, Y_m]$ are DC voltages of nodes or DC currents through circuit branches that describe the DC operating point of circuit. A transient analysis yields the circuit outputs $\boldsymbol{y}(t) = [y_1(t), y_2(t), \ldots, y_m(t)]$. A circuit output, for example the r-th output, or a performance specification, for example the t-th output, can be represented as a function of all parameters, i.e.

$$y_r = f(p_1, p_2, ..., p_k) \text{ and } s_t = f(p_1, p_2, ..., p_k). \quad (10)$$

Regardless of symmetrical or asymmetrical tolerance case, the circuit outputs and performance specifications at nominal values of parameters will be $\boldsymbol{y_0} = [y_1(\boldsymbol{P_0}), y_2(\boldsymbol{P_0}), \ldots, y_m(\boldsymbol{P_0})]$ and $\boldsymbol{S_0} = [s_1(\boldsymbol{P_0}), s_2(\boldsymbol{P_0}), \ldots, s_n(\boldsymbol{P_0})]$. Each output and performance specification of a circuit is expressed by a value or a curve at nominal point in parameter space.

Considering the variations in the parameter space and testing the circuit for the polytope vertices, there will correspondingly be variation in the circuit outputs and specifications:

$$\boldsymbol{y}(\boldsymbol{P_m^l}) = [y_1(\boldsymbol{P_m^l}), y_2(\boldsymbol{P_m^l}), \ldots, y_m(\boldsymbol{P_m^l})], \quad (11)$$

$$\boldsymbol{S}(\boldsymbol{P_m^l}) = [s_1(\boldsymbol{P_m^l}), s_2(\boldsymbol{P_m^l}), \ldots, s_n(\boldsymbol{P_m^l})]. \quad (12)$$

The relationships between a circuit output or performance specification and the parameters will become a band instead of a single curve. So, the circuit output y_r is bounded by y_{rmin} and y_{rmax}, the performance specification s_t is bounded by s_{tmin} and s_{tmax}: $y_{rmin} \le y_r \le y_{rmax}$ and $s_{tmin} \le s_t \le s_{tmax}$. The bounds y_{rmin} and y_{rmax}, s_{tmin} and s_{tmax} are the worst values of circuit outputs and performance specifications for a worst-case analysis. For a fault detection problem, the same bounds delimit the operation of the fault-free circuit. The upper bound of a circuit output can be looked as stress analysis result.

This procedure is not based on the sensitivity analysis and it can be implemented in conjunction with a circuit simulator or computational environment (Matlab, Mathcad, Mathematica etc.) when an appropriate model of the device/circuit is available. As it will shown in the following, this procedure can be applied for the worst case analysis of the analog circuits with symmetrical and/or asymmetrical tolerances.

4 Procedure Validation. Case Studies

Using a general-purpose circuit simulator, we will show how to implement and validate the proposed procedure. The circuit simulator is used to perform the DC Operating Point Analysis of the circuit for the polytope vertices. In order to verify the proposed procedure for the worst-case analysis of an analog circuit, its results will be compared with those produced by the DC worst case analysis allowed by the circuit simulator and an experimental setup. For this purpose, we consider a small-signal amplifier with a NJFET type BFW11. The circuit diagram of the test circuit is shown in Fig. 1.

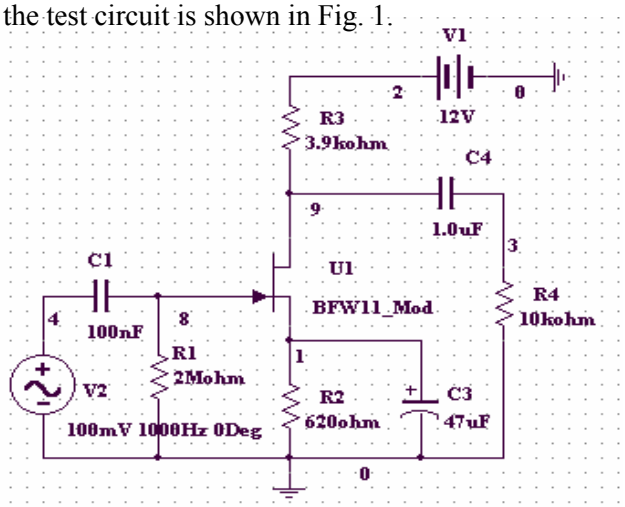

Fig. 1. Circuit diagram of the small-signal amplifier with JFET type BFW11_Mod

Firstly, we consider the circuit with symmetrical tolerances of two resistors in circuit and perform the

DC worst case analysis based on the dedicated menu of simulator and our procedure. Secondly, the bounds of the parameter dispersion of the transistor at constant temperature are taken into account as asymmetrical tolerances of circuit with rapport to a JFET sample.

Our NJFET sample type BFW11 was chosen from a lot of ten transistors for which the characteristic curves were measured. We extracted the threshold voltage, nominal saturation current and output conductance of each transistor from its characteristic curves. Then, converting the measurement data, we created a device model. Such a model has been created for three devices namely: NJFET sample and two NJFETs of which characteristic curves represent the lot dispersion. For the NJFET sample model, we find out the following parameters: V_{T0} (V) = - 2 (threshold voltage), β (mA/V^2) = 1.24685 (transconductance parameter) and λ (V^{-1}) = 0.0246 (channel length modulation coefficient). The rest of model parameters holds the values set for the NJFET type BFW11 contained by the Master Database of the circuit simulator. The new device with its model was saved in User Database as a component named BFW11_Mod. The bias circuit was designed to set the DC operating point into the active forward region with the following nominal coordinates: $I_{DQ} \cong 1.5$ mA, $V_{GSQ} \cong -1$ V and $V_{DSQ} \cong 6$ V. Consequently, we obtain the following values of resistances: R_1 = 2 MΩ, R_2 = 620 Ω and R_3 = 3.9 kΩ. The tolerance of all the passive components have a tolerance of ±5%. We consider a constant temperature (27^{o}C), for the sake of brevity and a better match of the measurement and simulation conditions.

4.1 Worst case analysis of an analog circuit with symmetrical tolerances

At this point, the effects of the model parameter tolerances are not considered. Looking for DC worst case analysis of the given circuit, we consider only the effects of variations of two resistive parameters on the voltages of drain and source nodes ($Y1$ = V9 and $Y2$ = V1) and the supply branch current ($Y3$ = vv1#branch = I_D) are taken into account. So, the circuit parameters are as follows: $p_1 = R_2$, p_{10} = 620 Ω, ε_1 = 31 Ω; $p_2 = R_3$, p_{20} = 3.9 kΩ , ε_2 = 195 Ω.

The verification process of proposed procedure has four steps as follows:

1. The circuit from the Fig. 1 is simulated for the DC worst case analysis using the aforementioned tolerances, i.e. ε_1 and ε_2. The analysis results are shown in Table 1.

2. In order to find out the bounds of the specified circuit outputs, the R_2 and R_3 parameter values are modified according to each vertex of polytope. Then, the new circuit is simulated for perfoming the DC Operating Point Analysis. The polytope with symmetrical tolerances are four vertices:

$$\boldsymbol{P}^1 = \begin{bmatrix} 589 \\ 3705 \end{bmatrix}; \boldsymbol{P}^2 = \begin{bmatrix} 651 \\ 3705 \end{bmatrix}; \boldsymbol{P}^3 = \begin{bmatrix} 589 \\ 4095 \end{bmatrix};$$

$$\boldsymbol{P}^4 = \begin{bmatrix} 651 \\ 4095 \end{bmatrix}.$$

The analysis results are also given in Table 1.

Table 1. The results of the worst case analysis performed with the dedicated menu of a circuit simulator, proposed technique and experimental setup

Approach		DC circuit outputs		
		Y_1(V)	Y_2(V)	Y_3(mA)
DC WCA menu		6.4647	0.97259	1.48777
Polytope vertices	$\boldsymbol{P}^1$	6.21161	0.9202	**1.56232**
	$\boldsymbol{P}^2$	**6.55433**	**0.95685**	1.46982
	$\boldsymbol{P}^3$	**5.63123**	**0.91604**	1.5552
	$\boldsymbol{P}^4$	6.00551	0.95297	**1.46386**
Experi-mental	$\boldsymbol{P}^1$	6.24147	0.91545	**1.55426**
	$\boldsymbol{P}^2$	**6.58225**	**0.95194**	1.46228
	$\boldsymbol{P}^3$	**5.6643**	**0.91128**	1.54718
	$\boldsymbol{P}^4$	6.03643	0.94805	**1.4563**

3. The three DC outputs of the circuit constructed with the NJFET sample for the four pairs of values of resistances R_2 and R_3 are measured. The experimental results are given in Table 1 too.

4. Comparison between the results of the worst case analysis performed with the dedicated menu of a circuit simulator, proposed technique based on the testing of the polytope vertices, and experimental setup show the following:

a. The worst case analysis performed by means of the dedicated menu of simulator provides an only value for each DC output of circuit: $Y_{1w.c.a}$ (V) = 6.4647, $Y_{2w.c.a.}$ (V) = 0.97259, $Y_{3w.c.a.}$ (mA) = 1.48777. The supplementary index marks the worst case value (w.c.a.) of DC outputs.

b. The proposed technique provides a value band for each DC output of circuit. The minimum and maximum values of each band (bolded in Table 1) represent the results of the worst case analysis based on testing the circuit for the polytope vertices.

c. The worst case values of the DC circuit outputs supplied by dedicated menu of the simulator are nearly recovered for the $\boldsymbol{P^2}$ vertex of polytope.
d. The two value bands of the DC outputs and their bounds from the experimental results are nearly the same as that obtained utilizing the proposed procedure.

4.2 Worst case analysis of an analog circuit with asymmetrical tolerances

In this section, we will illustrate how to apply the proposed procedure on a circuit with some asymmetrical tolerances by means of a circuit simulator. The asymmetrical tolerances describe the NJFET lot dispersion with rapport to NJFET sample. In our circuit simulator version, the sensitivity analysis and consequently the worst case analysis with rapport with the model parameters of active devices is not possible. For this purpose, we construct the component model for the two transistors of which characteristic curves represent the lot dispersion. Let be BFW11_Mod_a the device for which we extracted from measured curves the following parameters: V_{t0} (V) = -1.0686, I_{DSS} (mA) = 1.976 and $\lambda(V^{-1})$ = 0.02591. The other transistor named BFW11_Mod_b is characterized by the parameter values: V_{t0} (V) = -2.3085, I_{DSS} (mA) = 5.8112 and $\lambda(V^{-1})$ = 0.02317. The user models characterizing the lot dispersion are constructed and saved with the same names as the devices. The main parameters of the two models are summarized in Table 2. As for previous case, the rest of the model parameters have the same values as they of BFW11 model in Master Database of simulator.

Table 2. Main parameters of the BFW11_Mod_a and BFW11_Mod_b models

	BFW11_Mod_a	BFW11_Mod_b
V_{T0} (V)	-1.0686	-2.3085
β (mA/V^2)	1.73071	1.09045
λ (V^{-1})	0.02591	0.02317

Now, we consider the effects of five circuit parameters on the same DC outputs as in previous case. Among these, we have two component parameters with symmetrical tolerances, i.e. R_2 and R_3, and three device parameters with asymmetrical tolerances, i.e. V_{th}, β and λ. The nominal value and tolerance of these five parameters are as follows: $p_1 = R_2$, p_{10} (Ω) = 620, ε_1 (Ω) = 31; $p_2 = R_3$, p_{20} (kΩ) = 3.9, ε_2 (Ω) = 195; $p_3 = V_{T0}$, p_{30} (V) = -2, ε_{p3} (V) = 0.9314, ε_{n3} (V) = 0.3085; $p_4 = \beta$, p_{40} (mA/V^2) = 1.24685, ε_{p4} (mA/V^2) = 0.48386, ε_{n4} (mA/V^2) = 0.1564; $p_5 = \lambda$, p_{50} (V^{-1}) = 0.0246045, ε_{p5} (V^{-1}) = 0.001311, ε_{n5} (V^{-1}) = 0.001429. The nominal values p_{30}, p_{40} and p_{50} correspond to the model parameter values of BFW11_mod device. Their asymmetrical tolerances associated to these nominal values, i.e. ε_{p3}, ε_{n3}, ε_{p4}, ε_{n4}, ε_{p5}, ε_{n5}, represent the differences between the values of the homonym parameters of BFW11_Mod model and BFW11_Mod_a model, respectively BFW11_Mod_b model.

According to the proposed procedure, the polytope with averaged nominal point has 2^5 vertices corresponding to the five considered parameters of circuit. The hypothesis of the constant temperature introduces some constraints concerning the combination of tolerances assigned to the model parameters of JFET. This means that the mean values of tolerances associated to the two model parameters will be simultaneously added or subtracted from the averaged nominal values for all three parameters. Consequently, only 2^3 vertices of polytope rest to be tested.

Next, we have to calculate the averaged nominal values and mean tolerances of the parameters according to (7) and (8). These algebraic calculations yield the following data: $p^0_{m1} = p_{10}$ (Ω) = 620, $\varepsilon_{m1} = \varepsilon_1$ (Ω) = 31; $p^0_{m2} = p_{20}$ (kΩ) = 3.9, $\varepsilon_{m2} = \varepsilon_2$ (Ω) = 195; p^0_{m3} (V) = -1.68855, ε_{m3} (V) = 0.61995; p^0_{m4} (mA/V^2) = 1.41058, ε_{m4} (mA/V^2) = 0.32013; p^0_{m5} (V^{-1}) = 0.024545, ε_{m5} (V^{-1}) = 0.00137.

Now, applying (9) we can write the vertices of the polytope with averaged nominal point as follows:

$$P^1_m = \begin{bmatrix} 589 \\ 3705 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P^2_m = \begin{bmatrix} 651 \\ 3705 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P^3_m = \begin{bmatrix} 589 \\ 4095 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}$$

$$P^4_m = \begin{bmatrix} 651 \\ 4095 \\ -1.0686 \\ 1.73071 \\ 0.02591 \end{bmatrix}; P^5_m = \begin{bmatrix} 589 \\ 3705 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}; P^6_m = \begin{bmatrix} 651 \\ 3705 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}$$

$$P_m^7 = \begin{bmatrix} 589 \\ 4095 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}; P_m^8 = \begin{bmatrix} 651 \\ 4095 \\ -2.3085 \\ 1.09045 \\ 0.02317 \end{bmatrix}.$$

To find out the DC worst case outputs of the circuit, we have to run eight times the DC Operating Point Analysis from the circuit simulator for the eight specified vertices. Each polytope vertex means a particular circuit concerning the active device, i.e. either BFW11_Mod_a or BFW11_Mod_b, and extreme values of the two resistances. The simulation results are shown in Table 3.

Table 3. The results of the DC worst case analysis based on the polytope vertex test.

Polytope vertices	DC circuit outputs		
	Y_1(V)	Y_2(V)	Y_3(mA)
P^1	9.14932	0.45318	0.76941
P^2	**9.31214**	0.47228	0.72546
P^3	8.8569	**0.45208**	0.76754
P^4	9.03572	0.47124	**0.72387**
P^5	5.36171	1.05532	**1.79171**
P^6	5.75153	**1.09791**	1.6865
P^7	**4.69983**	1.05001	1.7827
P^8	5.12496	1.09296	1.67889

The minimum and maximum values of each band (bolded in Table 3) represent the results of the worst case analysis based on the polytope vertex test. The parameter value dispersion of active device highlighted by the differences of the band bounds of each DC outputs of the circuits in Table 1 and 3 has a critical impact on meeting the design specifications.

5 Conclusion

In this paper, a procedure to perform the worst case analysis of an analog circuit with symmetrical and/or asymmetrical tolerance is presented. The proposed procedure is different to that used in circuit simulator, because it is not based on the sensitivity analysis. The worst case values of the circuit outputs or performance specifications are obtained by performing DC or AC or transient analysis for the extreme values of parameters given by the vertices of a polytope. The number of vertices increases with the number of circuit parameters taken into account. When the worst case analysis is performed in conjunction with a circuit simulator for a large number of parameters such a procedure becomes heavy. Each polytope vertex requiers the modification and resimulation of the circuit. This drawnback disappears when the procedure is applied in conjunction with a computational environment. The results obtained utilizing the proposed procedure are nearly the same as the experimental results. This means that the proposed procedure can be an alternative means to perform the worst case analysis of an analog circuit.

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