Design of Power Amplifier with On-Chip Matching Circuits using CPW Line Impedance (*K*) Inverters

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Abstract: - Recently, spiral inductors have widely been used in the design of matching circuits of a wireless transceiver. However, such elements usually have low quality factor (Q) and may encounter the self-resonance in microwave-frequency band which permits its use in higher frequencies, and on the other hand, they occupy the large on-chip space. This paper presents a new design theory for the impedance-matching circuits for a single-chip SiGe BiCMOS receiver front-end for 5 GHz-band WLAN. The presented matching circuits are composed of conductor-backed coplanar waveguide (CPW) meanderline resonators and impedance (*K*) inverter. The prototype power amplifier (PA) is fabricated and measured. A few of the measured results to verify the design theory are presented.

Key-Words: - CPW Line, Impedance (*K*) inverters, Impedance-matching circuits, Transmission-line theory.

1 Introduction

In the RF section of LSI chip, impedance and noise matching circuits are necessary for interconnecting each part such as low-noise amplifier (LNA), power amplifier (PA), duplexer, mixers, and so on, and lumped elements are usually used for the design of matching circuits. Impedance matching is usually realized by off-chip bonding wires or on-chip spiral inductors. Realization of matching circuits using the off-chip bonding wires is not an engineering art of work because it usually demands a trial and error process. On the other hand, conventional matching circuits realized by using spiral inductors occupies large on-chip space and it also encounters self-resonance in microwave frequency band which permits its use beyond that frequency. They also suffers from the low quality factor (Q). Therefore, realization of on-chip matching circuits employing on-chip transformers has drawn the attraction of many researchers in recent years [1]-[3]. However, such circuits suffers 2.5 dB transmission losses at 900MHz under best condition [3].

Distributed elements made of transmission lines to replace spiral inductors are particularly effective when their size becomes smaller, as the frequency in use increases. Among the transmission lines, coplanar waveguide (CPW) line is easy to fabricate by the LSI technology compared to its counter part such as microstrip or strip lines because the signal line and ground plane exist on the same plane [4],[5].

The applications of the distributed elements made of transmission lines were reported in the CMOS or BiCMOS RF-LSI chip [4]-[8]. The CPW lines was exploited as an inductor and used to design a conventional-type matching circuit for an LNA [6] in microwave-band frequency, and they were also used as an inductor in GaAs based monolithic microwave integrated circuit (MMIC) for millimeter-wave devices [7], [8]. However, the application of CPW lines as an inductor takes larger space than a conventional spiral inductor [6]. Some of the present authors have also implemented the CPW superconducting impedance-matching circuit for interconnecting an antenna and duplexer [9] and for a LSI chip at 2.4 GHz band [10].

In this paper, the design theory of the CPW impedance-matching circuits for single-chip SiGe BiCMOS PA for wireless LAN at 5.2 GHz band is presented using a commercial electromagnetic (EM) and SPICE co-simulator (ADS2004A; Agilent Technologies). The circuit can simultaneously possess filter characteristics for bandpass and matching characteristics for maximum power gain and optimal noise performance. The presented theory is verified by comparing the simulation with measurement.

2 Design of PA with Proposed CPW Line Matching Circuits

2.1 Design of 1-Pole Matching Circuits using *K*-Inverters

In the present work, main focus is given on the design of the on-chip impedance-matching circuit for PA and its verification. The presented matching circuit is composed of the CPW meander lines and impedance (*K*) inverters.

Fig. 1 shows the equivalent circuit diagram of the presented matching circuit. Y_L ($=G_L+jB_L$) is the input admittance of the amplifier and Δl is the line length in order to compensate the jB_L. Z_1 and $K_{0,1}$ are the characteristic impedance of the quarter wavelength line and *K* inverter, respectively. The design parameters are given by [11],

$$\left.\begin{aligned} \Delta\ell &= -\frac{B_L}{\omega_0 C}, \\ Z_1 &= \frac{\pi}{4}\frac{w}{g_1 g_2 G_L}, \\ K_{0,1} &= \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4}Z_1\right) \end{aligned}\right\} \tag{1}$$

where, *C* is the capacitance per unit length of the transmission line, and *w* and g_i are the normalized bandwidth and normalized filter element, respectively [5]. The reactance slope parameter (x_1) is for the series resonance circuit. The design parameters of the CPW matching circuit are f_0=5.2 GHz and *w*=100 MHz, which is used as an IEEE 802.11a application.

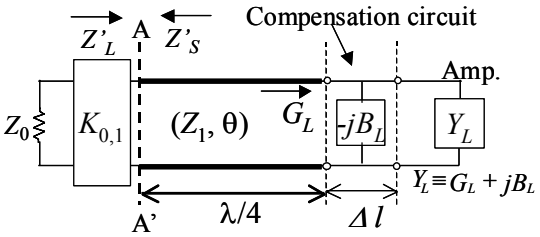


Fig. 1 Circuit model of the proposed matching circuit using λ/4 transmission lines.

The physical interpretation of the design theory in Smith chart is illustrated in Fig. 2. For example, Z^*_L is the conjugate of input impedance of the receiver front-end (Z_L=1/Y_L) (say of amplifier) and its position is shown by point x in the Smith chart. The insertion of the λ/4-transmission line converts the high impedance to very low, and its position is represented by x' in the Smith chart. By using negative capacitance (-*C*), now its position will be shifted to new position, y and again due to the *K*-inverter, the 50Ω-matching can be designed. A compensation circuit to achieve –*C* is realized by making the length of the transmission line slightly shorter than λ/4.

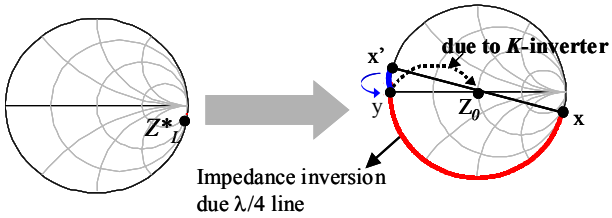


Fig. 2 Smith chart representation of the circuit model of the presented matching circuit using λ/4 line and *K*-inverter.

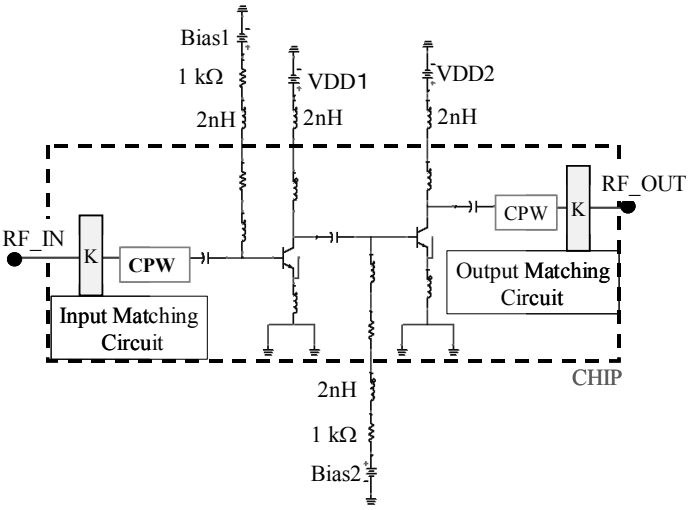


Fig.3 Block diagram of the 5GHz-band power amplifier.

2.2 Design of PA with On-Chip Matching Circuits

Fig.3 shows the schematic of the 5.2 GHz PA. In the figure, circuit model of the quarter wavelength CPW matching circuit is also presented. In order to obtain the linearity, cascade structure is chosen. To separate return paths for RF signal and bias dc current, split grounding structure is used, otherwise which causes oscillation in our previous study. Fig. 4 shows designed gain (S_{21}), input return loss (S_{11}), and output return losses (S_{22}) of the PA. Fig. 5 shows the input power dependence of the output power. The 1-dB

compression point is P_{in}=3.3 dBm. CPW on-chip input and output matching circuits are designed and simulated by the EM simulator (Momentum, Agilent technologies).

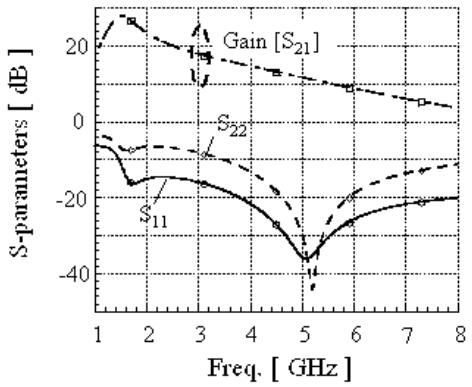


Fig. 4 Designed input return loss (S_{11}), output return loss (S_{22}) and gain (S_{21}) of the PA where the matching circuit is designed by the presented theory.

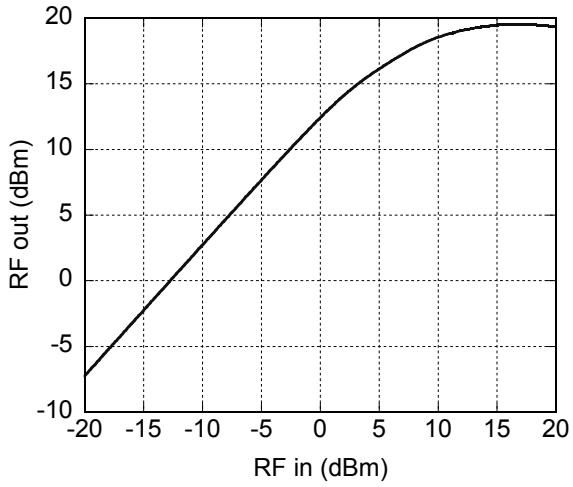


Fig. 5 Input power dependence of the output power showing linearity of PA.

3 Measured Results and Discussion

Fig. 6 shows the chip photo of PA with presented matching circuits at input and output port fabricated on TSMC 0.35μm SiGe BiCMOS technology. Spiral inductors are used to apply DC power into the transistors which was built on-chip. The input and output microwave characteristics are measured by using air coplanar probes (GSG 150; Cascade Microtech Inc.) and vector network analyzer (HP-8722; HP). Fig. 7 shows the measured S-parameters of the PA including gain (S_{21}), input and output return losses (S_{11} and S_{22}), respectively. The measured gain is obtained about 10dB at frequency of 2.2 GHz although its designed value is 11dB at 5.2 GHz. The discrepancy in the measured and designed frequency is caused by the inductance of the bonding wires that connects the grounding pad which was not considered during the design process. Taking account of this inductance in simulation, Fig. 8 shows the comparison of simulated results of S-parameters.

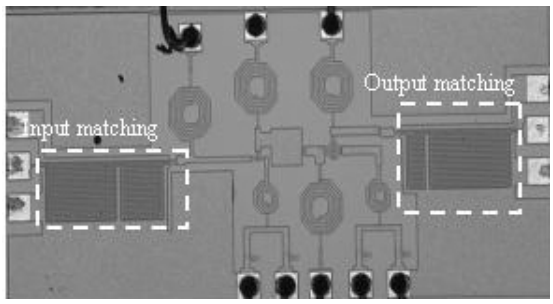


Fig. 6 Microphotograph of PA with the proposed impedance-matching circuits fabricated in TSMC 0.35 um SiGe BiCMOS one poly three metal process. (Chip size: 2.38 mm x 1.05 mm).

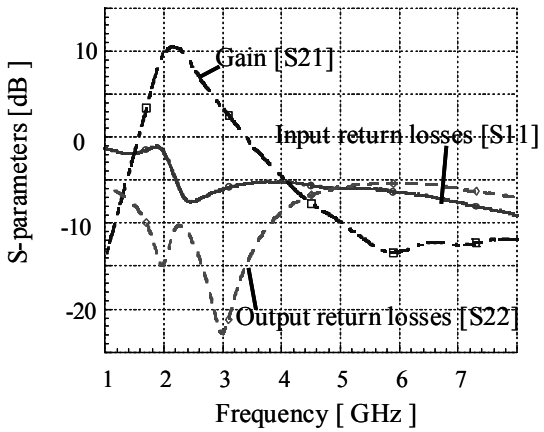


Fig. 7 Measured S-parameters of fabricated PA.

In Fig. 8(a), comparison of input return loss and output return loss are shown and comparison of gain is shown in Fig. 8(b), where the simulated results including gain are very close to the measured results.

K-inverters are fabricated using shunt meander structure [5]. Fig. 9 shows microphotograph of *K*-inverter circuits which is designed using equation (1) and simulated by the EM simulator (Momentum, Agilent technologies). The conductance of the metal is 4.1×10^7 S/m. The signal width and the interval between the slots of the CPW transmission line are 5 μm and 15 μm, respectively. For size reduction, the λ/4 line was bended into meander structure and Co-simulation technique which characterize passive elements together with active elements have been used. Fig. 10 shows the comparison of the frequency responses of the *K*-inverter. Insertion loss (S_{21}) of the EM-simulated result is almost in agreement with that of the experimental result.

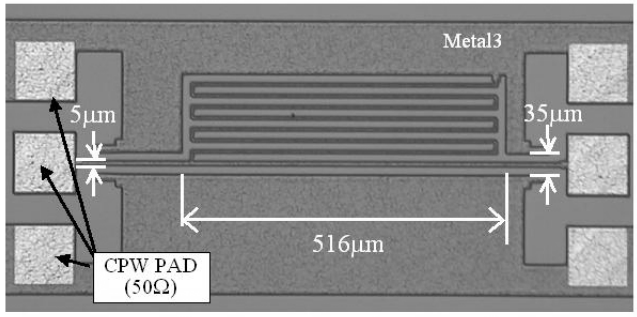
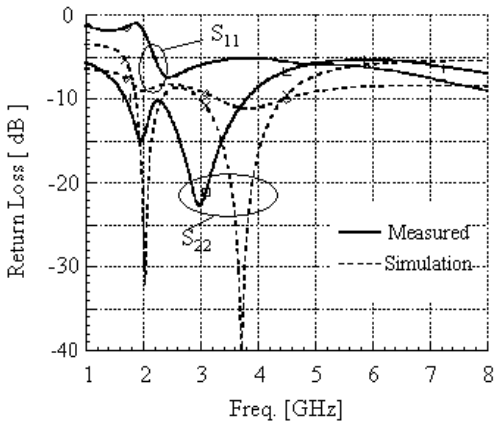
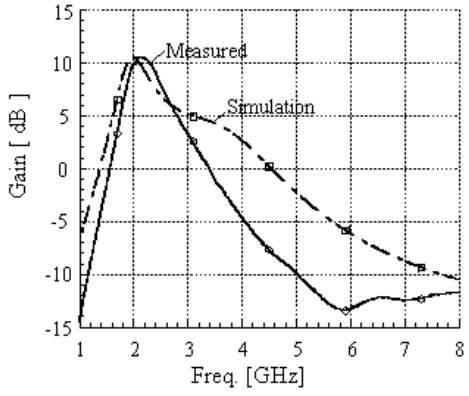


Fig. 9 Microphotograph of the *K*-inverter.(Taken out from another fabricated chip which is not shown in Fig. 4.).



(a) Comparison of input return loss and output return loss.



(b) Comparison of gain

Fig. 8 Comparison of S-parameters taking account of inductance of bonding wires from the ground pads.

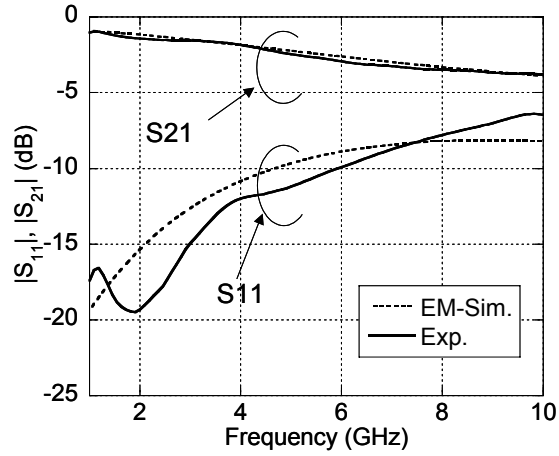


Fig. 10 Frequency responses of the CPW meanderline resontor.

4 Conclusion

Design methodology of matching circuits for a single chip SiGe BiCMOS receiver front-end (PA) which is composed of λ/4 CPW meander resonators and *K*-inverter is presented and verified by comparing the simulation results with measured results on a designed chip fabricated in TSMC0.35 μm SiGe BiCMOS technology. The CPW lines are realized by meander structures so that they can be fabricated inside a chip and their shape can be adjusted in order to exploit the vacant space on the substrate effectively unlikely in the case of spiral inductors. It takes less space than that of the spiral inductors. A rough comparison shows that the matching circuit designed by the proposed method

takes 30% less space than that of the on-chip spiral inductors.

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