Predicate Gates for Spatial Logic

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Abstract: - The predicate logic gates are proposed for spatially modulated signals. Two voltage impulses are transmitted along the coupled wires, and they are considered as a predicate expression. The developed gates perform the logical operations AND, NOT and OR with these expressions. They are used for a predicate logic microprocessor.

Key-Words: - Artificial spatial intelligence, predicate logic, topological computing, spatial predicate gates

1 Introduction

Artificial intelligence modeling attracts increased attention of the computer scientists and engineers. One of the brain activities is with calculations, and it has been modeled successfully by digital computers based on the Boolean logic. Some developments were performed for predicate logic hardware for modeling natural languages [1,2].

Unfortunately, another of the unique brain activities – the logical handling of images or spatial intelligence is still rather far from successful hardware modeling according to the best authors' knowledge. Mostly, the software and corresponding equipment operate with the pixels, and this process is a very time consuming. Meanwhile, the fast and human-like handling of the spatial information is in a high demand for many applications including robot vision, real-time radar-image processing and automatic target recognition.

According to common opinion, the human-brain unique ability on the image processing and cognition is with qualitative processing and reasoning of the images in the space-time. The images have certain geometry, brightness and color. At the difference to the most software tools, the spatial shapes are associated in the brain with the "soft", topologically defined forms. Each topologically different form corresponds to a logical unit. Other characteristics of the shapes like brightness and color can be described by fuzzy or discretely defined information. Suppose that the topological form is the predicate then other characteristics are the predicate variables, and all the parameters can compose a predicate expression. Finally, the spatial logic is the first- or the second-order predicate one, and it can be modeled by predicate logic electronic circuitry. Taking into account that the hardware for spatial (qualitative) logic has been rather far from any practical realization, our paper is dedicated on this topic.

The results are based on the research started in 1988 when the qualitative theory of boundary problem of electromagnetism was developed [3]. These techniques allow calculating the topology of the electromagnetic field according to the given boundary conditions without time-consuming pre-computations. Then, the qualitative results can be used for physical analyses of the problems or for initial approximations for more advanced computations. Later, new signals carrying information by their magnitudes and field topological charts were invented and associated with the predicates [4-7]. A set of electronic circuits was developed for the Boolean, predicate, pseudo-quantum and mixed discrete-analogue signal processing. A conception of a reconfigurable processor (1992) was also proposed. Today, the predicate hardware is used in the Itanium family of processors (1999) and graphical NVIDIA's cards distinguished by their increased computational power [8].

The presented here results are on a certain type of predicate gates built on the spatio-temporal ideology. They can be used in predicate logic microprocessors for linguistic "computations," database machines and SQL servers.

[2] This work was carried out during the tenure of an ERCIM – Alain Bensoussan Fellowship Programme

2 Predicate Logic and the Gate Truth–Tables

The earlier considered topologically modulated signals are the differential and common modes impulses (Fig. 1) of coupled strip lines [5]. They carry digital information by the field topological charts $T_{0,1}$ and the impulse magnitudes $a_{1,0}$. Thus, each mode has two logical magnitude levels associated with the predicate and predicate variable.

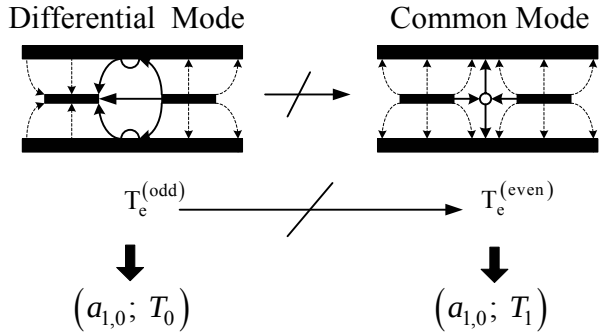

Fig. 1. 2D-maps of topologically modulated signals. The electric field.

The truth–tables for NOT, OR and AND operations with the predicate expressions are shown in Tables 1-3.

Table 1. Truth-table for the predicate logical operation NOT

Input	Output
(T_0, a_0)	(T_1, a_1)
(T_0, a_0)	(T_0, a_1)
(T_0, a_0)	(T_1, a_0)
(T_1, a_1)	(T_0, a_0)
(T_1, a_1)	(T_0, a_1)
(T_1, a_1)	(T_1, a_0)
(T_0, a_1)	(T_1, a_1)
(T_0, a_1)	(T_0, a_0)
(T_0, a_1)	(T_1, a_0)
(T_1, a_0)	(T_1, a_1)
(T_1, a_0)	(T_0, a_0)
(T_1, a_0)	(T_0, a_1)

They are derived based on the fact that the operations of prepositional logic transform the predicates into predicates. Another important issue is that all operations of prepositional logic are applicable to the predicates as well as their properties are maintained [9].

Table 2. Truth-table for the predicate logical operation OR

Input 1	Input 2	Output
(T_0, a_0)	(T_0, a_0)	(T_0, a_0)
(T_0, a_1)	(T_0, a_0)	(T_0, a_1)
(T_1, a_0)	(T_0, a_0)	(T_1, a_0)
(T_1, a_1)	(T_0, a_0)	(T_1, a_1)
(T_0, a_0)	(T_1, a_0)	(T_1, a_0)
(T_0, a_1)	(T_1, a_0)	(T_1, a_1)
(T_1, a_0)	(T_1, a_0)	(T_1, a_0)
(T_1, a_1)	(T_1, a_0)	(T_1, a_1)
(T_0, a_0)	(T_0, a_1)	(T_0, a_1)
(T_0, a_1)	(T_0, a_1)	(T_0, a_1)
(T_1, a_0)	(T_0, a_1)	(T_1, a_1)
(T_1, a_1)	(T_0, a_1)	(T_1, a_1)
(T_0, a_0)	(T_1, a_1)	(T_1, a_1)
(T_0, a_1)	(T_1, a_1)	(T_1, a_1)
(T_1, a_0)	(T_1, a_1)	(T_1, a_1)
(T_1, a_1)	(T_1, a_1)	(T_1, a_1)

Table 3. Truth-table for the predicate logical operation AND

Input 1	Input 2	Output
(T_0, a_0)	(T_0, a_0)	(T_0, a_0)
(T_0, a_1)	(T_0, a_0)	(T_0, a_0)
(T_1, a_0)	(T_0, a_0)	(T_0, a_0)
(T_1, a_1)	(T_0, a_0)	(T_0, a_0)
(T_0, a_0)	(T_1, a_0)	(T_0, a_0)
(T_0, a_1)	(T_1, a_0)	(T_0, a_0)
(T_1, a_0)	(T_1, a_0)	(T_1, a_0)
(T_1, a_1)	(T_1, a_0)	(T_1, a_0)
(T_0, a_0)	(T_0, a_1)	(T_0, a_0)
(T_0, a_1)	(T_0, a_1)	(T_0, a_1)
(T_1, a_0)	(T_0, a_1)	(T_0, a_0)
(T_1, a_1)	(T_0, a_1)	(T_0, a_1)
(T_0, a_0)	(T_1, a_1)	(T_0, a_0)
(T_0, a_1)	(T_1, a_1)	(T_0, a_1)
(T_1, a_0)	(T_1, a_1)	(T_1, a_0)
(T_1, a_1)	(T_1, a_1)	(T_1, a_1)

3 Logical Design of Predicate Gates

The above-proposed signals and the assigned to them predicate expressions are for high-speed signaling and operations. Unfortunately, in spite of the visible and well-studied advantages of the couple-pair signaling in high-speed electronics, the industry available digital design software is oriented mostly to the unipolar (single-ended) signals. To adopt our developments for the existing commercially available software, the predicate expressions are mapped into the predicate ones for the unipolar signals on a pair of wires:

$$(T,a)\Rightarrow(b,c) \qquad (1)$$

where the variables $b,c\in\{0,1\}$. In this way, the proposed truth-tables (Tables 1-3) are modified to the Tables 4-6. The symbols T_0 and a_0 in the tables are substituted with the logic level "0", and the symbols T_1 and a_1 with the logic level "1".

Table 4. Modified truth-table for the predicate logical operation NOT

№	Input		Output	
	Ti	*ai*	*Tj*	*aj*
1	0	0	1	1
2	0	0	0	1
3	0	0	1	0
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	0	1	1	1
8	0	1	0	0
9	0	1	1	0
10	1	0	1	1
11	1	0	0	0
12	1	0	0	1

Table 5. Modified truth-table for the predicate logical operation OR

№	Input 1		Input 2		Output	
	Ti_1	ai_1	Ti_2	ai_2	*Tj*	*aj*
1	0	0	0	0	0	0
2	0	1	0	0	0	1
3	1	0	0	0	1	0
4	1	1	0	0	1	1
5	0	0	1	0	1	0
6	0	1	1	0	1	1
7	1	0	1	0	1	0
8	1	1	1	0	1	1
9	0	0	0	1	0	1
10	0	1	0	1	0	1
11	1	0	0	1	1	1
12	1	1	0	1	1	1
13	0	0	1	1	1	1
14	0	1	1	1	1	1
15	1	0	1	1	1	1
16	1	1	1	1	1	1

Table 6. Modified truth-table for the predicate logical operation AND

№	Input 1		Input 2		Output	
	Ti_1	ai_1	Ti_2	ai_2	*Tj*	*aj*
1	0	0	0	0	0	0
2	0	1	0	0	0	0
3	1	0	0	0	0	0
4	1	1	0	0	0	0
5	0	0	1	0	0	0
6	0	1	1	0	0	0
7	1	0	1	0	1	0
8	1	1	1	0	1	0
9	0	0	0	1	0	0
10	0	1	0	1	0	1
11	1	0	0	1	0	0
12	1	1	0	1	0	1
13	0	0	1	1	0	0
14	0	1	1	1	0	1
15	1	0	1	1	1	0
16	1	1	1	1	1	1

Below, the designs of the mapped gates are considered according to Tables 4-6.

3.1 Predicate NOT gate

Here, the simplest designs of the predicate NOT gates are proposed. For this reason, three different types of predicate logic gates called ANOT (Amplitude NOT), TNOT (Topologically Chart NOT) and BNOT (Boolean NOT) are used. They cover all possible binary combinations in the above-mentioned truth-tables.

3.1.1 ANOT predicate gate

The proposed ANOT predicate gate (Fig. 2) has the truth-table shown in Table 7.

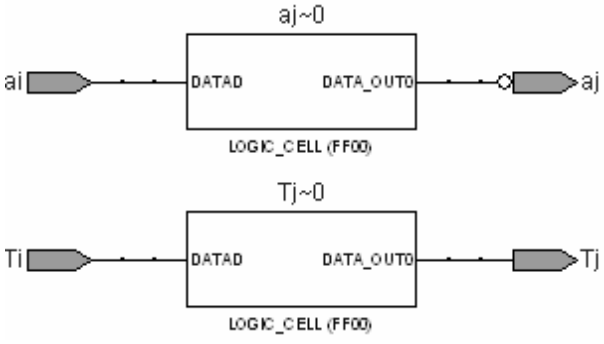

Fig. 2. Synthesized ANOT gate

Table 7. Truth-table for the predicate ANOT gate

Input		Output	
Ti	*ai*	*Tj*	*aj*
0	0	0	1
0	1	0	0
1	0	1	1
1	1	1	0

This gate inverts only the logical levels corresponding to the mapped amplitudes of the signals.

3.1.2 TNOT predicate gate

The TNOT gate inverting the logical levels associated with the topological charts is shown in Fig. 3. It consists of a follower and a NOT gate, and its logic is shown in Table 8.

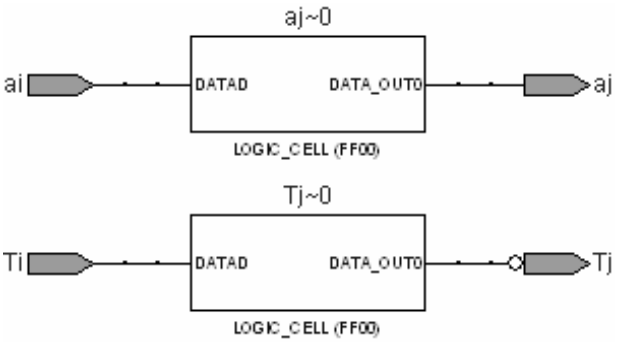

Fig.3. Synthesized TNOT gate

Table 8. Truth-table for the predicate TNOT gate

Input		Output	
Ti	*ai*	*Tj*	*aj*
0	0	1	0
0	1	1	1
1	0	0	0
1	1	0	1

3.1.3 BNOT gate

The BNOT gate (Fig. 4) inverts all logical input levels according to Table 9.

Table 9. Truth-table for the predicate BNOT gate

Input		Output	
Ti	*ai*	*Tj*	*aj*
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

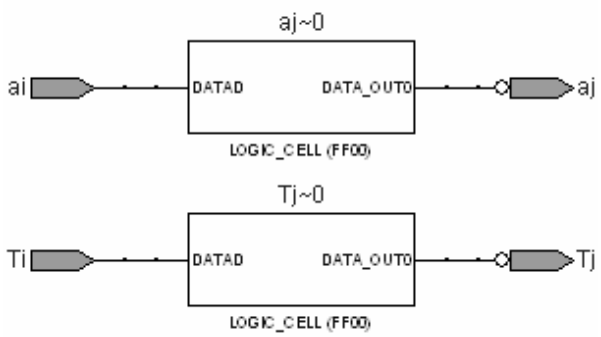

Fig. 4. Synthesized BNOT gate

3.1.4 UNOT predicate gate

Additionally to the above-considered gates performing selected logical operations, a universal NOT (UNOT) gate has been designed (Fig. 5). It consists of the ANOT, TNOT and BNOT gates connected to the common output through a multiplexer (Mux: D). The two-bit control signal *S* defines a certain type of the previously defined logical operations – ANOT, TNOT or BNOT.

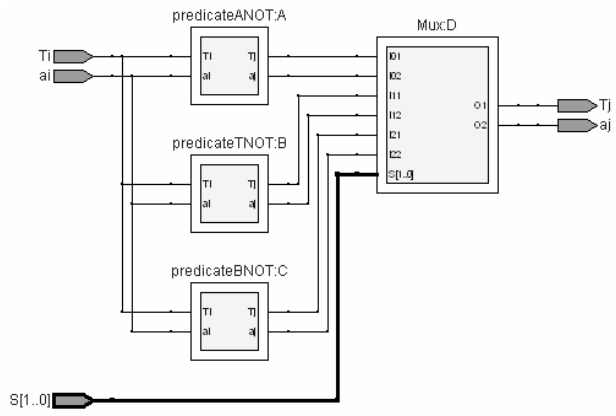

Fig. 5. Synthesized UNOT gate

3.2 Predicate OR gate

An OR gate handling with the predicate expressions (Table 5) is shown in Fig. 6.

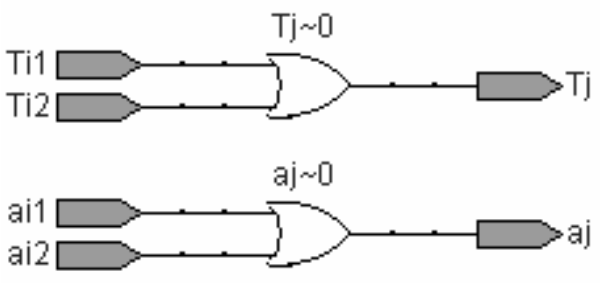

Fig. 6. Synthesized predicate OR gate

For this purpose, a couple of two-input standard OR gates is used. This gate transforms the logical levels associated with the predicate *a* and the predicate variable *T* according to Table 5.

3.3 Predicate AND gate

Similarly, a predicate gate AND is introduced (Fig. 7). It consists of two-inputs Boolean AND gates, and its logic is described with Table 6.

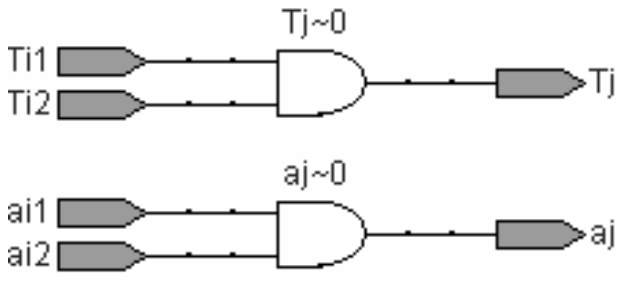

Fig. 7. Synthesized predicate AND gate

All gates are designed using the VHDL (Very High Speed Integrated Circuit Description Language) [14, 15].

4 Simulation of the Proposed Gates

The predicate logic gates designs are simulated and tested by ModelSim Xilinx edition III/Starter version 6.01e [12].

These simulation results are shown in Figs 8 – 10. The test methodology of the predicate logic gates is the next. All possible input combinations are introduced. The output logical levels are registered and compared according to the gates' truth-tables.

The testing results of the UNOT gate are shown in Fig. 8. The input signals are labeled by (Ti, ai), the control signal by *S* and the output signals by (Tj, aj). The control signal value *S* is changed starting from "00" to "11". The inputs (Ti, ai) obtain the next four possible binary combinations – "00", "01", "10" and "11" for a certain *S* value. The wave diagrams in Fig. 8 show the logic values on the inputs and outputs of the UNOT gate for the control signal that correspond to the logical combination "10". In this case, it has been selected BNOT operation (BNOT predicate gate).

In Fig. 9, a part of the test results of the predicate gate AND is shown. Here, the input signals are the first four wave diagrams, and the output signals are assigned to (*tj)* and (*aj)* symbols. The results of logical simulations are according to the Table 6.

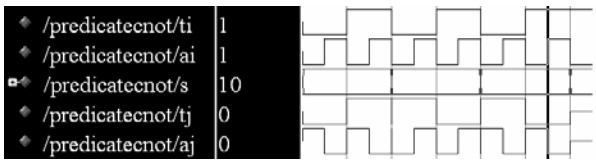

Fig. 8. Simulated wave diagrams of the UNOT gate

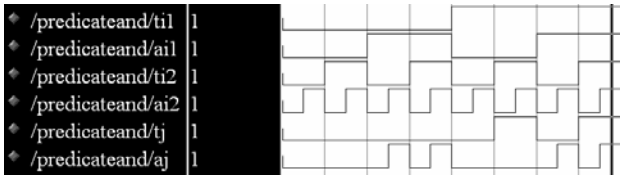

Fig. 9. Simulated wave diagrams of the predicate AND gate

Fig. 10 shows the input (Ti_1, ai_1, Ti_2, ai_2) and the output $(Tj\ , aj)$ signals of the predicate OR gate.

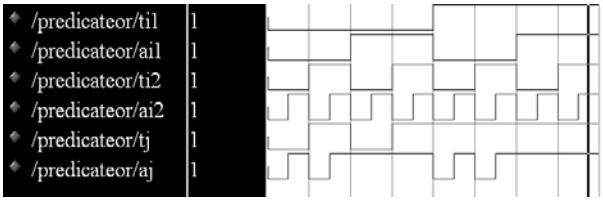

Fig. 10. Simulated wave diagrams of the predicate OR gate

5 Experimental Verification of Gates

All proposed gates are synthesized and verified using the UP2 board manufactured by Altera Corp. [11]. It is a stand-alone experimental board based on the FLEX®10K, and it includes a MAX®7000 device [10]. The sources of the input signals are the 8 FLEX_SW1 switches located on the board providing the logic signals to the eight general-purpose I/O pins. An input pin is set to the logic level "1" when the switch is open. The closed switch provides the signal with the logic level "0" [10]. The two-channel digital storage oscilloscope DSO3152A [13] displays the voltage levels on the gates outputs.

An example of the derived results is shown in Fig. 11. This is a part of the predicate OR gate test when the values $ai_1 = 0, ai_2 = 0, Ti_1 = 0, Ti_2 = 1$ are applied. The measured voltage on the output aj is the logic "0"

(200 mV) and on Tj is the logic "1" (3.60 V) (see Table 5).

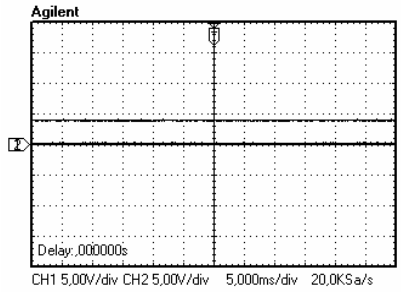

Fig. 11. A part of the predicate OR gate verification process

Other derived results are shown in Fig. 12. This is a part of the predicate AND gate test when the input signal levels are $ai_1 = 1, ai_2 = 1, Ti_1 = 1, Ti_2 = 1$. The measured voltages on the outputs aj and Tj are 4.20 V that correspond to the logic level "1" and the truth-table of the predicate AND gate (see Table 6).

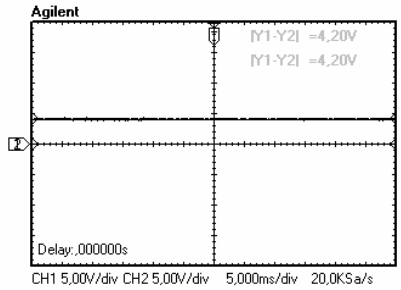

Fig. 12. A part of the predicate AND gate verification process

The last one of the derived results is shown in Fig. 13. This is a part of the predicate UNOT gate testing when the logical values $ai = 1, Ti = 1, S = 10$ are applied (BNOT operation is selected). The measured voltages on the outputs aj and Tj are the same and equal to 200 mV that corresponds to the logic level "0".

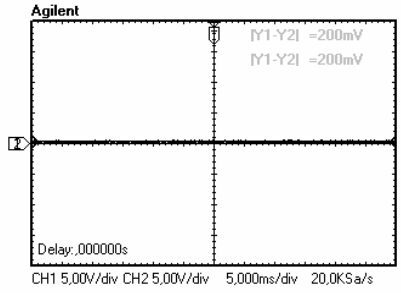

Fig. 13. A part of the predicate UNOT gate verification process

6 Conclusions

The spatial intelligence is one of the most important brain activities. It has not been paid essential attention on that for many years. Some research activities show that the spatial information is processed by the way reminding the qualitative calculations. It has been introduced that spatial computing and predicate logic can model some aspects of such processes. A minimal set of predicate gates has been designed, modeled and verified. They perform the basic logical operations with the predicate expressions. The design flow and proposed electronic circuitry are based on the contemporary software tools and technology used for rapid digital design prototyping. The performed research is a step towards to the development of predicate logic microprocessors applicable for linguistic calculations, database machines and SQL servers.

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