Determining the Basic JFET Parameters from Static Characteristics

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Abstract: - A general-purpose circuit simulator is an appropriate tool that can be used very effectively to promote student understanding of the link between theory and application. It can be employed to compare device theory with the actual operation of an electronic device, using an effective visual format. It can also facilitate the implementation of computer-aided circuit design and verification. This paper presents an example of utilizing such a circuit simulator to JFET parameter estimation from its characteristic curves in an introductory electronics course. This example is only first part of a project concerning the JFET operation and its fundamental applications. As part of the same project, it follows the small-signal audio amplifier design that is verified firstly by simulation and then by measurement on the actual prototype JFET amplifier that the student has constructed in the laboratory. The first part of the project conceived as laboratory exercise allows the student to perform an estimation of the transconductance, threshold gate voltage and length-channel modulation parameter of a NJFET transistor.

Key-Words: - JFET, Static characteristics, Basic JFET parameter estimation, Simulation

1 Introduction

The operating characteristics of JFETs are often unpredictable because of their internal geometric dependence. Understanding even minute differences in individual JFET operating characteristics is an important aspect in the design of many electronic systems. When designing audio amplifiers, for example, it is important to determine exactly what levels of performance will be available for various inputs. Consequently, tests can be done to more accurately determine the operating characteristics of JFET devices [1]-[5]. Such tests require the measurement of the drain current over a range of drainto-source and gate-to-source voltages. The overall electronic system design can be optimized once these values are known. Semiconductor parameter analyzers or more sophisticated platforms that integrated specific hardware and software make possible extracting the parameters of a device.

Using standard test equipment, MATLAB, and the Data Acquisition Toolbox, a system to test individual JFET characteristics can be designed. Such a system for determining the characteristic curves for a JFET is minutely described in [6]. First, the hardware is set up and then the MATLAB code for acquiring data and analyzing the results is written. The drain current versus the drain-to-source voltage characteristic curve are plotted for two JFETs that are part of the same production lot. These plots shown that, though the JFET devices were produced at the same time, they are electrically very different because of the differences in

each JFET's internal geometry [1] - [13]. A simple test lab setup can plot the characteristic curves for a complete operating characterizing of JFET devices too.

Almost all the engineering programs in technical universities require an introductory electronics course. This introduction to electronics "service" course endeavors to provide the junior-level student with a sound understanding of the electrical characteristics of semiconductor devices as well as their use in basic electronic circuits such as logic gates, power supplies, wave generators, and amplifiers. Its associated laboratory is designed to be taken concurrently with the lecture course and to reinforce lecture concepts with practical application. It is well known that link between theory and application has always been a critical objective in electronics education. For the past three years, a general-purpose circuit simulator has been used as a principal tool in laboratory exercises for electronic device testing, circuit simulation and circuit testing [14].

This paper presents one example laboratory exercise from the course that will illustrate the use of a circuit simulator for comprehensive device operation analysis. It should be noted that students in the course have previously completed two laboratory sessions concerned with learning the fundamentals of the circuit simulator and virtual instrument operation. Also, at this moment, the students have working experience in Excel.

2 NJFET Static Characteristic Simulation

The first part of the laboratory exercise concerns the measurement of the characteristic curves for an NJFET transistor. In the lecture portion of the course, the students have studied the theory of operation of the JFET and are now familiar with the characteristic equations that govern its current-voltage relationship. They are also familiar with the data sheet for the transistor that is specified in the laboratory, and will be able to compare their subsequent measurement of its characteristic parameters with values they have obtained from that data sheet.

The students are first instructed to build the circuit diagram in Fig. 1 for the NJFET analysis that they will use in this part of the exercise. The objective here is to have them become familiar with how the basic characteristic parameters of the transistor can be readout from the characteristic curves of the device. Next, they are instructed to run the DC Sweep Analysis menu to obtain the transfer and output characteristic curves of NJFET, following directions in the exercise description. They are then instructed to transfer the graphic data in Excel or Mathcad files and how these data can be processed to estimate the basic parameters of a NJFET. output static characteristics of the transistor, i.e., drain current versus drain-source voltage for particular gatesource voltages (V_{GS} =-2 V, V_{GS} =-1.5 V, V_{GS} =-1 V, V_{GS} =-0.5 V, V_{GS} =0 V,) are shown in Fig. 2b.



Fig. 1. Circuit diagram for the NJFET static characteristic simulation



a.

b.

Fig. 2. Static characteristics of a common-source NJFET: **a.** Drain current versus gate-source voltage; **b.** Drain current versus drain-source voltage

Fig. 2a displays the I-V transfer static characteristics of the transistor, i.e., drain current versus gate-source voltage for particular drain-source voltages (V_{DS} =5 V and V_{DS} =10 V, in this example) obtained by running Multisim program [15]. The I-V

At this moment, the students are required to use graphical cursors to identify the "gate threshold voltage" (V_{th}), "pinchoff voltage" (V_{DSP}) and "nominal saturation current" (I_{DSS}) from the I-V static characteristic as it is shown in Fig. 2.

3 Relationships between Basic Parameters and Static Characteristics Before continuing, it might be useful to look at the typical operating characteristics of JFET devices and their large-signal models as they are used in circuit simulators and hand analysis [7], [16], [17].



Fig. 3. Equivalent circuit of Shichman-Hodges model

The JFET models derived from the FET model of Shichman and Hodges are implemented into many circuit simulators as SPICE, Multisim, etc. According to this model with its equivalent circuit shown in Fig. 3, the dc characteristics are defined by the parameters V_{TO} (VTO) and β (BETA), which determine the variation of drain current with gate voltage, and λ (LAMBDA) that determines the output conductance. The parameter I_S is the saturation current of the two gate junctions. Two ohmic resistances, R_D and R_S , are included too.

The following expressions as they are given in the simulator help describe the large-signal JFET operating into forward region (V_{DS} >0):

$$I_D = 0 \text{ for } V_{GS} - V_{TO} < 0;$$
 (1)

$$I_{D} = \beta \cdot (V_{GS} - V_{TO})^{2} \cdot (1 + \lambda \cdot V_{DS}) \text{ for } 0 < V_{GS} - V_{TO} < V_{DS}; \qquad (2)$$

$$I_D = \beta \cdot V_{DS} \cdot [2 \cdot (V_{GS} - V_{TO}) \cdot V_{DS}] \cdot (1 + \lambda \cdot V_{DS})$$
(3)
for $0 < V_{DS} < V_{GS} - V_{TO}$.

In the above equations, the threshold gate voltage $V_{TO}=V_{th}$ and the transconductance parameter β can be calculated as

$$\beta = I_{DSS} / V_{T0}^2 . \tag{4}$$

Using the graphical cursors on the transfer characteristics for the given NJFET type BFW11, they find out $V_{th} = -2$ V and $I_D = 5.313$ mA at $V_{DS} = 5$ V, and $V_{GS} = 0$ V, and $I_D = 6.0807$ mA at $V_{DS} = 10$ V, and $V_{GS} = 0$ V. The different values of the drain current at specified values of the drain-source voltages put in evidence the non—null value of the lengh-channel modulation parameter. Proceeding in the same way with the output characteristics, the students can determine the nominal saturation current or zero-gate-voltage drain current,

the pinchoff voltage for each gate voltage value, the slopes of the two plot regions. In this example, using the drain plot corresponding to $V_{GS}=0$ V, one determines $I_{DSS}=5,1616$ mA for $V_{DS}=V_{DSP}=V_{GS}-V_{th}=2$ V. Also, one recovers $I_D=5.313$ mA at $V_{DS}=5$ V and $I_D=6.0807$ mA at $V_{DS}=10$ V, from the output characteristic plotted for $V_{GS}=0$ V. The parameter λ can be estimateed from the plot portion belonging to the active region and using the relation

$$\frac{\partial I_D}{\partial V_{DS}} = \beta \cdot (V_{GS} - V_{th})^2 \cdot \lambda = \lambda \cdot I_{DSS}.$$
(5)

For $V_{GS}=0$ V, the above equation becomes

$$\frac{\partial I_D}{\partial V_{DS}} = \lambda \cdot I_{DSS} \,. \tag{6}$$

Applying the equations (4) and (6), one obtains the following results: β =1.32 mA/V² and λ =0.03593V⁻¹. The basic parameter values of the NJFET type BFW11 model from Master data base are: V_{TO} = -2.085 V, β =1.24635 mA/V² and λ =0.0246045 V⁻¹.

After reading out the basic parameters and verifying the static relationships that characterize the JFET operation in ohmic region and active region, the graphic data must be exported in Excel. Then, they process the data files in Excel to precisely determine the characteristic parameters of the transistor.

4 Data Processing in Excel Files

Processing the information contained by the static transfer characteristics of device, the basic parameters of a JFET sample namely V_{TO} , β and λ can be determined with a better accuracy. These curves characterize the JFET operation in active region. For this purpose, in equation (2), we introduce the effective transconductance parameter β ' defined as follows:

$$\beta' = \beta \cdot (1 + \lambda \cdot V_{DS}). \tag{7}$$

Now, the equation (2) becomes

$$I_D = \beta' (V_{GS} - V_{TO})^2. \tag{8}$$

The above equation can be put in the form

$$V_{GS} = \frac{\sqrt{I_D}}{\sqrt{\beta'}} + V_{TO} \,. \tag{9}$$

The equation (9) describes a straight-line of which slope is $1/\sqrt{\beta'}$ and the zero $\sqrt{I_D}$ intercept is expected to be V_{th} . Excel obtains the slope and intercept from a straight-line fit to the data. The simulated transfer characteristic thus yields the two parameters β' and V_{th} . Now, it is clear that plotting two straight-lines described by equation (9) for two different drainsource voltage values, one can determine the three basic JFET parameters. Indeed, the parameter λ is obtained from finding β' at two different V_{DS} values. This is based on the equation

$$\frac{\beta_1'}{\beta_2'} = \frac{1 + \lambda \cdot V_{DS1}}{1 + \lambda \cdot V_{DS2}},\tag{10}$$

where the β ' values are measured and λ is the only unknown.

In the following, we refer to the two transfer characteristics, briefly, as $I_{D1}=f(V_{GS}, V_{DS1})$ for $V_{DS1}=5$ V and β'_1 , and $I_{D2}=f(V_{DS}, V_{DS2})$ for $V_{DS1}=10$ V and β'_2 . These characteristics plotted from the simulation data exported in Excel are shown in Fig. 4. The two straightlines plotted accordingly to equation (9) for $V_{DS1}=5$ V and β'_1 , and $V_{DS1}=10$ V and β'_2 respectively, are shown in fig. 5. The zero $\sqrt{I_D}$ intercept is $V_{th}=-2.05$ V, for both plots.



Fig. 4. Transfer characteristics $I_{D1}=f(V_{GS}, V_{DS1})$ and $I_{D2}=f(V_{DS}, V_{DS2})$

After the slopes of the plots $V_{GS}=f(\sqrt{I_D})$ are measured, they are utilized in equation (10) to find out the parameter λ . Then, substituting the λ value in (7) yields the β and I_{DSS} values. With $\beta'_1=1.267870213$ mA/V² and $\beta'_2=1.396229525$ mA/V², the data processing has as final results $\lambda=0.0225288$ V⁻¹, $\beta=$ 1.13951 mA/V² and $I_{DSS}=4.78$ mA. In order to compare the previously results, the Table 1 resumes the approximate values, more precise values of the basic parameters of NJFET and model parameter values in circuit simulator. The students can then compare their measurements with the specifications they have previously determined from the transistor data sheet.

Table 1. The basic parameter values of the NJFET type BFW11

| | V_{th} [V] | $\beta [mA/V^2]$ | $\lambda [V^{-1}]$ |
|-------------|--------------|------------------|--------------------|
| Approximate | -2. | 1.32 | 0.03593 |
| Precise | -2.05 | 1.13951 | 0.0225288 |
| Model | -2.085 | 1.24635 | 0.0246045 |



Fig. 5. Gate-source voltage plot versus $\sqrt{I_D}$ for $V_{DS1}=5$ V and $V_{DS1}=10$ V

5 Conclusion

This paper has presented a laboratory exercise on JFET transistor parameter analysis in an introductory electronics course. A general-purpose circuit simulator in conjunction with Excel has been employed, which aids the students in analyzing transistor static characteristics and utilizing them to estimate the basic transistor parameters. These parameters will be then used to design and verify an audio-frequency range small-signal amplifier based on a four-resistor dc bias circuit and confirm the Q-point and amplifier performance of the design by direct measurements using a board circuit. This approach helps the

beginning student to understand the link between device theory and its applications and to familiarize them with electronic instruments without having previous experience with laboratory instrumentation. Student evaluation of these projects has been very positive with respect to their effectiveness in helping them to understand the link between device theory and application.

References:

- [1] K. L. Ashley, *Analog Electronics with LabView*, Pearson Education, Inc., Prentice Hall PTR, 2003.
- [2] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th edition, Wiley, 2001.
- [3] S. M. Sze, Semiconductor Devices, Physics and Technology, 2nd edition, John Wiley and Sons, New York, 2002.
- [4] R. R. Boyd, *Tolerance Analysis of Electronic Circuit Using Mathcad*, CRC Press LLC, 2000.
- [5] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.
- [6] Determining the characteristic curve for a Junction Field-Effect Transistor (JFET) using MATLAB and the Data acquisition toolbox. *Mathworks Inc.*,

http://www.mathworks.com/technicalsupport.html

- [7] IC-CAP device modeling software, http://www.agilent.com/ Product specifications and descriptions.html.
- [8] C. Dwyer, M. Cheung and D. J. Sorin, Semiempirical SPICE models for carbon nanotube FET logic, *Proc. of the Conf. Nanotechnology*, 2004, pp. 386–388.

- [9] A. Raychowdhury, S.Mukhopadhyay and K. Roy, A circuit compatible model of ballistic carbon nanotube field-effect transistors, *IEEE Trans. Computer-Aided Design*, vol. 23, 2003, pp. 1411– 1417.
- [10] C. Reese and Z. Bao, Organic single-crystal transistors, *Materials-today*, vol. 10, No. 3, 2007, pp. 20-28.
- [11] Y. Chernukhin et al., Deploying Modelica Models into Multiple Simulation Environments, *Proc. of BMAS 2005*, 2005, pp. 1-27.
- [12] D. M. Schreurs, J. Verspecht, S. Vandenberghe and E. Vandamme, Straightforward and Accurate Nonlinear Device Model Parameter-Estimation Method Based on Vectorial Large-Signal Mesurements, *IEEE Trans. on Microwave Theory* and Tech., vol. 50, no. 10, 2002, pp. 2315-2319.
- [13] A. B. Mallik et al., Organic Field-Effect Transistors in design, synthesis, and transistor performance of organic semiconductors in organic Field-Effect Transistors. *Taylor and Francis*, 2007 [online].
- [14] E. Niculescu, D.M. Purcaru and M. Maria, *Electronics. Simulations, Analyses and Experiments,* (In Romanian), Reprograph Publishing House, 2006, Romania
- [15] *Multisim 2001. Getting Started and Tutorial*, Interactive Image Technologies Ltd., 2000
- [16] *IsSPICE* 5. *User's guide*. http://www.intusoft.com/technical support.html
- [17] T. A. Fjeldly, T. Y. Herdal and M. Shur, Introduction to Device Modelling and Circuit Simulation, John Wiley and Sons, New York, 1998