Sensitivity Factor Analysis in the Bias Circuits with FET

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Abstract: - The paper proposes a procedure to calculate the sensitivity factors of the quiescent drain current of a FET operating in the active region in conjunction with a general-purpose circuit simulator. Unlike the procedure developed for the sensitivity factors of the quiescent collector current in BJT, this one is not based on the drain current expression of the FET. We showed that the sensitivity factors of the quiescent drain current can be calculated by repeated simulations of the bias circuit modified according to the change of a parameter value.

Key-Words: - Sensitivity factors, Bias circuits, FETs

1 Introduction

In the practical design of transistor circuits, the quiescent operating point Q is carefully established to ensure that the transistor will operate over a specified range, that linearity will be achieved and that P_{max} of device will not be exceeded. Once a design has been completed, it is necessary to check for quiescent point variations due to temperature changes and possible unit-to-unit parameter variations. These variations must be kept within acceptable limits as set by the specifications. Among the independent parameters which can cause a shift of the Q point of a FET are the following: the wide variation in the transconductance parameter β and threshold voltage for a particular transistor type; variation in the afore mentioned parameters due to their dependence on temperature; variations in the supply voltages due to imperfect regulation; variations in the circuit resistances due to tolerance and/or temperature effects [1] - [7].

Some of these parameters, e.g. temperature effects, are of importance for all designs while others, e.g. resistor tolerance and FET parameter variations, are more important when we are concerned with a production run of a number of identical amplifiers or large analog circuits [8] - [16].

2 Problem Formulation

In a FET, the threshold voltage and the transconductance parameter are functions of temperature. These parameters also vary somewhat from unit to unit as a result of differences in manufacturing process. This paper presents a way to find out the sensitivity factors of the drain current in bias circuits with FETs. In the next section, we discuss several methods to calculate the sensitivity factors of the drain current with rapport with two parameters of FET using a generalized bias circuit that controls the bias variation in the devices and covers all types of *n*-channel devices (JFET, enhancement- and depletion-mode MOSFET). Although *n*-channel FETs are used throughout, the same technique can be used to bias the *p*-channel type [6].

2.1 Generalized bias circuit

We consider a bias circuit widely used to control the bias variation in the FETs based on the DC negative feedback on drain current, which schematic diagram is shown in Fig. 1. The symbol *n*-channel written inside of the circle means any FET with *n* channel, i.e. NJFET, enhancement-mode NMOSFET and depletion-mode NMOSFET. This bias configuration is called generalized bias circuit because it can ensure the bias for all *n*-channel FETs and contents even the particular bias topologies used for JFET and depletion-mode MOSFET ($R_2 = \infty$). The resistance values and the supply voltage ensure a specified quiescent operating point in the active region for each device depending on its particular transfer characteristic curve. So, such a circuit must ensure a quiescent gate-to-source voltage V_{GSQ} with polarity and value adequate to the FET type as follows [7]:

- for a NJFET and depletion-mode NMOSFET operating into depletion mode, $V_{Th} < V_{GSQ} \leq 0$;
- for an enhancement-mode NMOSFET, $V_{th} < V_{GSQ} < V_{GSmax}$;
- for a depletion-mode NMOSFET operating into enhancement mode, $0 \leq V_{GSQ} < V_{GSmax}$.

The value of voltage V_{GSQ} depends on the specified quiescent point of FET.

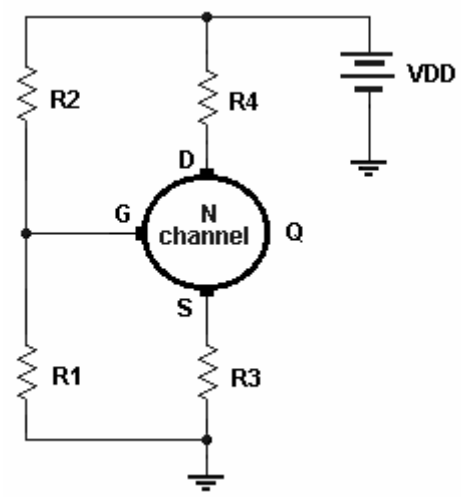

Fig. 1. The schematic diagram of the generalized bias circuit

2.1.1 Biasing the JFET

We consider the bias circuit in Fig. 1. In order that this topology to operate as a small-signal amplifier, we wish to bias this stage at a prescribed nominal value of quiescent drain-to-source voltage V_{DSQ}. The variation of the Q point with JFET-parameter variation is to remain within prescribed limits. To accomplish this, we must bias the JFET to ensure that the variation of quiescent drain current falls within prescribed limits since changes in I_{DQ} are reflected directly in V_{DSQ}.

The traditionally way to design such a circuit is based on the worst-case transfer characteristic curves of each particular JFET type utilizing a graphical procedure. These transfer curves are drawn assuming operation in the saturation or active region and show the worst-case variation of drain current as a function of gate-to-source voltage. For this operating mode, equation (1) or equivalently (2) applies:

$$I_D = I_{DSS}\,[1-(V_{GS}/V_{th})]^2, \quad (1)$$

$$I_D = \beta(V_{GS}-V_{th})^2. \quad (2)$$

In the above equations, I_{DSS} denotes the nominal saturation current and β is the transconductance parameter: $\beta = I_{DSS}/(V_{th})^2$. The equivalent form (2) of the drain current (1) allows us to unify the description of all FET types in the active region. So, the worst-case transfer curves give us the worst-case values of the JFET parameters: I_{DSSmin}, respectively β_{min} and I_{DSSmax}, respectively β_{max}, and V_{thmin} and V_{thmin}. These worst-case values of the JFET parameters are provided also by the manufacturer for each particular FET type.

The bias circuit given in Fig. 2 is the Thevenin equivalent circuit of the generalized bias circuit in Fig. 1, where $V_{GG} = [R_1/(R_1+R_2)]V_{DD}$ and $R_G = (R_1R_2)/(R_1+R_2)$. Since no DC current can flow into the gate of the FET, no DC current flows in R_G and the DC gate-to-source voltage is

$$V_{GS} = V_{GG}-I_D\,R_3, \quad (3)$$

where $V_{GG}=[R_1/(R_1+R_2)]V_{DD}$. The drain current is given by (1) or (2) and the drain-to-source voltage is

$$V_{DS} = V_{DD}-I_D\,(R_3+R_4). \quad (4)$$

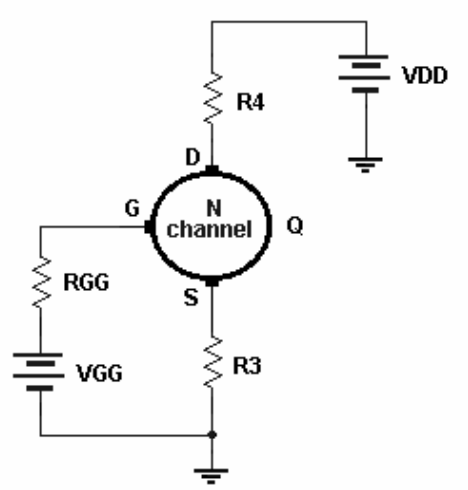

Fig. 2. The Thevenin equivalent circuit of the circuit given in Fig. 1.

The graphical design procedure of the stage is based on the worst-case transfer curves of a JFET and it is described in all electronics textbooks. Briefly, it is assumed that the nominal quiescent operating point (I_{DQ} and V_{DSQ}) and supply voltage V_{DD} are known. Also, the maximum allowable deviation from this nominal value ΔI_{DQ} is specified. Two worst-case operating points can be fixed on the transfer characteristics: Q_{max} corresponding to $I_{DQ,,max}$ and V_{GS1} and Q_{min} corresponding to $I_{DQ,min}$ and V_{GS2}. The straight line representing equation (3) must pass through the points Q_{max} and Q_{min} as shown in Fig. 3. The intersection of this line and V_{GS} axis yields V_{GG}, while the slope of line is $-1/R_3$. So,

$$R_3 = |\,V_{GS1}-V_{GS2}\,|/(I_{DQ,max}-I_{DQ,min}). \quad (5)$$

Then, the resistance R_4 is calculated:

$$R_4 = (V_{DD}-V_{DSQ})/I_{DQ}-R_3. \quad (6)$$

Choosing the current that flows through the resistors R_1 and R_2, and V_{GG} being known, the last resistances are calculated and the design of the bias circuit is now complete.

2.1.2 Biasing the MOSFET

The bias circuit in Fig. 1 works in the same fashion with JFET or MOSFET. The worst-case values of MOSFET parameters are given as $k_{max} = \beta_{max}$, $k_{min} = \beta_{min}$, and V_{thmax} and V_{thmin}. When the MOSFET is operating in the active region, the worst-case equations of the drain current are:

$$I_D = \beta_{max}\,(V_{GS}-V_{th,min})^2. \quad (7)$$

$$I_D = \beta_{min}\,(V_{GS}-V_{th,max})^2. \quad (8)$$

Equation (7) yields the largest I_D for a given value of V_{GS}, while (8) produces the smallest I_D. The design of the bias circuit is similar with that of JFET.

2.1.3 Drain current expression

Combining (2) and (3), we obtain a second-degree equation in unknown I_D:

$$aI_D^2 + bI_D + c = 0 \quad (9)$$

where:

$$a = \beta R_3^2;\ b = 2\beta R_3^2\left(V_{th} - V_{GG}\right) - 1;\ c = \beta\left(V_{GG}^2 + V_{th}^2\right).$$

The equation (9) has two solutions

$$I_{D1,2} = \frac{1}{2\beta R_3^2} \times \left[1 + 2\beta R_3\left(V_{GG} - V_{th}\right) \pm \sqrt{1 + 4\beta R_3\left(V_{GG} - V_{th}\right) - 8\beta^2 R_3^2 V_{GG} V_{th}}\right], \quad (10)$$

if the following inequality is accomplished:

$$1 + 4\beta R_3\left(V_{GG} - V_{th}\right) - 8\beta^2 R_3^2 V_{GG} V_{th} \rangle 0\,. \quad (11)$$

Among these two above solutions only one accepted solution is the quiescent drain current I_{DQ} namely that for which

$$V_{GG} - I_{DQ} R_3 \rangle V_{th}\,, \quad (12)$$

for all types of *n*-channel FET.

Now, we suppose that the worst-case of the FET parameters are known. The design problem of the bias circuit knows some aspects such as the following:

1. The nominal quiescent operating point and the maximum variation of drain current being specified or for a given performance specification such as the gain of the small-signal amplifier, it must find out the values of the resistances R_1, R_2, R_3 and R_4.
2. For given resistances R_1, R_2, R_3 and R_4, it must find out the maximum possible variation of I_{DQ} and V_{DSQ} taking into account the wide spread of the parameter values of FET and/or the temperature variations or voltage supply deviations.

The solution of the former formulation of design problem can be found using either a graphical or an analytical procedure.

We consider the nominal quiescent operating point given by I_{DQ}, V_{DSQ}, and the maximum variation of drain current specified as I_{DQmax} and I_{DQmin}. Firstly, we calculate the gate-to-source voltages corresponding to the variation limits of drain current:

$$V_{GS1} = V_{thmin} + (I_{DQmax}/\beta_{max})^{1/2}, \quad (13)$$

$$V_{GS2} = V_{thmax} + (I_{DQmin}/\beta_{min})^{1/2}. \quad (14)$$

Next, the Thevenin voltage V_{GG} and the resistance R_3 can be calculated:

$$V_{GG} = (V_{GS1} I_{DQmin} - V_{GS2} I_{DQmax})/(I_{DQmin} - I_{DQmax}), \quad (15)$$

$$R_3 = \left|(V_{GS1} - V_{GS2})\right|/(I_{DQ,max} - I_{DQ,min}). \quad (16)$$

Then, the resistance R_4 is found:

$$R_4 = (V_{DD} - V_{DSQ})/I_{DQ} - R_3. \quad (17)$$

Choosing the current that flows through the resistors R_1 and R_2, the last resistances are calculated and the design of the bias circuit is now complete.

The second aspect of design problem is related to so-called stability-factor analysis often used in engineering practice.

3 Sensitivity Factor Analysis

In the circuit in Fig. 1, any increase in drain current causes an increase in the source voltage, and therefore the gate-to-source voltage becomes more negative. This tends to reduce the current, thereby reducing the current increase which started the cycle. This sequence of events describes a negative feedback and resistor R_2 is responsible of stabilizing influence of the bias circuit.

Briefly stated, the problem of the stability-factor analysis is as follows: Given a physical variable (in our case, I_{DQ}), what change will it undergo when the variables on which it depends (in our case, V_{th}, β, V_{DD} etc.) change by prescribed (usually small) amounts? This type of analysis goes under various names, e.g., sensitivity analysis, variability analysis, and stability/sensitivity factor analysis. All these methods are based on assumption that, for small changes, the variable of interest is a linear function of the other variables and can be expressed in the form of a total differential. For our case, we write the quiescent drain current

$$I_{DQ} = I_{DQ}(\beta, V_{th}, V_{DD}). \quad (18)$$

Then the total differential is

$$dI_{DQ} = \frac{\partial I_{DQ}}{\partial \beta} d\beta + \frac{\partial I_{DQ}}{\partial V_{th}} dV_{th} + \frac{\partial I_{DQ}}{\partial V_{DD}} dV_{DD}\,. \quad (19)$$

Formally, likewise for a BJT, if the changes in the independent variables β, V_{th} and V_{DD} are small, we could define here three sensitivity factors of I_{DQ} as follows:

$$S_\beta = \frac{\Delta I_{DQ}}{\Delta \beta} \cong \frac{\partial I_{DQ}}{\partial \beta}; \quad (20a)$$

$$S_{V_{th}} = \frac{\Delta I_{DQ}}{\Delta V_{th}} \cong \frac{\partial I_{DQ}}{\partial V_{th}}; \quad (20b)$$

$$S_{V_{DD}} = \frac{\Delta I_{DQ}}{\Delta V_{DD}} \cong \frac{\partial I_{DQ}}{\partial V_{DD}}\,. \quad (20c)$$

Now, we can write that the total change ΔI_{DQ} in the quiescent drain current is proportional to the changes in each of the independent variables and to their sensitivity factors:

$$\Delta I_{DQ} = S_\beta \Delta\beta + S_{V_{th}} \Delta V_{th} + S_{V_{DD}} \Delta V_{DD}\,. \quad (21)$$

Unlike the quiescent collector current of a BJT, I_{DQ} is a strongly nonlinear function on all three variables, i.e. β, V_{th} and V_{DD}, as shows the equation (10). Moreover, large changes of the independent variables are involved.

Consequently, the procedure that applies to BJT to calculate the sensitivity factors cannot be applied to a bias circuit of a FET. However, in such a case, for given variation limits of β, V_{th} and V_{DD}, the total change in the quiescent drain current must be obtained directly, i.e.

$$\Delta I_{DQ} = I_{DQ}(\beta_{max}, V_{th\,min}, V_{DD\,max}) - I_{DQ}(\beta_{min}, V_{th\,max}, V_{DD\,min}) \quad (22)$$

In (22), the independent variables are chosen to maximize ΔI_{DQ} in order to provide a worst-case condition. Using (22) in conjunction with (4), the total change in the quiescent drain-to-source voltage results:

$$\Delta V_{DSQ} = \Delta V_{DD} + \Delta I_{DQ}(R_3 + R_4). \quad (23)$$

Such a procedure can be implemented by help of a computational package as Mathematica, Mathcad, Matlab etc.

To find each sensitivity factor of the quiescent drain current, we can employ a circuit simulator to calculate the actual increment of the quiescent drain current caused by the variation of only one independent variable [18]. This procedure will by described in the following.

Suppose a given bias circuit as that in Fig. 1. The circuit consists of a JFET_N sample, for which the β_0 and V_{th0} were measured at ambient temperature T=27°C. Let be V_{DD} the nominal voltage value of the supply. Let be JFET_N_e0 the simplified user model constructed utilizing only two parameter model of JFET, i.e. β_0 and V_{th0}, the rest of model parameter have the same values for all user models. Three other user models named in order JFET_N_b1 with the parameters β_1 and V_{th0}, JFET_N_t1 with the parameters β_0 and V_{th1}, and JFET_N_e with the parameters β_1 and V_{th1}, respectively, will be constructed too.

The three actual increments of the quiescent drain current corresponding to the three independent variables are denoted and calculated as follows:

- For a change in the transconductance parameter value, $\Delta\beta=\beta_1-\beta_0$,

$$\Delta I_{D,\beta}=I_{DQ}(\beta_1, V_{th0}, V_{DD})-I_{DQ}(\beta_0, V_{th0}, V_{DD}). \quad (24a)$$

- For a change in the threshold voltage, $\Delta V_{th} = V_{th1} - V_{th0}$,

$$\Delta I_{D,Vth}=I_{DQ}(\beta_0, V_{th1}, V_{DD})-I_{DQ}(\beta_0, V_{th0}, V_{DD}). \quad (24b)$$

- For a change in the supply voltage, $\Delta V_{DD} = V_{DD1}-V_{DD}$,

$$\Delta I_{D,VDD}=I_{DQ}(\beta_0, V_{th0}, V_{DD1})-I_{DQ}(\beta_0, V_{th0}, V_{DD}). \quad (24c)$$

If the variations of all three circuit parameters are considered to be simultaneous, then the total change in quiescent drain current will be

$$\Delta I_{DQ}=I_{DQ}(\beta_1, V_{th1}, V_{DD1})-I_{DQ}(\beta_0, V_{th0}, V_{DD}). \quad (25)$$

Four simulations of the bias circuit for a DC operating point analysis are needed to calculate the three actual increments of the quiescent drain current as follows: s_0 = nominal simulation for JFET_N_e0 and V_{DD}; s_1 = simulation for JFET_N_b1 and V_{DD}; s_2 = a simulation for JFET_N_t1 and V_{DD}; s_3 = a simulation for JFET_N_e0 and V_{DD1}. An additional simulation, s4, performed for the same circuit with JFET_N_e and V_{DD1} allows as to verify the validity of the equation (21) comparing its result with that given by equation (25).

4 Example

The proposed procedure to calculate the sensitivity factors of the quiescent drain current of a FET will be illustrated on the bias circuit in Fig. 3, derived from that shown in Fig. 1 and constructed with the NJFET type BF245A.

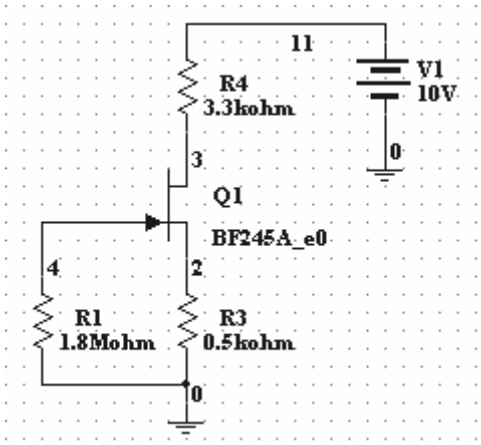

Fig.3. Bias circuit to be simulated

The proposed procedure has been tested by simulation with Multisim program [19]. For the first simulation, s_0, the device model is BF245A_e$_0$ where β_0=1.2 mA/V^2 and V_{th0} = -1.7 V. Then, we perform the second simulation of circuit, s_1, where the device model BF245A_b1 has the parameters β_1=1.5 mA/V^2 and V_{th0} = -1.7 V. The third simulation, s_2, is performed for device model BF245A_t1 with β_0=1.2 mA/V^2 and V_{th1} = -1.5 V. Finally, the fourth simulation, s_3, is performed for a device model BF245A_e with β_1=1.5 mA/V^2 and V_{th1} = -1.5 V, and V_{DD1}=12 V. The simulation results are summarized in Table 1, from which the actual increments of the quiescent drain current can be calculated.

Table 1. The simulation results.

s_i	I_{DQ} (mA)	ΔI_{DQ} (mA)	Δp	S_p
s_0	1.31			
s_1	1.44	0,13	$\Delta\beta$=0.3mA/V^2	0.43 V^2
s_2	1.09	-0.22	ΔV_{th}=0.2V	-1.1mA/V
s_3	1.31	0	ΔV_{DD}=2 V	0
s_4	1.22	-0.09	$\Delta\beta$=0.3mA/V^2 ΔV_{th}=0.2V	

The following general notations are used in above table: s_i for the simulations (s_0, s_1, s_2, s_3 and s_4), Δp for the parameter variations ($\Delta\beta$, ΔV_{th} and ΔV_{DD}) and S_p for the sensitivity factors of I_{DQ} (S_β, S_{Vth} and S_{VDD}).

The results given in Table 1 will be written again in order to be discussed. So, S_β=0.433 V^2, S_{Vth}=-1.1 mA/V and S_{VDD} =0, because I_{DQ} is independent on V_{DD} in the derived bias circuit in Fig. 3. Substitution of the sensitivity factor values and the parameter variations, i.e. $\Delta\beta$=0.3 mA/V^2, ΔV_{th}=0.2 V and ΔV_{DD}=2 V in equation (21) yields ΔI_{DQ}=0.43×0.3-1.1×0.2=0.13-0.22= -0.09 mA. On the other hand, substituting the results of simulations s_0 and s_4 in equation (25), the previous result is recovered, i.e. ΔI_{DQ}= -0.09 mA. This latest result validates the proposed procedure to calculate the sensitivity factors of quiescent drain current of a FET. Also, other result provided by simulations s_0 and s_4 is obtained in the form of total variation of the drain-to-source voltage: ΔV_{DSQ}= 1.65 V. Equation (23) for ΔV_{DD}=2 V and ΔI_{DQ}= -0.09 mA yields the same result, i.e. ΔV_{DSQ}= 1.65 V.

5 Conclusion

The paper proposes a procedure to calculate the sensitivity factors of the quiescent drain current of a FET operating in the active region in conjunction with a general-purpose circuit simulator. Unlike the procedure developed for the sensitivity factors of the quiescent collector current in BJT, this one is not based on the drain current expression of the FET. We demonstrated that the sensitivity factors of the quiescent drain current can be calculated by repeated simulations of the bias circuit. Each change of a circuit parameter involved in the sensitivity analysis modifies either the device model or the parameter values.

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